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PERFORMANCE ASSESSMENT AND ANALYSIS OF 31-LEVEL INVERTERS WITH REDUCED COMPONENTS FOR HYBRID RENEWABLE SYSTEMS

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Abstract

The available multilevel inverters are suitable for renewable energy applications, especially hybrid systems, as they improve the power quality and prevent the negative effects of renewable energies on the electricity grid. However, the standard multilevel inverters use several components to achieve a desired level, which increases cost, switching loss, and circuit complexity. The challenge is to design a multilevel inverter to achieve the same desired level with a reduced number of components and low total harmonic distortion (THD) to enhance the overall system efficiency. The objective of this study is to introduce a new design of a 31-level asymmetric multilevel inverter with only 10 power switches and four DC sources with a 1:2:5:10 direct current voltage ratio. The switches of the proposed design are triggered through a phase disposition level-shifted pulse width modulation technique. The proposed circuit was simulated using the MATLAB/SIMULINK program, where the simulation results show a capability of effective control, achieving a 31-level with low voltage and current THDs. For the R-load, the voltage and current THDs are 1.05%. While for the RL-load, the voltage THD is 1.05% and the current THD is 0.25%. The comparison with previous designs points out that the proposed multilevel inverter product can reach a 31-level with a lower number of components and less distortion.

Keywords: Multi-carrier PWM, Multilevel inverters, Renewable energy, Total harmonic distortion.

1. Introduction

In comparison with two-level inverters, multilevel inverters (MLIs) have received attention due to their ability to reach a high output voltage with low total harmonic distortion (THD). Recently, multilevel inverters have gained attention due to their high-quality output power and high efficiency, especially in renewable energy applications. Among the renewable energy sources, solar energy and wind turbines are becoming more prevalent. They are increasingly integrated into modern power systems to promote greater sustainability, enhance energy efficiency, and support the transition to cleaner and more resilient energy solutions. To ensure the smooth integration of renewable energy sources, advanced power conversion technologies, including multilevel inverters, are pivotal.

These conversion technologies are designed to effectively manage and convert renewable energies. They facilitate better energy storage, distribution, and consumption by enhancing the performance and reliability of energy conversion, while mitigating losses and enhancing system efficiency. This enables more successful use of renewable energy in several sectors, driving sustainability and energy resilience [1, 2]. Multilevel inverters provide several benefits over conventional two-level inverters, including the capacity to attain greater output voltage levels, a considerable mitigation in distortion, a reduction in electromagnetic interference, and voltage stress on switches. Because of these advantages, multilevel inverters are well suited for renewable energy and sustainable power applications [3, 4].

On the other hand, conventional MLIs, including neutral-point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters, demand a larger number of components, which in turn results in higher switching losses, elevated costs, and increased complexity in the overall circuit design [5]. To address these drawbacks, reduced-switch multilevel inverter topologies have been proposed to achieve comparable performance while using fewer components [6, 7].

Among the available MLI topologies, cascaded H-bridge (CHB) inverters have attracted considerable attention owing to their modular structure and operational flexibility [8, 9]. Based on the structure of the DC input voltages, cascaded H-bridge inverters are classified into two types: asymmetric and symmetric cascaded inverters. Asymmetric CHB inverters are widely adopted because they can generate a larger number of output voltage levels using unequal DC source magnitudes [10]. Many DC input voltage structures have been suggested to obtain a 31-level. Among the asymmetric DC-source configurations reported in the literature, the voltage ratios 1:2:4:8 and 1:2:5:10 are the most widely adopted owing to their ability to generate a high number of voltage levels with a reduced number of power components [11-17].

In terms of control and modulation techniques, many methods have been proposed to drive multilevel inverters. Selecting the right modulation technique is essential for efficient multilevel inverter control. Modulation techniques are generally classified according to their switching frequency into fundamental-switching (FS) and high-switching-frequency (HS) categories [18]. Fundamental-frequency modulation techniques include selective harmonic elimination (SHE), sine property control, and staircase control with fixed time steps [19-22]. While the most common inverters use high switching frequencies to control the gates, some

of these techniques include multi-carrier PWM (phase disposition and phase shifted), Hybrid PWM, and space vector PWM [23-27].

Increasing the number of output voltage levels generally reduces the THD of the inverter output waveform; however, this is often accompanied by an increase in the required number of power components [28]. Therefore, a higher level of MLIs is effective only when fewer components are used. Researchers have designed many 31-level MLI topologies. Dhanamjayulu et al. [11] proposed a 31-level single-phase inverter employing 12 switches and four DC sources. It utilizes a staircase PWM technique to generate pulses for gates.

Antar [16] developed a 31-level inverter utilizing 10 power switches and four DC sources. The results were simulated with two different controllers, which are phase disposition level-shifted-PWM and a modified absolute sinusoidal PWM; both controllers achieved low THDs. Saravanan et al. [29] proposed a practical 31-level multilevel inverter employing 12 switches, four DC sources, and four capacitors for electric vehicle applications. They used a multi-carrier PWM technique, and the results achieved a THD of 2.16% .

Based on the past studies of the multilevel inverters, the main purpose is to decrease the number of components, including switches and DC sources, in order to reduce cost and increase efficiency by reducing switching loss. Also, it reduces implementation cost and circuit complexity. Thus, this study proposes a 31-level multilevel inverter design that requires only ten switches and four DC sources. The key objectives are to achieve a high level of output voltage with lower distortion to enhance the power quality. The circuit operation is governed by a PDPWM control, which manages the switching actions to attain the desired level of output voltage.

In the paper, Section 2 describes the proposed inverter design and switching processes. Section 3 explains the findings, followed by a comparison to previous research. Finally, Section 4 wraps up the study by summarizing the key findings and suggesting future research possibilities.

2. Coefficients Development and Assessment Methodology

This study proposes a 31-level asymmetric multilevel inverter with only 10 power switches (IGBT) and four DC voltage sources, as shown in Fig. 1. This inverter is designed with fewer components, which helps reduce switching losses, cost, and complexity of design. The voltage sources are arranged according to a 1:2:5:10 Direct Current Voltage (Vdc) ratio to achieve the desired level. Accordingly,

$V_1 = \text{Vdc}$; $V_2 = 2\ \text{Vdc}$; $V_3 = 5\ \text{Vdc}$; and $V_4 = 10\ \text{Vdc}$.

According to Eqs. (1) and (2), the traditional cascade H-bridge inverters need 60 power switches and 15 DC input voltages to achieve a 31-level output voltage [16].

$$\text{Number of switches} = 2(M-1) \quad (1)$$

$$\text{Number of input voltages} = \frac{(M-1)}{2} \quad (2)$$

where M is the number of levels.

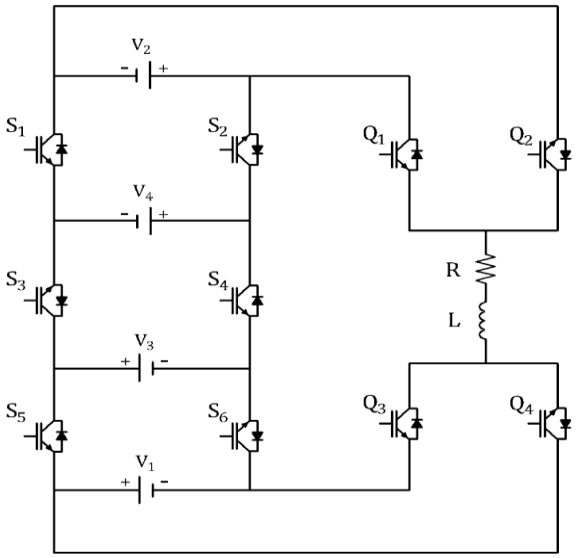

Fig. 1. Circuit of the proposed asymmetric 31-level MLI topology.

Table 1 presents the switching states of the proposed 31-level inverter. Each row corresponds to a specific state, detailing the combination of conducting switches (where '1' indicates ON and '0' indicates OFF) and the resulting output voltage level. The inverter, shown in Fig. 1, uses 10 switches (S_1 to S_6 and Q_1 to Q_4) to generate a stepped output voltage waveform. In this work, a 4 kHz switching frequency-based phase disposition level-shifted pulse width modulation (PDPWM) technique is used to generate gate pulses. It uses multiple carrier signals that are shifted vertically and compared with a single reference signal to generate switching signals for each level of the inverter.

Figure 2 illustrates the current paths for five operating modes of the proposed multilevel inverter: (a). +15 Vdc, (b). +7 Vdc, (c). 0 V, (d). -7 Vdc, and (e). -15 Vdc. Each mode is achieved by controlling specific switches to combine the appropriate voltage sources. The red arrows indicate the current flow direction through the active components and the load. This demonstrates the inverter's ability to generate five distinct output levels by varying the conduction path, enabling efficient voltage synthesis and improved waveform quality.

Table 1. Switching states of a 31-level inverter.

State	Conducting switches 1 = ON, 0 = OFF										Output voltage (V)
	S_1	S_2	S_3	S_4	S_5	S_6	Q_1	Q_2	Q_3	Q_4	
1	0	1	1	0	0	1	1	0	1	0	$10V_{dc} + 5V_{dc} = +15V_{dc}$
2	0	1	1	0	0	1	1	0	0	1	$10V_{dc} + 5V_{dc} - V_{dc} = +14V_{dc}$
3	0	1	1	0	0	1	0	1	1	0	$10V_{dc} + 5V_{dc} - 2V_{dc} = +13V_{dc}$
4	0	1	1	0	0	1	0	1	0	1	$10V_{dc} + 5V_{dc} - 2V_{dc} - V_{dc} = +12V_{dc}$
5	0	1	1	0	1	0	1	0	1	0	$10V_{dc} + V_{dc} = +11V_{dc}$
6	0	1	1	0	1	0	1	0	0	1	$10V_{dc} = +10V_{dc}$

7	0	1	1	0	1	0	0	1	1	0	$10V_{dc} + V_{dc} - 2V_{dc} = +9V_{dc}$
8	0	1	1	0	1	0	0	1	0	1	$10V_{dc} - 2V_{dc} = +8V_{dc}$
9	1	0	1	0	0	1	1	0	1	0	$5V_{dc} + 2V_{dc} = +7V_{dc}$
10	1	0	1	0	0	1	1	0	0	1	$5V_{dc} + 2V_{dc} - V_{dc} = +6V_{dc}$
11	1	0	1	0	0	1	0	1	1	0	$5V_{dc} = +5V_{dc}$
12	1	0	1	0	0	1	0	1	0	1	$5V_{dc} - V_{dc} = +4V_{dc}$
13	1	0	1	0	1	0	1	0	1	0	$V_{dc} + 2V_{dc} = +3V_{dc}$
14	1	0	1	0	1	0	1	0	0	1	$2V_{dc} = +2V_{dc}$
15	1	0	1	0	1	0	0	1	1	0	$V_{dc} = +V_{dc}$
16	1	0	1	0	1	0	0	1	0	1	0
17	0	1	0	1	0	1	1	0	0	1	$-V_{dc} = -V_{dc}$
18	0	1	0	1	0	1	0	1	1	0	$-2V_{dc} = -2V_{dc}$
19	0	1	0	1	0	1	0	1	0	1	$-(V_{dc} + 2V_{dc}) = -3V_{dc}$
20	0	1	0	1	1	0	1	0	1	0	$-(5V_{dc} - V_{dc}) = -4V_{dc}$
21	0	1	0	1	1	0	1	0	0	1	$-5V_{dc} = -5V_{dc}$
22	0	1	0	1	1	0	0	1	1	0	$-(5V_{dc} + 2V_{dc} - V_{dc}) = -6V_{dc}$
23	0	1	0	1	1	0	0	1	0	1	$-(5V_{dc} + 2V_{dc}) = -7V_{dc}$
24	1	0	0	1	0	1	1	0	1	0	$-(10V_{dc} - 2V_{dc}) = -8V_{dc}$
25	1	0	0	1	0	1	1	0	0	1	$-(10V_{dc} + V_{dc} - 2V_{dc}) = -9V_{dc}$
26	1	0	0	1	0	1	0	1	1	0	$-10V_{dc} = -10V_{dc}$
27	1	0	0	1	0	1	0	1	0	1	$-(10V_{dc} + V_{dc}) = -11V_{dc}$
28	1	0	0	1	1	0	1	0	1	0	$-(10V_{dc} + 5V_{dc} - 2V_{dc} - V_{dc}) = -12V_{dc}$
29	1	0	0	1	1	0	1	0	0	1	$-(10V_{dc} + 5V_{dc} - 2V_{dc}) = -13V_{dc}$
30	1	0	0	1	1	0	0	1	1	0	$-(10V_{dc} + 5V_{dc} - V_{dc}) = -14V_{dc}$
31	1	0	0	1	1	0	0	1	0	1	$-(10V_{dc} + 5V_{dc}) = -15V_{dc}$

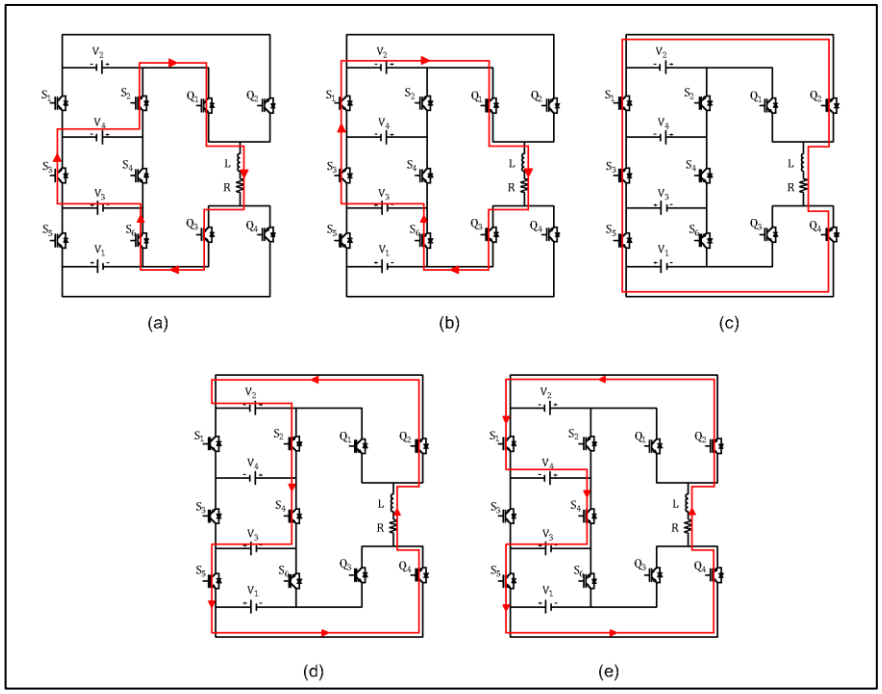

Fig. 2. Current paths at different operating modes: (a) +15 Vdc, (b) +7 Vdc, (c) 0 V, (d) -7 Vdc, and (e) -15 Vdc.

3. Results And Discussion

The proposed 31-level inverter was simulated using the MATLAB/Simulink software. The DC voltage sources used in simulation are as follows: V1 = 21.8 V, V_2 = 43.6 V, V_3 = 109 V, and V_4 = 218 V. These voltage values were chosen to ensure that the desired RMS voltage is obtained, which is 230 V. As mentioned previously, the modulation technique used in this study is multi-carrier PWM, specifically phase disposition level-shifted pulse width modulation (PDLSPWM), as shown in Fig. 3. This technique is widely used due to its simplicity and effectiveness in reducing harmonics. It uses multi-carrier signals that are in phase with each other but shifted vertically to meet the voltage levels' amplitude range. This PWM technique was employed to generate the appropriate pulses for the IGBTs' gates. According to the results, the PDLSPWM technique effectively achieved the desired output level with low THDs.

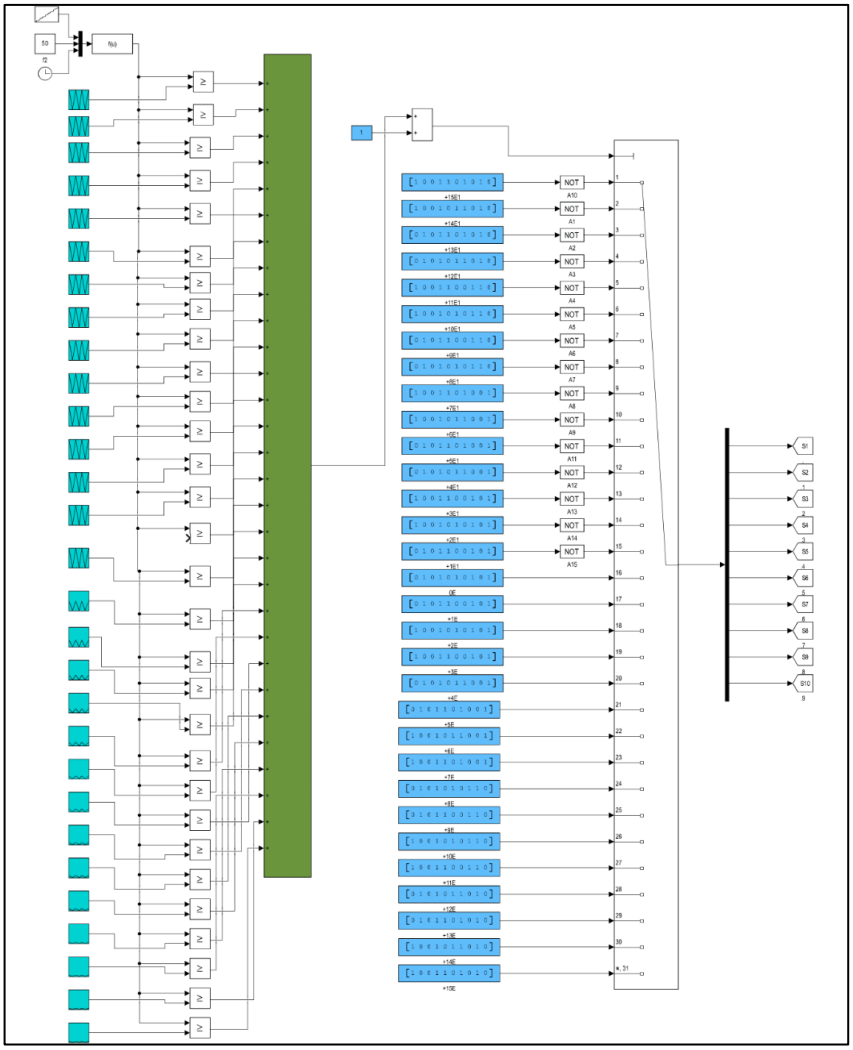

Fig. 3. PDLSPWM control.

The inverter's performance was examined under two load conditions: an R-load (20 Ω) and an RL-load (20 Ω and 80 mH). The output voltage and current waveforms under the R-load condition are shown in Fig. 4, with their THDs presented in Figs. 5 and 6, respectively. The inverter configuration presented in Fig. 4 generated a stepped sinusoidal voltage waveform corresponding to the voltage levels. As the load here is pure resistance, the current and voltage signals are in phase with each other and have the same THD values, which is 1.05% for both.

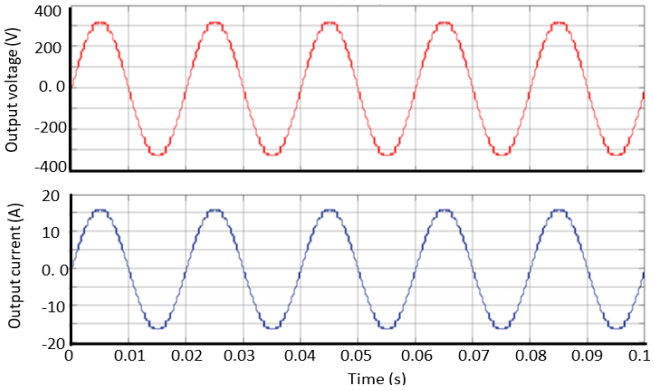

Fig. 4. Output voltage and current of the proposed inverter (R-load).

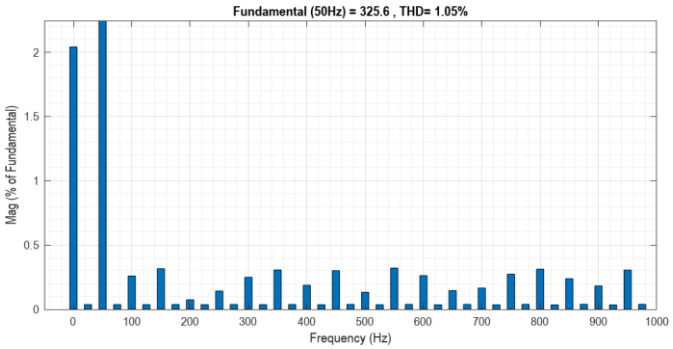

Fig. 5. Voltage THD (R-load).

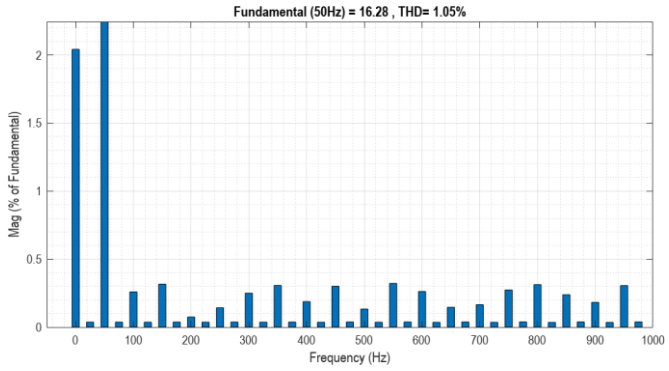

Fig. 2. Current THD (R-load).

Figure 7 illustrates the voltage and current waveforms for the RL-load, while their corresponding THDs are displayed in Figs. 8 and 9. For the RL-load, the voltage THD remains the same value of 1.05%; meanwhile, the current THD decreased to 0.25% as the inductor filtered the current signal. The stepped shape of the output current becomes smoother due to the presence of the inductor, which also causes the current to lag behind the voltage. The results are compared with the most recent related works in the literature, which are presented in Table 2. According to the comparison, the proposed inverter can effectively achieve 31-level output waveforms with fewer components and lower THDs. The comparison is conducted in terms of the number of power switches (SW), diodes (D), DC sources (DC), ratio of DC sources (DCR), voltage THD (%THD-V), and current THD (%THD-I).

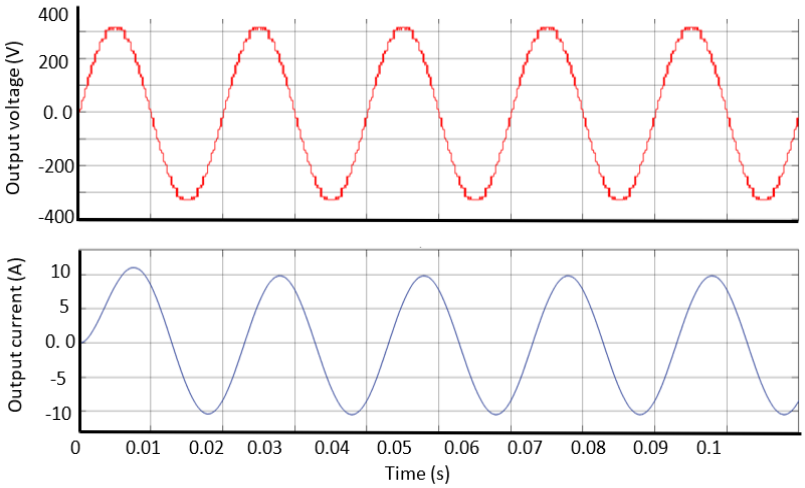

Fig. 7. Output voltage and current of the proposed inverter (RL-load).

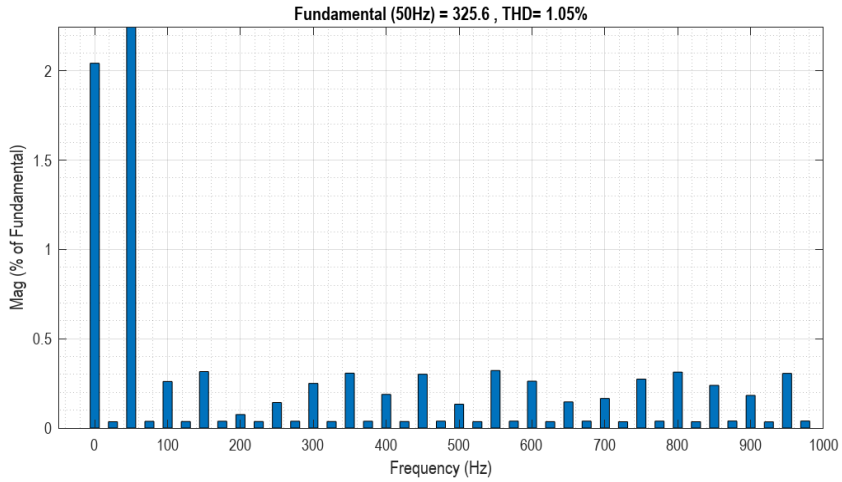

Fig. 8. Voltage THD (RL-load).

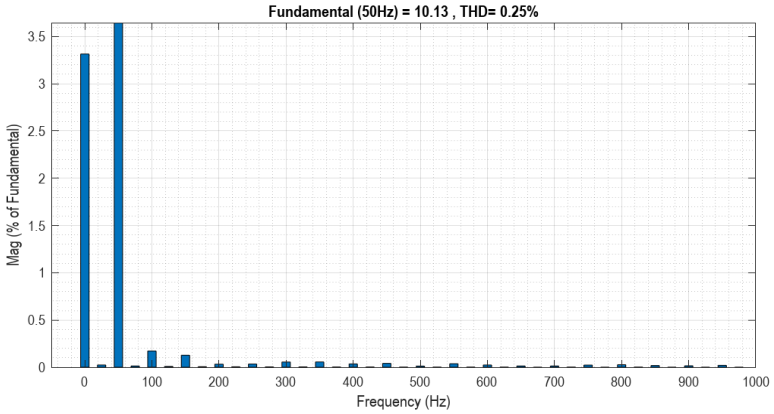

Fig. 9. Current THD (RL-load).

Table 1. Comparison of the suggested multilevel inverter with some of the related inverters

Reference	SW	D	DC	DCR	%THD-V	%THD-I
Dhanamjayulu et al. [11]	12	-	4	(1:2:4:8) Vdc	3.35	3.35
Jayakumar et al. [13]	8	4	4	(1:2:4:8) Vdc	(3.37) MCM tech. (3.13) ABC-SHE tech.	-
Prasad et al. [14]	14	-	4	(1:2:4:8) Vdc	3.35	-
Verma et al. [15]	12	-	4	(1:2:4:8) Vdc	4.04	2.15
Dhanamjayulu et al. [17]	10	-	4	(1:2:5:10) Vdc	3.62	3.71
Akther et al. [30]	12	-	4	(2:4:8:16) Vdc	6.72	6.71
Proposed MLI in the current work	10	-	4	(1:2:5:10) Vdc	1.05 (R-load) 1.05(RL-load)	1.05 (R-load) 0.25 (RL-load)

4. Conclusions

This work suggested a topology of a 31-level asymmetrical multilevel inverter with high-quality power and few components for renewable energy applications, particularly a hybrid system. This inverter uses only 10 IGBT switches and 4 DC sources, with a voltage structure in the ratio of 1:2:5:10 Vdc. The purpose was to design a reduced switch MLI to reduce cost, switching loss and simplify the circuit. The proposed topology could reach the desired 31-level with minimum distortion and fewer components. The gates of the power switches (IGBTs) were triggered by PDLSPWM control. It effectively turns on and off the switches to ensure proper switching operation and enhance power quality.

MATLAB/SIMULINK simulation tool was employed to investigate the performance of the proposed inverter. The simulation results show that the proposed inverter is efficient and successful, especially for renewable energy sources, as it reduces distortion, which increases the power quality. The inverter

was simulated with two different loads, namely, R-load and RL-load. For the pure resistive load, the voltage and current waveforms are in phase and have the same low THD value of 1.05% for both. For the RL-load, the voltage THD remained at 1.05%, yet the current THD decreased to 0.25% due to the effect of the inductor, and the current ripple (discrete steps) reduced. Compared with the most recent related works, the proposed multilevel inverter can compete with the existing inverters in terms of reducing components and minimizing the distortion.

For the future, the performance of the inverter can be validated through real-time experimental testing under a variety of load conditions. Additionally, this multilevel inverter can be redesigned with renewable energy sources, specifically a hybrid system, replacing the DC sources.

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Nomenclature

CHB	Cascaded H-Bridge
DC	Direct Current
FC	Flying Capacitor
M	Number of levels
NPC	Neutral-Point Clamped
PDLSPWM	Phase Disposition Level-Shifted Pulse Width Modulation
PWM	Pulse Width Modulation
RMS	Root Mean Squared
THD	Total Harmonic Distortion
Vdc	Direct Current Voltage

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