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A REAL TIME AMPLITUDE COMPENSATION METHOD USING LED CURRENT REGULATION SYSTEM FOR OPTICAL ENCODERS

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Abstract

Encoders are angular and speed position sensors that are mainly use in a motor feedback system. Optical encoders use the photodiodes to generate photocurrent in response to the light source or rather the Light Emitting Diodes (LEDs). The LEDs will degrade over time while the optical strength is sensitive to the temperature. Amplitude of an encoder signals is one of the three critical parameters in determining an encoder performance. This paper will present a method of regulating the LED current to maintain and compensate the amplitude signals using the available LED current. This method has been simulated using MATLAB and implemented in an encoder system designed using the 0.18 µm CMOS process. The proposed system has been fabricated, measured and the results are compared to the simulated results. The outcome shows that the system is able to regulate the LED current to compensate for the degradation and loss of LED power due to external variation such as temperature that affects the amplitude of the signals. From the measurement, without this method of amplitude compensation, the (Voltage Peak to Peak) Vpp of the signals can varies roughly +/- 200mV across temperature, but with this proposed method, the amplitude is maintained with variation around +/- 10mV by regulating the LED current.

Keywords: Amplitude correction, Analog LED regulation for encoders, Encoders, Sinusoidal optical encoders.

1. Introduction

Encoders are motion control sensors usually used in a feedback system for motor controls. Cronin D.V. patented one of the earliest modern encoders using the optical sensing technology using huge photocells as an optical sensing element and a light bulb as the optical source [1]. Many early literatures can be found in encoders using the optical sensing technology [2-7]. In some of the earlier encoder sensing technology, optical encoders are present in a wide range of applications involving motion control such as in elevators and servomotors [8, 9]. Optical encoders are key components in industrial, automotive and consumer industries [10, 11].

The objective of this paper is to present a method in solving one of the unwanted effects in the signals that is caused by the optical light source in an optical encoder while maintaining some flexibility in the components used. Generally, an optical light source which is constructed from a LED has its limitation and lifetime. The amount of LED power or the brightness of the LED will vary with temperature. Different units of some similar LEDs will also have some variation in power.

To determine the speed and direction of the motion, the encoder requires at least two signals with 90 degrees apart generated by the sensing elements. These two signals can be converted into four signals by means of having more photodiode pairs and code pattern or making a differential output signal using a differential amplifier [12]. These signals will then be amplified before it is processed and calibrated. However, these signals will not be ideal and contained dc offsets, varying amplitude, phase shifts and noise. These non-idealities come from the sensor construction, mechanical construction and the variation of fabrication processes. Thus, to achieve better performance, these signal defects need to be corrected. Some of these defects can be corrected or calibrated during the one-time factory calibration process. However, for defects that are caused by degradation over lifetime or temperature would need a real time detection and correction.

The amplitude difference between two or four signals can be corrected during a one-time factory calibration. However, in the case of amplitude drop or in some condition - amplitude increases due to mechanical movement, mechanical construction imperfection or LED power variation over temperature and degradation over lifetime, these defects would need a real time detection and correction. It is favourable to have the correction of the LED as subtle as possible as sudden change in the LED power will cause spikes or drastic change to the analog signals when mishandling occurs. These sudden changes to the analog signals will cause the encoder performance to degrade instantly, which is not favourable. The proposed method is to regulate (increase or decrease) the LED current which could maintain the LED power so that the amplitude of the signals can be maintained across lifetime, temperature variation also environmental condition.

Previous published papers presented a LED driver circuit which consisted of multiple current regulators and a voltage pre-regulator using adaptive output voltage to keep voltage drop across several LED string at minimum [13]. A boost type LED driver with an on-chip ambient light sensing was proposed to control the LED current based on the surrounding illumination [14]. This is being used in a liquid crystal display backlight module. Another proposal was using a digital control mechanism employing a resistive digital to analog converter for feeding the analog feedback to give it an optimum control and flexibility over the relation speed and stability [15]. There is also a proposal of using an adaptive feedback gain

compensation technique and adaptive feedforward loop control-based design [16]. The proposals in these papers are mostly on detecting a stable DC signal and not real time dynamic signal. In an encoder application, it is more desirable to detect and maintain the source of the input sinusoidal signals which affect the performance. Having multiple LEDs are also not desirable in an encoder application, as the placement of several LEDs will create optical crosstalk resulting in signal distortion. As for amplitude correction in an optical encoder, a proposal using a digital signal processor (DSP) with a look up table stored is used to correct the amplitude imperfection [17]. A similar method has been proposed in paper [18] which the use of digital algorithm is needed with a microprocessor or controller. With such prior arts, there are not many references on compensating amplitude of the optical encoder signals with LED regulation method, as proposed here.

In the current market an encoder does not have a LED regulation circuit. Instead, the encoder depends on the lifetime of the LED, and once the LED degrades, the whole encoder will be replaced. Other more recent encoder products with LED regulation do not need the external circuitry of the NPN and resistor (Re) as proposed in Fig. 1. This method saves cost, compromising on the flexibility of using different types of LED as well as the flexibility of using different initial LED current values. The benefit of the proposed method of LED regulation is to have the flexibility of using different types of LED as the technology improves without the need to change ~~of~~ the encoder (Application Specific Integrated Circuit (ASIC) design. When the LED light intensity versus the LED current improves, these can be easily solved using a different type of resistor (Re) values. This paper is intended for optical encoder sensor ASIC design which is able to track and compensate any drop in amplitude during real time. This is done by regulating the LED current without compromising on the performance. This design does not need much overhead in resources such as a memory, digital processing or converters.

This paper proposes an analog method to detect the sinusoidal signals changes and regulate the LED to maintain the amplitude of the signals in real time using merely analog blocks without digital implementation nor overhead. External circuitries used are presented in Fig. 1 and a more detailed explanation is in Fig. 2. The rest of the paper is organized as follows: Section 2 introduces an overview of a general optical encoder sensor system and the interface with external circuitries. Section 3 proposes the method and concept of LED current regulation with modelling results. Section 4 shows the implementation of the concepts and simulation results, while Section 5 provides the measured results from the actual fabrication of the design. The conclusion of this paper is presented in Section 6.

2. System Overview

In a typical optical encoder design, the light source consists of a LED that shines the light through an aperture of pattern on the code disk. These patterns will be detected by the photodiode sensors in the ASIC, converting the light pattern into photocurrents, which will then be amplified into usable voltage signals. The sensor output is a pair of quadrature signals, which for sinusoidal signals are two sinusoidal signals with 90 degrees apart, named as SP and CP in this paper. The generation of an inverse of the signals 180 degrees apart from the two sinusoidal signals are also common. They are known as SN and CN where SN is 180 degrees apart from SP and CN is 180 degrees apart from CP. These signals will then need

to be amplified to make it usable for the next part of the signal processing. The changes of the LED light source will affect the amplitude of these signals caused by the mechanical construction movement, degradation of the LED over lifetime, temperature variation on the LED power or even physical blocking of the light due to dust or particles. Some of these changes can be permanent while some can be temporary. Thus, a detection and compensation method to regulate the LED power so that the voltage signal is consistent is needed to prevent degradation of performance in the encoder.

2.1. Overview of a block diagram of an optical encoder with LED regulation circuit

Figure 1 shows an example of the block diagram in an optical encoder with a LED current regulation block. To complete the system, there is also an external NPN transistor and some passive components such as a resistor and a capacitor to control the current going through the LED thus controlling the brightness of the LED. Resistor Rb and capacitor Cb is a filter circuit which can be modified in terms of frequency or speed of change to the regulation depending on the application. Most of the time, any optical light changes are preferred gradually as the compensation are mainly due to degradation of the LED and temperature. Having these external components in the system would allow the flexibility of changes and modification to suit its application needs.

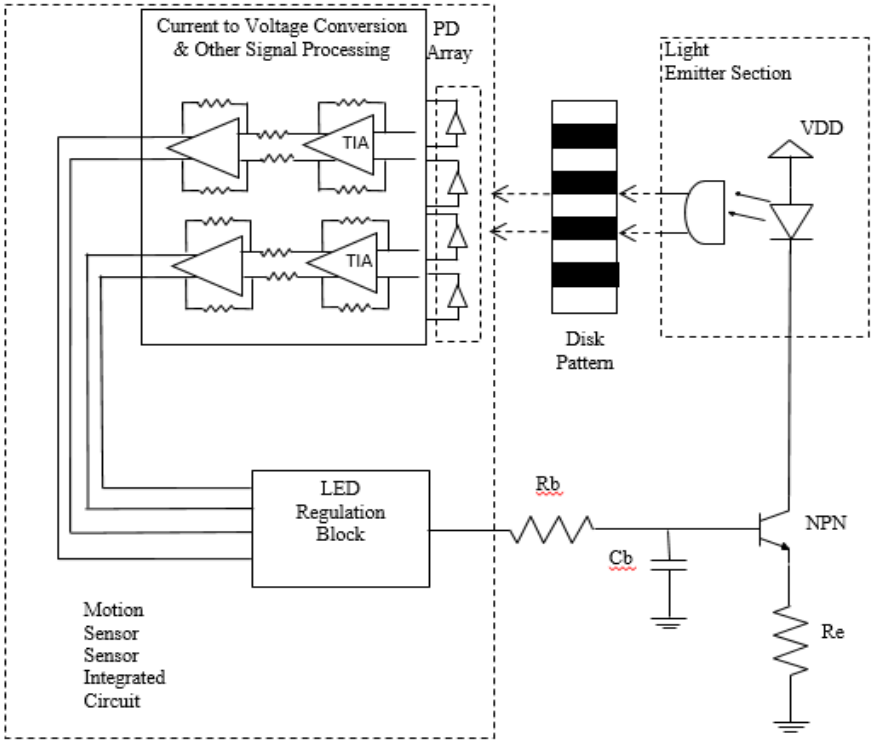

Fig. 1. An example of block diagram of an optical encoder with a LED regulation circuit.

2.2. Parameters in the system

The three dominant parameters that will cause degradation of the encoder performance are the dc offset, amplitude variation and phase shifts. Amplitude variation is inherited from the initial construction and process variation, but it can be corrected or compensated during the assembly of the encoder. However, for amplitude changes that degrade the LED and the light power of the LED in operation a real time detection and compensation method is required. For a low-cost simple encoder, the regulation of the LED current can be done by using the proposed method in this paper.

3. LED Regulation Concept

Figure 2 shows a part of Fig. 1, which derived the LED regulation concept. It shows the external components of the circuit, such as resistors (R_b and R_e), transistor (NPN), capacitor (C_b) and LED. The calculation for the LED current control is based on the external components part. V_{reg} is a voltage that tracks the amplitude of the sinusoidal SP, SN, CP and CN signals. R_b is the resistor that converts V_{reg} into current, I_b which is used in the NPN transistor to control the current that flows through the LED. Capacitor C_b is used to smoothen out any unwanted abrupt or high frequency changes in V_{reg}. R_e is a resistor located at the emitter portion of the NPN transistor. As I_b is much smaller compared to I_c or I_{LED}, the I_e is assumed to be approximately equalled to I_c and I_{LED}. An equation to calculate the current through the LED with respect to V_{reg} can be modelled in Eq. (1).

$$I_e \sim I_c \sim I_{LED} = \frac{V_{reg} - (I_b R_b) - V_{be}}{R_e} \quad (1)$$

Based on Eq. (1), the LED current will increase if the detected amplitude of the sinusoidal signals is lower than required and decrease if the detected amplitude of the signals is higher than required. In other words, the voltage, V_{reg} is inversely proportional to the amplitude of the sinusoidal signals. Maximum value for V_{reg} is determined by the dropout voltage of the external components as well as the voltage range of the power supply. It is designed to be limited by the LED Reg block design. External factors that affect the limit of the voltage are the power supply VDD and the forward voltage (VF) of the LED. The equation below shows the needed voltage so that the external NPN transistor will be in active region.

$$VDD - LED_{VF} = V_{ce} > V_{be} \quad (2)$$

To conceptualize the idea, a DC voltage needs to track the amplitude of the sinusoidal signals and the concept can be derived from the trigonometry formula below.

$$\sin^2 + \cos^2 = 1 \quad (3)$$

Proof of concept

The MATLAB simulation results are shown from Figs. 3 to 5. Figure 3 shows two sinusoidal signals SP and CP with an ideal 1Vpp generating a DC output of 1 using the Eq. (3). Figure 4 shows the effect of a smaller amplitude in SP and CP while Fig. 5 shows the effect of a bigger amplitude in SP and CP. The DC output is proportional to the amplitude changes.

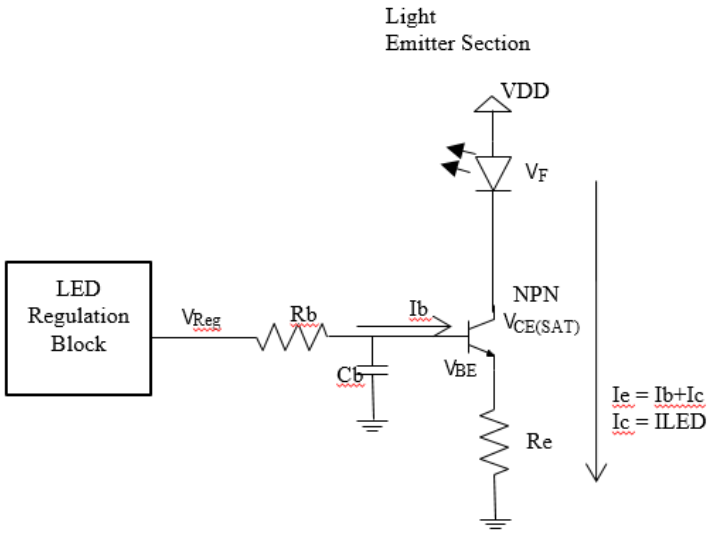

Fig. 2. Block diagram of the components used in the LED regulation concept.

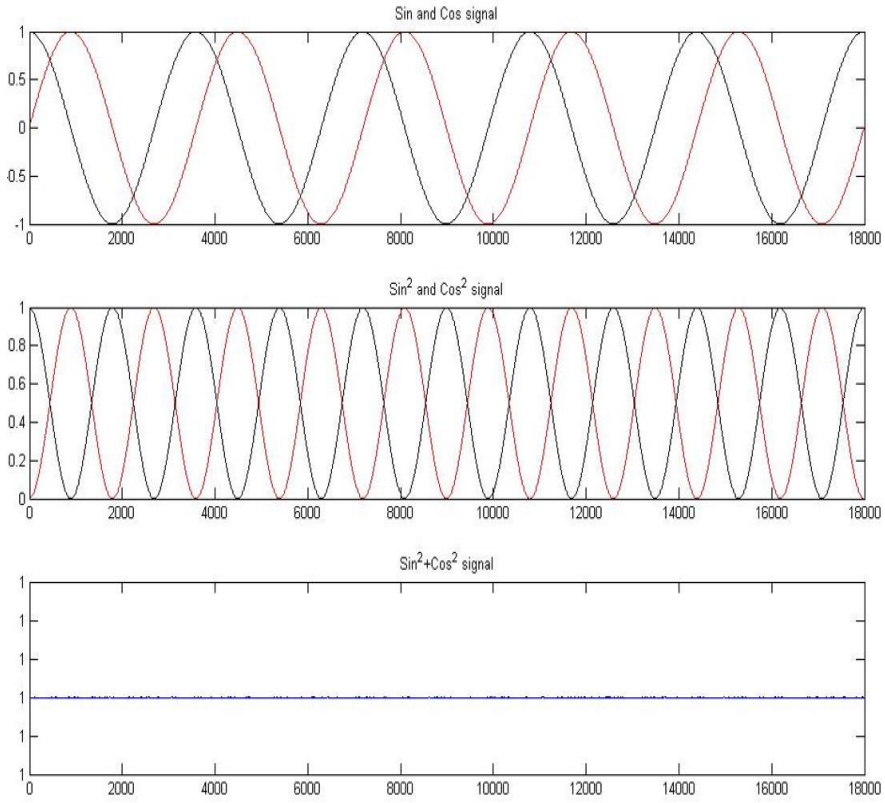

Fig. 3 (a) Two inputs of Sin and Cos signal at 1Vpp,
(b) Sin^2 and Cos^2 signals, (c) Summation of Sin^2 and Cos^2 signals.

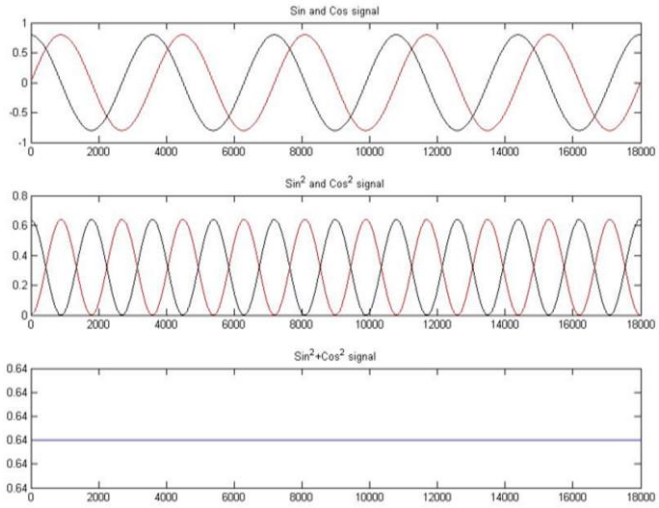

Fig. 4 (a) Two inputs of Sin and Cos signal at lower Vpp, (b) Sin^2 and Cos^2 signals, (c) Summation of Sin^2 and Cos^2 signals.

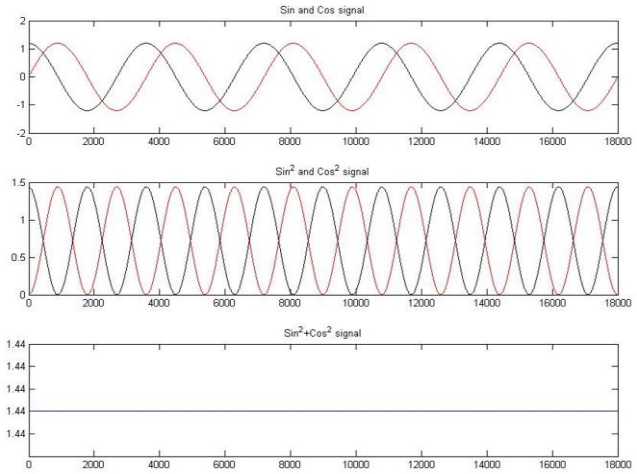

Fig. 5 (a) Two inputs of Sin and Cos signal at higher Vpp, (b) Sin^2 and Cos^2 signals, (c) Summation of Sin^2 and Cos^2 signals.

From the formula shown in Eq. (3), a constant DC voltage that is proportional to the amplitude of the sinusoidal signals can still be generated although there is variation on the amplitudes.

4. Design Implementation

The proposed method has been implemented in the LED regulation system. The amplitude of the sinusoidal signals will be tracked, ensuring that the generated DC voltage reduces when the amplitude increases and vice versa. Figure 6 shows the block diagram of the LED regulation system implemented using a 0.18um CMOS process. The process is chosen for this paper because it is an affordable and stable technology.

This process supports 5V and 3.3V power supply, which explained the maximum drop out current that can be limited by the supply voltage range, as described in Section 3.

In order to emulate the concept in Eq. (3), a few analog multiplier blocks have been added to the system. The purpose of the analog multiplier is to achieve a transfer function as shown in Eq. (4) [19**,** 20]. If the input signals of V_x is equalled to V_y, then a squared function can be achieved.

$$V_o = V_x V_y \tag{4}$$

Any typical design of a good amplifier can be used as a voltage reference [21-22]. For accuracy, the bandgap circuit used [23] needs to have low variation as it is generating the reference voltage, and the same goes for variation control which is needed as the current reference circuit as well [24].

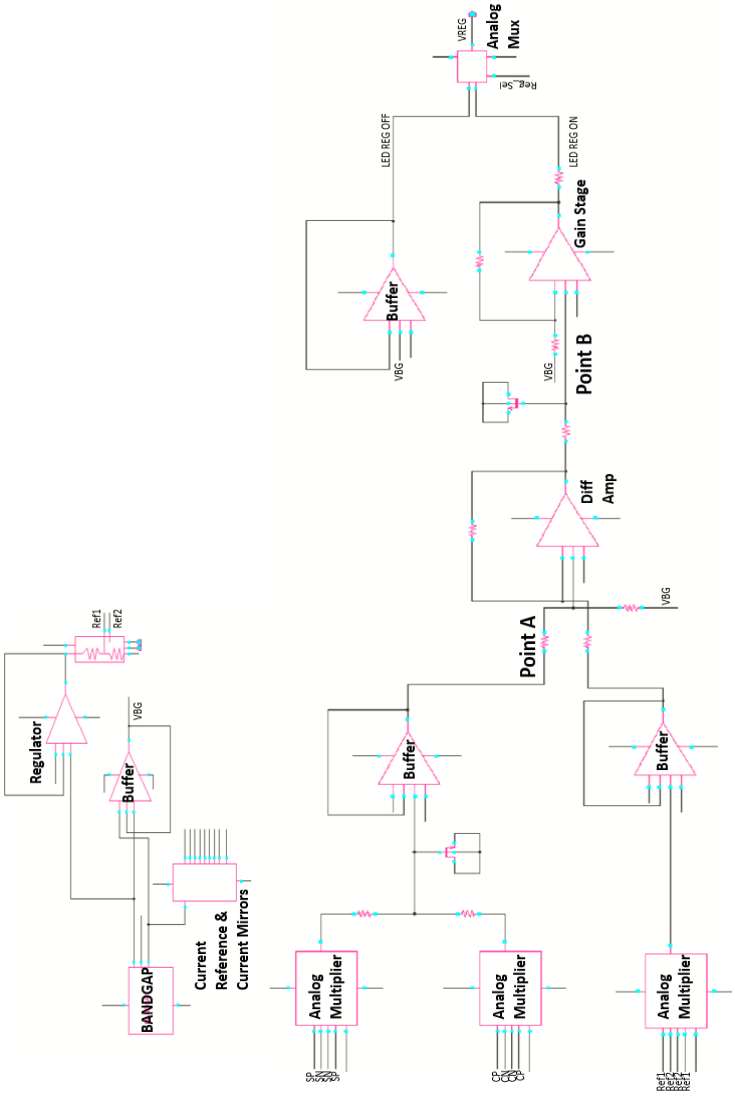

Fig. 6. Schematic block diagram of the proposed LED regulation block.

4.1. Design implementation for the proof of concept

From Fig. 6, the sinusoidal signals: SP with SN and CP with CN, are fed into two analog multipliers respectively. These signals are doubled the frequency of the input with a phase difference of 180 degrees apart. Summing the two output signals using a resistor divider from both the analog multipliers from SP with SN and CP with CN will generate a DC level, which tracks the amplitude of these four signals. Simulation output for these signals is shown in Fig. 7. The SP and SN go through the 1st analog multiplier and the output after this block is shown as SPnSN which is double the frequency of the original SP and SN whereas CP and CN go through the 2nd analog multiplier block and generates CPnCN. These two combined signals of SPnSN and CPnCN are two sinusoidal signals, which are double the frequency of the original SP, SN, CP and CN signals and are 180 degrees apart. Summing these two signals using the resistor string generates a DC signal shown as MultAve in Fig. 7. This proves that the proposed method fulfils Eq. (3). This implementation further verifies the proposed models shown in Figs. 3 to 5.

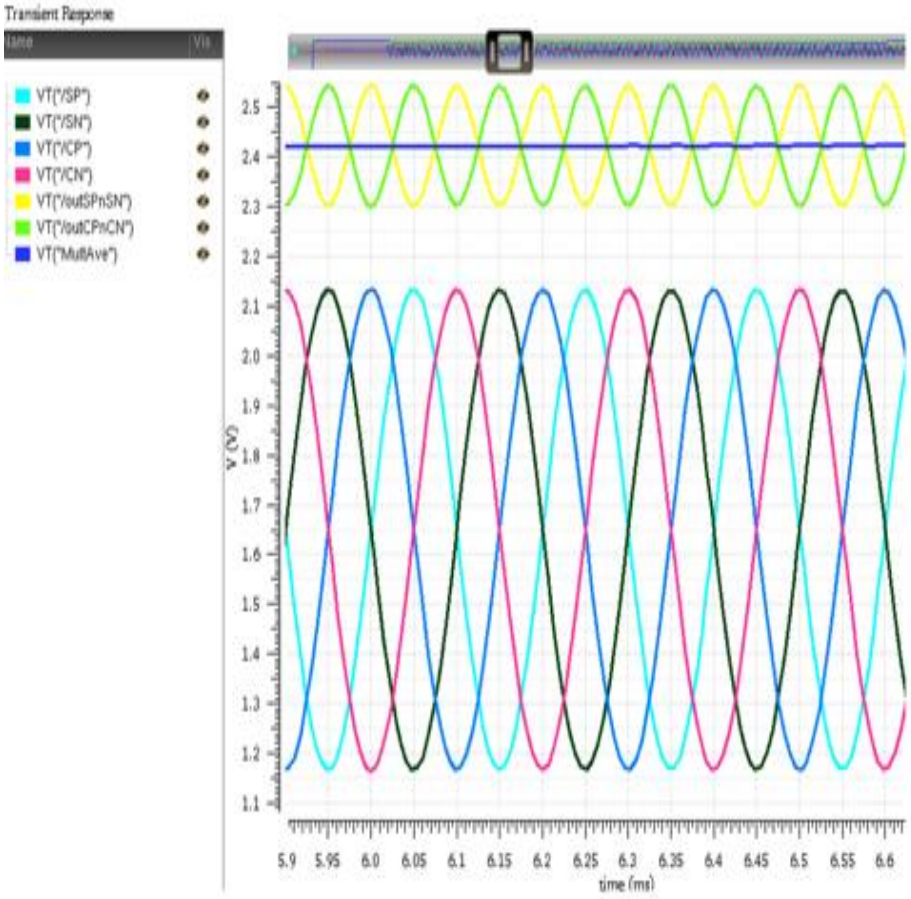

Fig 7. Input signals and output of the analog multiplier blocks to generate a DC voltage that tracks the amplitude of the input signals.

4.2. Design implementation to solve variation

A third analog multiplier with input of two DC voltages is added to generate a reference DC voltage. The reference voltage will be able to track the DC voltage level of the output from the previous two analog multipliers, creating a differential signal that will eliminate the variation that exist in this DC voltage level. Typically, the DC voltage level can vary with changes in process or temperature. Thus, going through a non-inverting amplifier, the residue of DC level caused by the variation of the process and temperature can be cancelled out. The differential signal, which only contains the information of the SP, SN, CP and CN can then be tied to a desired voltage level. The output of the non-inverting amplifier is connected to a simple RC filter to remove any small rippling due to any imperfection from the input signals.

Referred to Fig. 6, signals at Point A and Point B are taken to simulate for the temperature and process variation. Figure 8 shows the simulated output signals at Point A (top subplot) and Point B (bottom subplot). Simulated result at Point A showed that the signal is sensitive to the process and temperature, hence it is not suitable to be used to generate LED current. However, the simulated result at Point B showed that the signal is stable and not affected by the temperature and process variation at all. It is shown that the unwanted signals due to the temperature and process variation has been eliminated through the differential amplifier which is inserted between Point A and Point B. In addition to that, this signal can be used to bias the amplifier in the gain stage as well as to bias an intended starting voltage. This signal will be the source of voltage regulation block, V_{reg}.

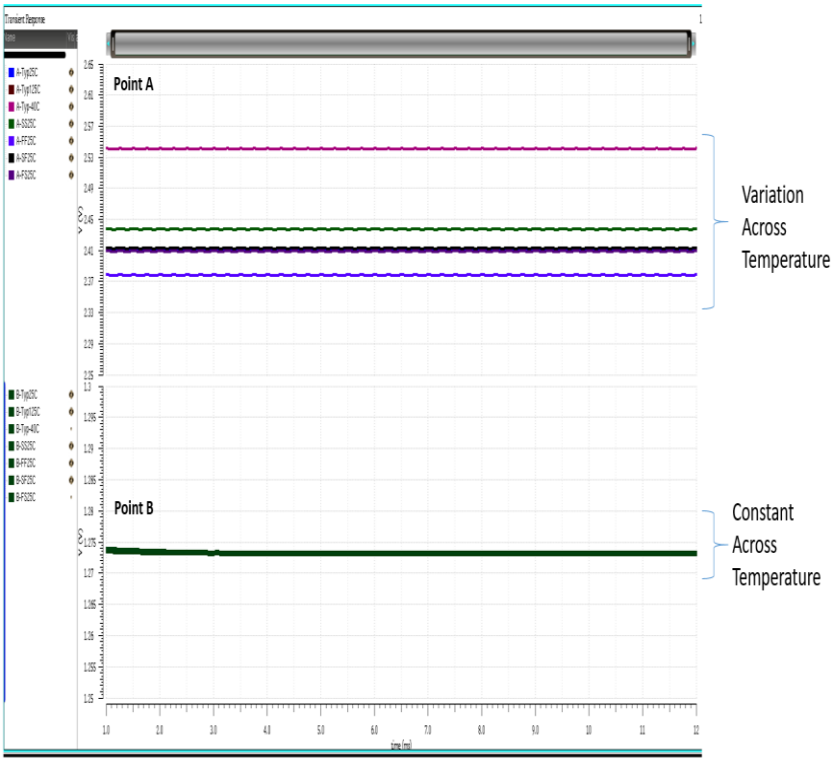

Fig. 8. Output of the signals at Point A and Point B as shown in Fig. 6.

In Fig. 6, the output stage is a gain stage where the sensitivity of the LED regulation will be based on its application. For example, amplification can be added to the signal at Point B to adjust the sensitivity of the detection and correction. This stage also provides the drive strength to drive the external circuitries. The output of this stage, V_{reg} will then be connected to external circuitry as shown in Fig. 2.

Figure 9 shows the simulation results of the whole LED Regulation system. A test bench is created to model a LED degradation feedback loop and to maintain the amplitude of the four sinusoidal signals. As shown, the LED current (middle subplot) increases to compensate for the modelled power loss of the LED. The top subplot shows the four sinusoidal signals with their amplitude consistently at the targeted values while the middle subplot shows the V_{reg} voltage, which is increasing to compensate for the LED power loss. The bottom subplot shows the LED current, which is proportional to the V_{reg} voltage. The simulation results also show that once the LED current reaches its maximum supported current, the amplitude of the sinusoidal signals will reduce due to the continuing modelling of LED degradation.

The starting point for the V_{reg} is chosen at 1.28V, which is a typical ASIC bandgap voltage. The NPN transistor chosen for this design has a typical V_{BE} of 0.65V with current value suitable for this application. These external parameters are fixed by the requirement of the design and also the parameters of the external components. In order to obtain a nominal LED current of 25mA, an external resistor valued at 25Ohm is chosen, based on Eq. (1). The maximum current or the voltage limit for this design is limited by the external components and voltage range. The VDD for this design is 3.3V and the forward voltage of the LED is around 1.2V at typical corners, thus the V_{reg} voltage should be around 2.1V maximally.

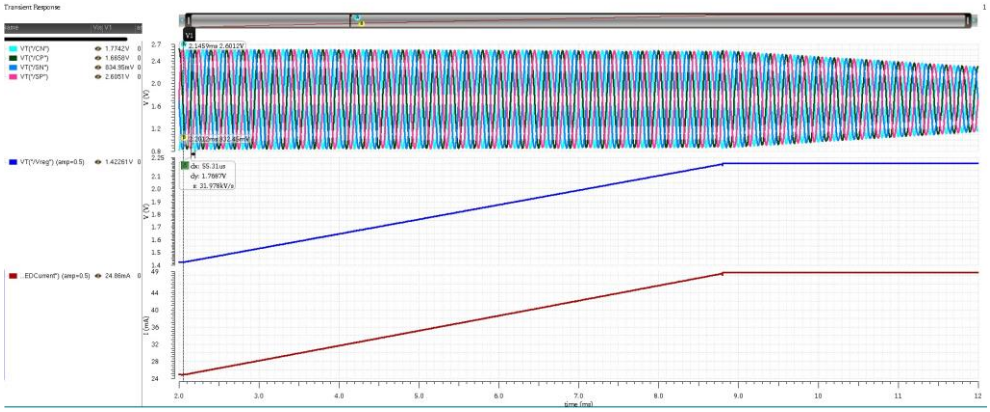

Fig. 9. Output of the sinusoidal signals SP, SN, CP and CN with consistent amplitude and increasing LED current.

5. Experimental Results

The proposed LED current regulation system was implemented and fabricated using a 0.18 µm CMOS process as shown in Fig. 1. The proposed LED current regulation block depicted in Fig. 6 has been included together with the Photodiode and Current to Voltage Conversion portrayed in Fig. 1. Figure 10 shows the fabricated layout of the LED regulation system while Fig. 11 is the die photograph of the LED Regulation Block.

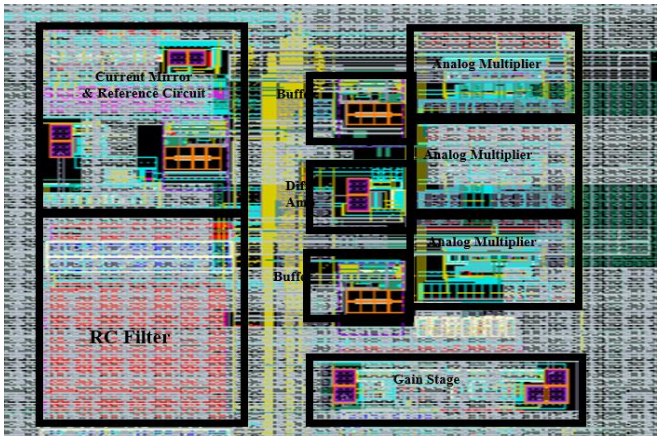

Fig. 10. Layout of the LED regulation system.

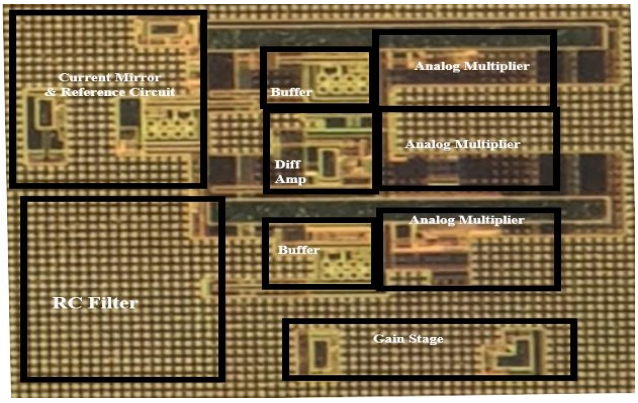

Fig. 11. Die photograph of the LED regulation block.

Figure 12 is the measured result from the four sinusoidal signals SP, SN CP and CN, the V_{reg} voltage and the LED current. The LED current was measured using a current probe. In the encoder system, the input to the system is generated from the photocurrent of a fabricated photodiode. The LED light distance to the photodiode sensor was increased by adjusting the test setup to model a degradation of light power albeit faster than the actual degradation in time domain in order to capture the effect from the oscilloscope. By increasing the distance from LED source to the photodiode, the optical power seen by the photodiode reduces, modelling an amplitude reduction of the signals. Without the proposed LED regulation method, the amplitude of the signals will drop. With the proposed method, when the distance of the light source to the photodiode increases, the Vreg voltage which is the output from the LED Regulation block, which is proportional to the LED current from Eqn. 1, increases. By boosting more current into the LED, the light power increases making the signal to the photo sensor increases. Similarly if the light power increases and can be modelled by making the distance of the light source to the photo sensor nearer, the LED current will reduce. The results shown in Fig. 12 of the proposed method shows the amplitude of the signals are maintained to its design voltage of $1.8V_{pp}$ by compensating the loss of light power or intensity by increasing

the current through the LED. Once the threshold of the LED current was reached, the LED current no longer can increase and the Vpp of the signals starts degrading as seen in Fig. 12 when Vreg and LED current starts to saturate. The measured results in Fig. 12 matched closely to the simulation results.

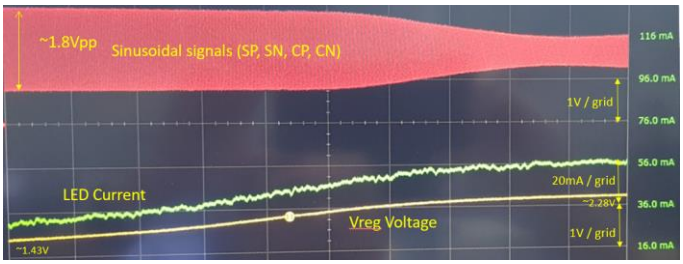

Fig. 12. Measured signals of the 4 sinusoidal, Vreg voltage and the LED current.

Table 1 summarizes the results from design simulation compared to the results from the die measurement with and without the LED regulation system. The design is subjected to a control temperature sweep at its intended temperature using a thermostream machine when the measurement is recorded. Based on Table 1, it is shown that with the proposed method in this paper with the LED Regulation block turned ON, the LED current changes (reduces or increases) and this compensated the V_{pp} values. However, without the proposed method (LED Regulation OFF), the V_{pp} and LED current increased comparatively. The design is also measured across temperatures to verify that the proposed method is applicable to temperature variation. This prove that the LED current regulation system is able to regulate the LED current to compensate for the degradation and loss of LED power.

Table 1. Summary of design simulation results and measurement results.

		Temperature (°C)		
		-40	**25**	**125**
Design Simulation Results	**LED Regulation OFF**			
	Sinusoidal Vpp	**1.67 Vpp**	**1.85 Vpp**	**2.13 Vpp**
	LED Current	**22.54 mA**	**25.55 mA**	**30.81 mA**
	LED Regulation ON			
	Sinusoidal Vpp	**1.76 Vpp**	**1.76 Vpp**	**1.82 Vpp**
	LED Current	**23.67 mA**	**24.91 mA**	**27.05 mA**
Measurement Results	**LED Regulation OFF**			
	Sinusoidal Vpp	**1.68 Vpp**	**1.789 Vpp**	**2.01 Vpp**
	LED Current	**22.91 mA**	**24.3 mA**	**29.40 mA**
	LED Regulation ON			
	Sinusoidal Vpp	**1.79 Vpp**	**1.8 Vpp**	**1.81 Vpp**
	LED Current	**23.8 mA**	**24.4 mA**	**28.8 mA**

6. Conclusions

In this paper, the concept and implementation of compensating the amplitude of the sinusoidal signals in an optical encoder using LED current regulation is presented with model, implementation and measurement results. The model uses a simple trigonometric formula to prove the concept. The proposed analog design implementation utilizing analog multipliers and amplifiers to fulfil the trigonometric formula. The implementation posed some challenges in term of process, temperature and voltage variation. The outcome shows that the system is

able to regulate the LED current to compensate for the degradation and loss of LED power that affects the amplitude of the signal used. From the simulation data, the nominal current of ~25mA is obtained which is closed to the calculated value. With the LED regulation off; it is shown that the amplitude of the sinusoidal signal varies with temperature and is in the range of $1.67V_{pp}$ to $2.13V_{pp}$. After turning on the compensation method, the amplitude of the signals is maintained at the design value of $\sim 1.8V_{pp}$ via compensating the LED current, maintaining the brightness or optical power. Other than temperature, this real time amplitude adjustment using the LED is also able to compensate the degradation of LED over lifetime, mechanical tolerance and also unwanted particles such as dust or contaminant to a certain extend. The amplitude of the signals is maintained regardless of LED power until the maximum allowable LED current. The design is also measured across temperature to verify that the proposed method is applicable to temperature variation. Hence, the design provides the flexibility of changes to different types of LED with some external component mainly the resistor Re. The implementation is based solely on analog blocks to eliminate the use of digital blocks, and this is suitable for a real time, low cost and less complex optical encoder.

Nomenclatures

C_b	Capacitor at base of NPN transistor
I_b	Base current
I_c	Collector current
I_e	Emitter current
I_{LED}	Current going through the LED
mA	Miliampere
R_b	Resistor at base of NPN transistor
R_e	Resistor at emitter of NPN transistor
V_{be}	Voltage difference between Base of NPN transistor and emitter of NPN transistor
$V_{CE(sat)}$	Saturation voltage of the NPN transistor
V_f	Forward voltage of the LED
V_{reg}	Regulated voltage by the LED Regulation block biasing the NPN transistor

Abbreviations

ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
DSP	Digital Signal Processing
LED	Light Emitting Diode
NPN	Bipolar Transistor
PD	Photo diode
PWL	Piece Wise Linear
Vpp	Peak to Peak Voltage

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Appendix A

Simulation Test Bench

A simulation test bench to model a close loop system of the LED degradation is used in Section 4.4 to obtain the simulation results. The close-loop system modelling of the test bench is shown in Fig. A-1.

Test bench description

The LED Regulation close loop system with modelling of LED degradation is shown in Fig. A-1. The design block under test is the LED Regulation Block and its corresponding external components. The NPN SPICE model file can be taken from the website of the component's supplier or any generic NPN models though it might not be so accurate.

The voltage source connected in series with the collector of the NPN is to include the forward voltage of the LED. Depending on the LED used and its Vf values, it will be a parameter that will contribute to the head room of the design. The voltage source of (A) is just a voltage source that has no values in voltage as it is used as just a reference for the Current Controlled Voltage Source in (B). This component is to convert the current going through the NPN transistor which is also the current going

through the LED into voltage. A Voltage Controlled Voltage source (C) is added with gain in the source to make any LED current used in the system to be 1V to mimic a 0 hour (LED at initial time) operation. Example of the values of gain needed is when the design of the system starts at 25mA with the LED at optimal operation, the gain of 40 in the source is included to get 1V. Another voltage controlled voltage source at (E) is included where a Piecewise Linear Voltage source (D) is connected at the Negative port of (E) to reduce the voltage generated and modelling a degradation of the LED or any effect of the LED that is required. Next, a delay block is added to model of any delay that is required in the close loop system. In general, it is not used to model the light, as light theoretically travel fast thus will not cause any delay. Next, four sinusoidal voltage source with same amplitude and frequency but with difference phase is generated to model the 4 sinusoidal signals 90 degrees apart from each other of the encoder system. For this simulation and design, the amplitude is 900mV. Vcomp block is a VerilogA block that multiplies each individual sinusoidal signals with the voltage from (E). The last component used is a DC voltage source of (G) to include back the midpoint voltage of the 4 sinusoidal waveforms and in this design is 1.65V correspond to Power Source 3.3V divided by 2.

At the start of the simulation, input to the Vcomp is the sinusoidal signal and voltage from (E) which starts at 1V. The PWL voltage starts to go up where the total voltage at (E) will start to go down - as (D) is connected to negative port of (E). With the lowering of voltage at Vcomp, the sinusoidal signal generated will reduce in amplitude. The LED Regulation block in the design will detect the change of amplitude thus boosting up the LED current. If the LED Regulation block are functioning, the voltage at (E) will maintain at 1V as the voltage degradation generated by (D) is compensated by the increase in LED current thus output at (C). This equilibrium state goes on until the LED current by the design is clipped and no longer able to increase thus the Vpp of the voltage will reduce.

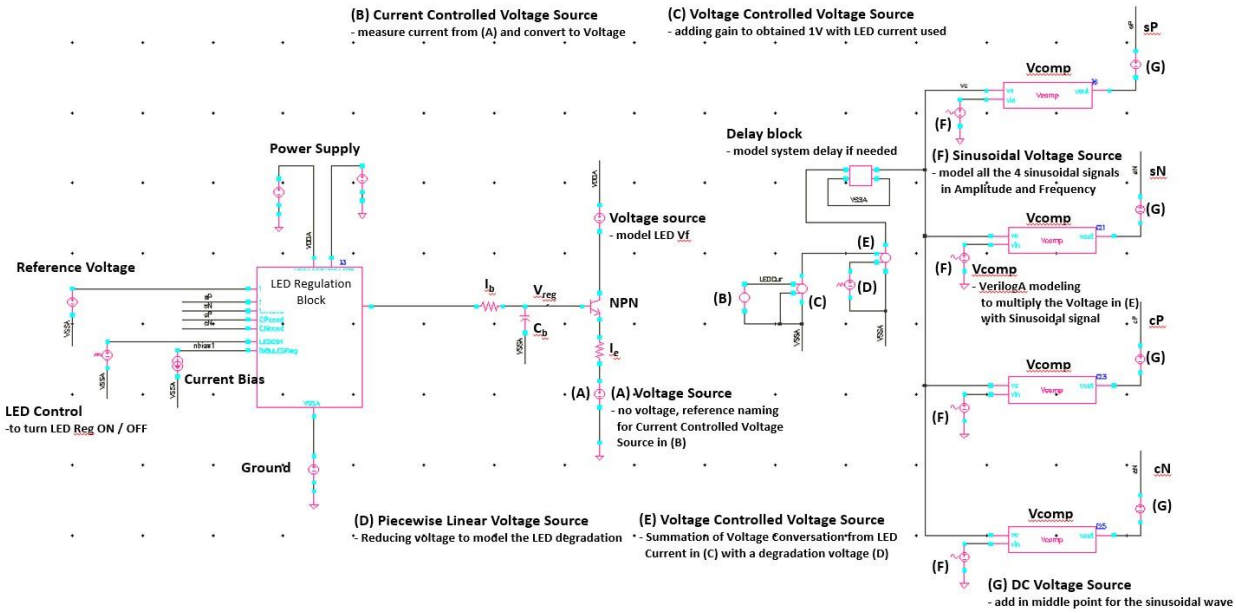

Fig. A-1. Schematic of test bench used in Circuit Simulation to model a close loop feedback of the LED Regulation path with degradation.