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EFFICIENT DESIGN AND IMPLEMENTATION OF THE REALTIME MULTI TYPES DIGITAL MODULATIONS SYSTEM BASED FPGA

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Abstract

Wherever there has been a real need for an optimum digital communications system that can switch between multiple modulation types as needed. This paper proposes a novel and optimum new design and implementation for multi types of digital modulation techniques in one compact system. A Field-Programmable Gate Array (FPGA) (Spartan 3E) development board associated with Very High-Speed Hardware Description Language (VHDL) and Xilinx ISE 14.7 was used for the hardware implementation of the proposed system. The suggested design of this system realized eleven types of modulation types with a minimum required memory size and the high flexibility of switching between the different types of digital modulation and the originality from the past works. The Lookup Table (LUT) with only 256 samples (memory array) for carrier wave generation was used with assistant digital to analog (DAC) board which was designed for this purpose to generate the analog output wave for all the above eleven types of digital modulation in real-time.

Keywords: Architecture design, Digital communication, Digital modulations, FPGA, Real-time implementation, VHDL

1. Introduction

Digital modulation techniques are essential in digital communication systems, such as satellite communication systems, telephone systems, and mobile cellular communication systems [1]. To select the suitable modulation technique, many factors must be considered: bandwidth efficiency, high power efficiency, low bit error probability, low sensitivity of multipath fading, low cost, and ease of implementation [2]. Generally, the modulation schemes are categorized into two main classes: non-constant and constant envelopes, as shown in Fig. 1 [1]. The constant envelope type is generally suitable for communication systems that must operate in the high power efficiency of the transmitter to achieve maximum signal-to-noise ratio in the receiver and produce minimum bit error rate (such as FSK and PSK). The non-constant envelope design, such as ASK and QAM, are generally not efficient for systems with maximum power efficiency in the transmitter and minimum bit error rate in the receiver. However, QAM has been widely utilized in modems networks, such as computer modems [2, 3]. Digital modulation systems are usually represented in time domain waveform, phase or constellation diagram, and power spectrum density PSD as an illustration in Fig. 2 [2]. The bandwidth of the signal in the communications channel is based on the symbol rate [4, 5]. The frequency bitstream is the bit rate. While the bit rate divided by the number of bits is the symbol rate submitted for each symbol s, shown in Eq. (1) [5].

$$\text{Symbol rate} = \frac{\text{bit rate}}{\text{the number of bits transmitted with each symbol}} \quad (1)$$

High performance of hardware systems and flexibility in design and implementation is required for the development of communication system. In digital communication systems, the data that needs to be transferred to the destination side need free-error and should make effectively utilization of the channel bandwidth available. A Field Programmable Gate Array (FPGA) is a programmable logic device that includes configurable logic blocks (CLBs), input-output blocks (IOs), functionality, and interconnection that can be reconfigurable after manufacturing [6]. This technology contains the translation of an algorithm from a high-level to hardware language like Verilog or VHDL description language [7, 8].

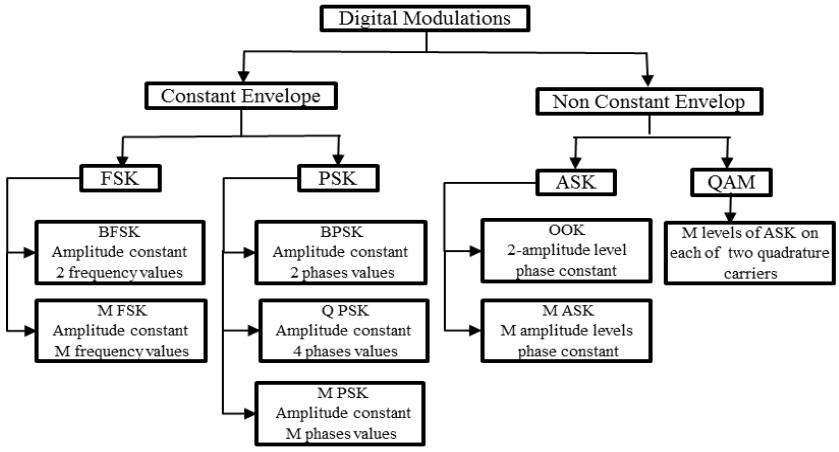


Fig. 1. Digital modulation classification diagram.

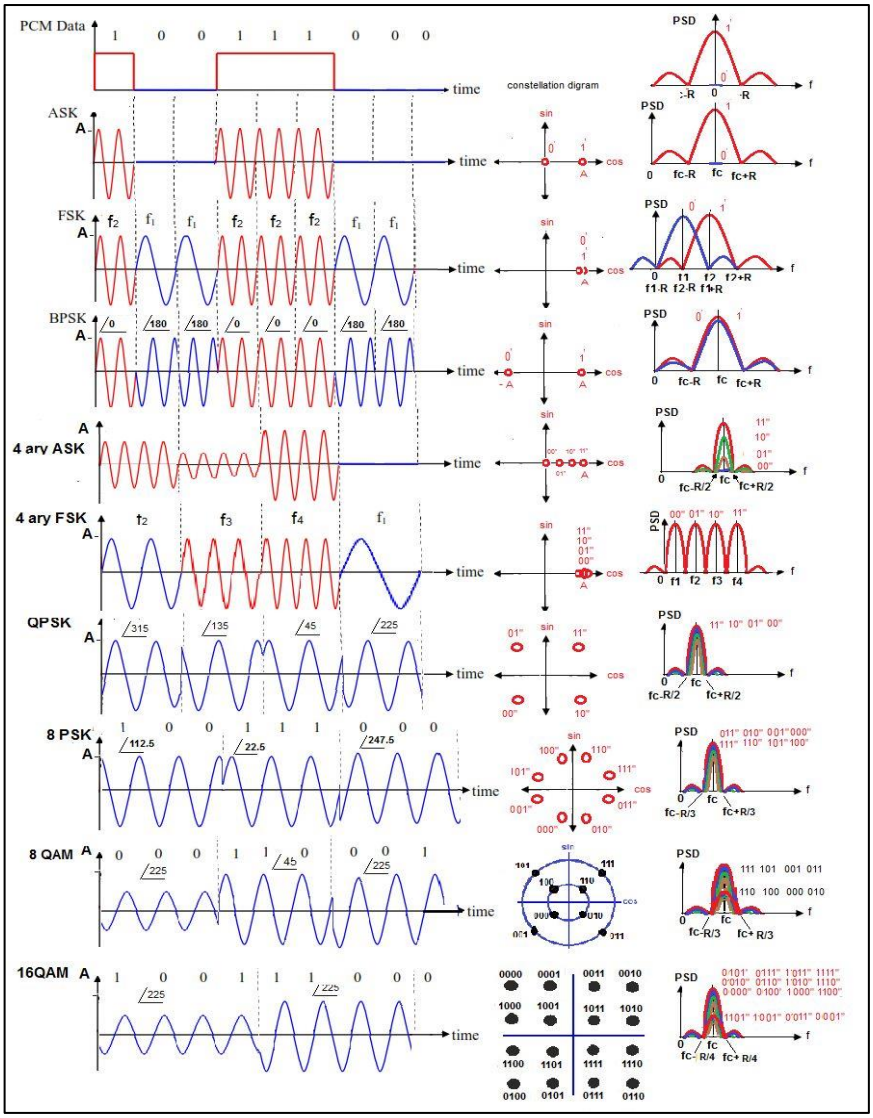


Fig. 2. Waveform, constellation diagram and PSD for the digital modulation systems.

The paper aims to design optimum multi types of real-time digital modulation (ASK, FSK, PSK, DPSK, QPSK, DQPSK, 8 PSK, 8 QAM, 16 QAM, 4-ARRAY ASK, and 4-ARRAY FSK) in one system based FPGA, with optimizations in implementation.

The paper is organized as follows. In Section 2, the related works are briefly explained. In Section 3, primary considerations in designing a digital modulation system with VHDL are given in detail. The proposed design of the optimum digital modulation system is described in Section 4. The simulation and implementation are emphasized and evaluated in Sections 5 and 6. Finally, conclusions and future works are mentioned in Section 7.

2. Related Works

This section will declare a review of the recent literature published in the related field: Previously, a digital modulation system (ASK, FSK, and PSK) by a new method was designed and implemented on FPGA spartan3E using VHDL with Xilinx ISE 8.2i [9].

Sinha and Lotia [10] presented BASK, BPSK, BFSK, and QPSK digital modulators. Modulators were designed using (VHDL) language and realized on high-speed FPGA. BER of BASK was higher than BER of BPSK. Besides, the BPSK modulation technique was shown to have a BER low than the BFSK modulation technique. The functionality of these digital modulators will be demonstrated through simulations using Xilinx 13.2.

Shahana et al. [11] realized selectable M-PSK modulators (BPSK, QPSK, 8PSK, 16PSK) on a single Spartan-3AN FPGA using Xilinx System Generator and VHDL language.

Al Safi and Bazuin [12] investigated a new design for hardware implementation of Binary PSK (BPSK) and Quadrature PSK (QPSK) techniques in FPGA using VHDL language.

Jamm et al. [13] investigated the design and implemented the digital modulation system using a system generator with Xilinx ISE 14.7 design suite. The FPGA implementation of digital modulation techniques (BASK-BFSK-BPSK-DPSK) has been run on the Spartan 3E board. These digital modulators were built in the Xilinx System generator and were later synthesized into FPGA board Nexys 2 Spartan 3E.

Al Safi and Bazuin [14] proposed an FPGA-based implementation of different kinds of ASK (OOK, BASK, 4ASK) and QAM (4QAM, 16QAM), using VHDL and ZYBO board (Zynq-7000) target devices. Carrier sine wave generation is done by a 24-bit phase accumulator and Look-Up Table (LUT).

Muthalagu et al. [15] presented design and implementation optimized QPSK and OQPSK modulation techniques on FPGA (Spartan-3E) with VHDL Language and compared with conventional QPSK and OQPSK design.

Rao et al. [16] suggested implementing three modulation techniques (BPSK DQPSK, DSSS) using Xilinx ISE 14.5 with VHDL. The device used is VIRTEX4. IOB utilization is found to be 31% in BPSK and is reduced to 11% in DSSS Modulator, which is further reduced to 7% in DQPSK. Power consumed is about 0.081w for three types of modulations.

Mohammed and Abdullah [17] applied analog and digital modulation systems on FPGA such as BASK, BFSK, BPSK, DPSK, AM, FM, and PM on ARTIX 7 FPGA using a system generator with Vivado 2017.4. The conclusion from this work proved that the numbers of resources in FPGA of digital modulation system design compared for analog modulation design.

3. Primary Consideration in Designing the Digital Modulation System with VHDL

VHDL is a hardware description language that describes the behavior of a circuit or system. It is intended for circuit synthesis and circuit simulation [18, 19]. This

section will discuss the basic building block of digital modulation system carrier wave generation (sine wave), bit rate, and baud rate generation.

3.1. Carrier Wave Generation

In modulation techniques, carrier wave generation is a significant proposed wave generation based on LUT (small memory), generates an analog waveform that stores digital samples of a sinusoidal waveform. A LUT is a set of memory locations that contain some pre-calculated value, as shown in Eq. (2) [20]:

$$ROM\ (i) = A * sin((2\pi * n)/M) \quad (2)$$

where the memory word length is used for LUT. varying M produces a sinusoid of different frequencies. To keep the output on the positive side between (0-5) volts, Eq. (2) needs to be modified as Eq. (3) [1]:

$$ROM(n) = A/2 + A/2 * sin((2\pi * n)/M) \quad (3)$$

In this paper, one ROM is calculated with M=256 samples. The first sample's value of generated sine wave starts with value 80 hex and increases to FF hex at sample 63, then decreases to 80hex at sample 127, then drops to 00hex at sample 191. Lastly, it expands reach 80 hex at sample 255. So, the same LUT with 256 samples (memory array) for carrier wave generation will generate the output wave for all types of digital modulation.

3.2. Symbol rate and Bit Rate Generation

For hardware implementation on FPGA, the synchronization is represented the heart design. Some calculations must be solved to get the exact modulation without any drift or loss in information such as time of bit, carrier, carrier time clock, several source clocks as shown in Eqs. (4), (5), and (6) [1]. The configuration with target device FPGA Spartan 3E type xc3s500efg320-4 is done. The chip's frequency is 50 MHz (the time of each clock is 20 nsec). The number of source clocks depending on this frequency for a different type of baud rate is calculated as shown in Table 1. Baud rate (24414.06) had been selected, which is considered the suitable choice for realization and implementation in the proposed optimum system:

$$\text{T. Bit} = \text{T. Carrier} = \frac{1}{\text{frequency of baud rate}} \quad (4)$$

$$\text{T. Clock of Carrier} = \frac{1}{256 * \text{frequency of baud rate}} \quad (5)$$

$$\text{No. of Source Clock} = \frac{\text{T.Clock of Carrier}}{\text{T.of Source Clock}} \quad (6)$$

Table 1. Carrier frequency, baud rate, bit rate computing.

Baud Rate	T bit (μsec)	T CLK of Carrier (nsec)	No. of Source CLK
300	3333.34	13020.83	640
600	1666.67	6510.41	320
1200	833.34	3255.2	160
2400	416.67	1627.6	80
4800	208.34	813.8	40
9600	104.16	406.9	20

4. Research Methodology of the Proposed Digital Modulation System Design

This section will discuss the proposed optimum design of the digital modulations system using Xilinx ISE 14.7 based on the VHDL. To explain the system operation, the whole system will be divided into three subsystems:

4.1. Digital modulation design one

The suitable modulations of the first proposed part are ASK, FSK, BPSK, and DPSK, as shown in Fig. 3. The basic building diagram consists of source clock (CLK), Start (ST), data input (DIN), and select (SEL) signals as inputs of the system. (Data out) signal as the output of the system. The block (Bit rate generation) is used for synchronization and produces CLK1, CLK2, and CLK3 from the source CLK signal. CLK2 is half the frequency of CLK1. CLK2 is the synchronization for each sample from one cycle of the carrier signal in BASK, BPSK, DPSK, and BFSK when the B1 signal movement is zero. CLK1 is the synchronization for each sample from one cycle of the carrier signal in BFSK when the B1 signal equals one to two carrier cycles for the last state, as shown in Table 1. While CLK3, which represents the input to the baud rate generation block, is the bit rate for the system. The block (baud rate generation) operates as capturing one bit from input data DIN each time to out B1 and BX1. XOR produces BX1 between B1 and DIN to use for DPSK. Lastly, the modulator can be chosen depending on SEL (2 bits) a, shown in Table 2, which illustrates the system design operation.

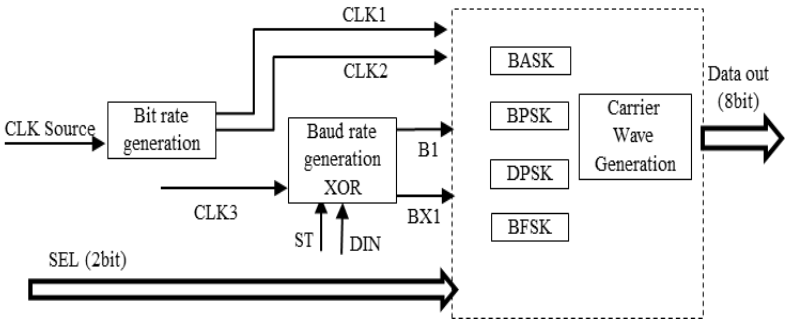


Fig. 3. Digital modulation system design one.

Table 2. Digital modulation system design one operation.

SEL	Type	DIN	Type of CLK	No. Samples	State (Carrier Wave Generation)
00	ASK	0 (B1)	CLK2	256	ADD[0]
		1(B1)	CLK2	256	ADD[0] TO ADD[255]
01	PSK	0(B1)	CLK2	256	ADD[0] TO ADD[255]
		1(B1)	CLK2	256	ADD[128] TO ADD[255] ADD[0] TO ADD[127]
10	DPSK	0(BX1)	CLK2	256	ADD[0] TO ADD[255]
		1(BX1)	CLK2	256	ADD[128] TO ADD[255] ADD[0] TO ADD[127]
11	FSK	0(B1)	CLK2	256	ADD[0] TO ADD[255]
		1(B1)	CLK1	512	ADD[0] TO ADD[255] ADD[0] TO ADD[255]

4.2. Digital modulation design two

The proposed second modulator design is suitable for 4-array ASK, 4-array FSK, QPSK, and DQPSK modulation, as shown in Fig. 4. Baud rate generation 2 (capturing 2bit) will be used; output B2 and Bx2 data equal two bits of input data DIN (1 bit). Block bit rate generation produces CLK1, CLK2, CLK3, and CLK4 for synchronization. In this design, some logical operations (shift right and offset) have been used for the same carrier to generate the exact optimum digital modulation system. Table 3 shows codes, SEL (2bits), and start samples of the page for QPSK and DQPSK. The system design operation for 4-array FSK and 4-array ASK and SEL (2 bit) are shown in Table 4.

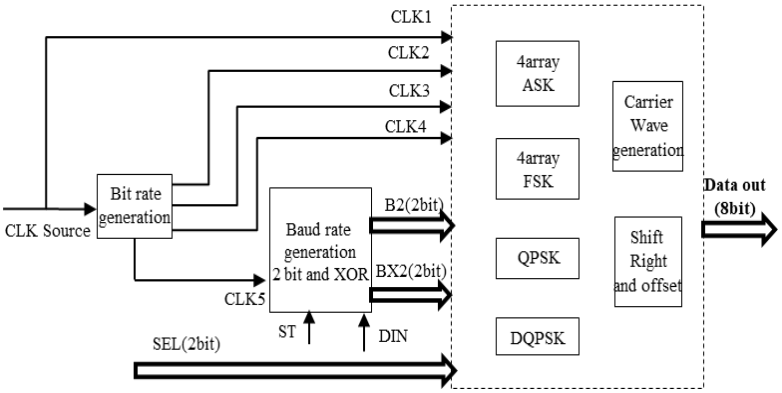


Fig. 4. Digital modulation system design two.

4.3. Digital Modulation Design Three

Figure 5 displays the third proposed subsystem design using baud rate generation 3 (Capturing 3 bit), suitable for 8PSK and 8QAM modulations, and baud rate generation 4 (capturing 4 bit) for 16QAM modulation with 256 samples (memory array) for carrier wave generation, and logical operation (shift and offset) to give precise modulation. Depending on the SEL (2 bits), the type of modulation can be chosen. For 8PSK and 8QAM, three bits are enough for coding operation, but 16QAM needs 4 bits for the coding process. As a result, two baud rate generations (3 bits, 4 bits) are used in this design. Table 5 shows the code and sample of 8PSK, 8QAM, and 16QAM.

Table 3. Codes and samples for QPSK and DQPSK.

SEL	Type	Code 2 Bits	Phase (Degree)	Sample Start (carrier wave generation)
10	QPSK	11(B2)	45	ADD [128] TO ADD [255] ADD[0] TO ADD[127]
		01(B2)	135	ADD [96] TO ADD [255] ADD[0] TO ADD[95]
		00(B2)	225	ADD [160] TO ADD [255] ADD[0] TO ADD[159]
		10(B2)	315	ADD [32] TO ADD [255] ADD[0] TO ADD[31]
11	DQPSK	11(XB2)	45	ADD [128] TO ADD [255] ADD[0] TO ADD[127]
		01(BX2)	135	ADD [96] TO ADD [255]

		ADD[0] TO ADD[95]
00(BX2)	225	ADD [160] TO ADD [255] ADD[0] TO ADD[159]
10(BX2)	315	ADD [32] TO ADD [255] ADD[0] TO ADD[31]

Table 4. Codes and samples for 4-array FSK and 4-array ASK.

SEL	Type	Bit (B2)	Type of CLK	State	No. of cycle	Amplitude
01	4-FSK	00	CLK4	ADD[0] TO ADD[255]	1(256 samples)	full
		01	CLK3	ADD[0] TO ADD[255]	2(512 samples)	full
		10	CLK2	ADD[0] TO ADD[255]	3(768 samples)	full
		11	CLK1	ADD[0] TO ADD[255]	4(1024 samples)	full
00	4-ASK	00	CLK4	ADD[0]	1(256 samples)	zero
		01	CLK4	ADD[0] TO ADD[255]	1(256 samples)	Divide by 4
		10	CLK4	ADD[0] TO ADD[255]	1(256 samples)	Divide by 2
		11	CLK4	ADD[0] TO ADD[255]	1(256 samples)	full

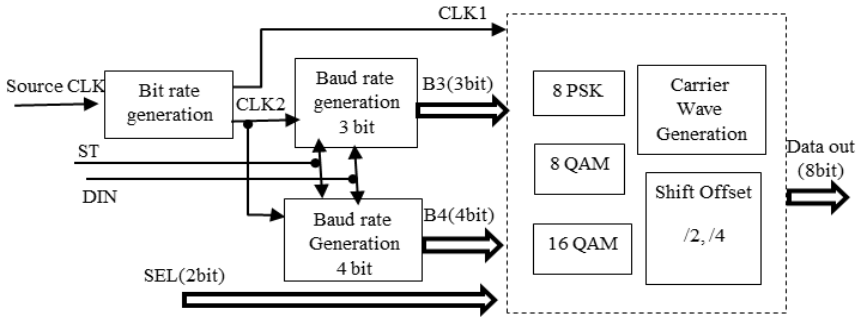


Fig. 5. Digital modulation system design three.

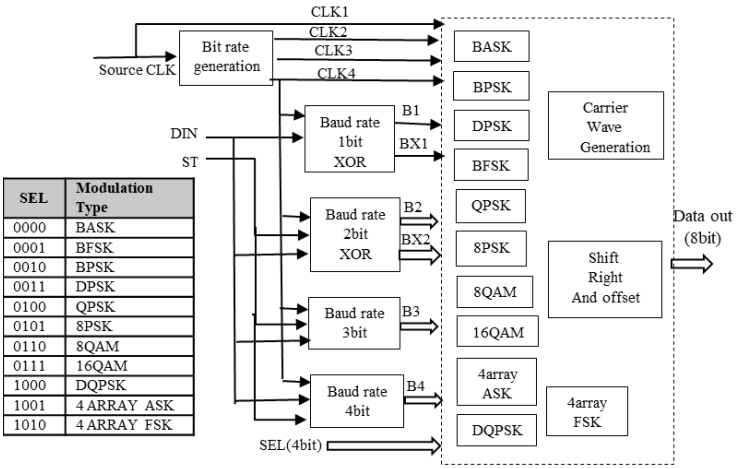
Table 5. Codes, samples, and operation of digital modulation design three.

Sel	Type	Code Bits(B3,B4)	Phase	Amp	No. Sample Start (State)
00	8_PSK	000	22.5		16(10H)
		001	67.5		48(30H)
		011	112.5		80(50H)
		010	157.5		112(70H)
		110	202.5		144(90H)
		111	247.5		176(B0H)
		101	292.5		208(D0H)
		100	337.5		240(F0H)
01	8_QAM	111	45	1.0	32(20H)
		110	45	0.33	32(20H)
		101	135	1.0	96(60H)

		100	135	0.33	96(60H)
		001	225	1.0	160(A0)
		000	225	0.33	160(A0)
		011	315	1.0	224(E0H)
		010	315	0.33	224(E0H)
10	16_QAM	1110	15	0.77	11(0B)
		1111	45	1.0	32(20H)
		1100	45	0.33	32(20H)
		1101	75	0.77	53(35H)
		0101	105	0.77	75(4BH)
		0111	135	1.0	96(60H)
		0100	135	0.33	96(60H)
		0110	165	0.77	117(75H)

4.4. The overall digital modulation system design

The optimum design of a digital modulation system contains different types of modulations such as (BASK, BPSK, DPSK, BFSK, QPSK, 8PSK, 8QAM, 16QAM, 4ARRAY ASK, and DQPSK) which combines the previously three system designs in one system. The overall optimum system design is shown in Fig. 6. This system includes DIN, ST, CLK source, and SEL signals as inputs. The data out signal is the output of this system. Based on the SEL (4 bits), the type of modulation at the output worked. The chosen bit rate and baud rate generation (1bit, 2 bits, 3 bits, and 4bits) are previously explained in designs one, two, and three (see subsections 4.1, 4.2, 4.3).



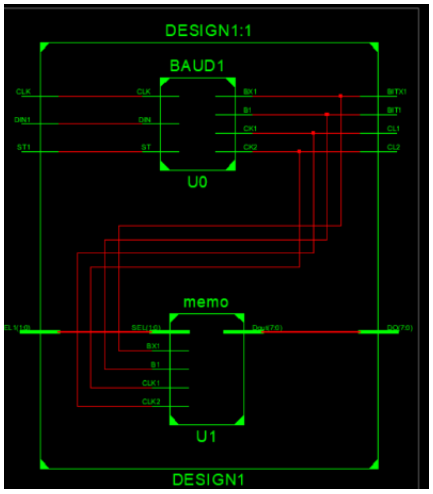
SEL	Modulation Type
0000	BASK
0001	BFSK
0010	BPSK
0011	DPSK
0100	QPSK
0101	8PSK
0110	8QAM
0111	16QAM
1000	DQPSK
1001	4 ARRAY ASK
1010	4 ARRAY FSK

Fig. 6. The overall digital modulation system design.

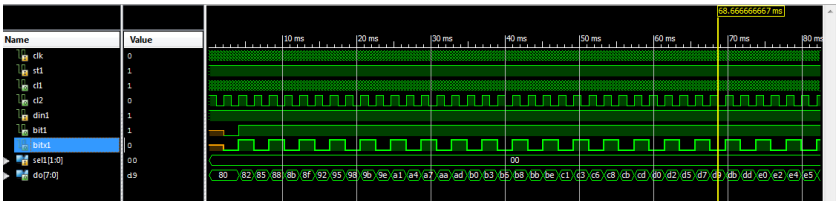
5. Simulation Results

The proposed digital modulation system design is modelled with VHDL and simulated using Xilinx ISE 14.7. Figure 7 declares the RTL schematic diagram and submitted system design simulation result one. From Fig. 7(b), it can be noted that the SEL signal equals 00. This means that the type of digital modulation displayed is the ASK modulation. Figure 7(c) and (d) show the simulation results of digital modulation system design two and design three, while the RTL schematic diagrams for these designs are similar but different in baud rate and memory contained based

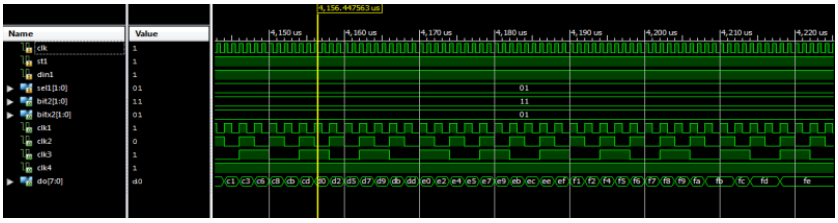
on the plan. The RTL schematic diagram and simulation results for the optimum overall digital modulation system are illustrated in Fig. 7(e) and (f). Table 6 shows the device utilization summary for each digital modulation system design.



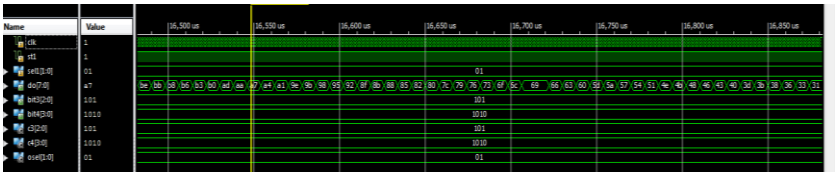
(a) RTL schematic diagram of the system design one.



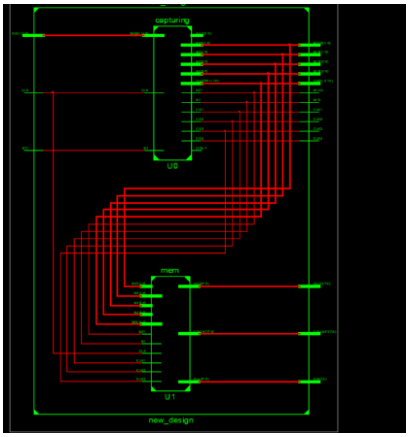
(b) Simulation result of the system design one.



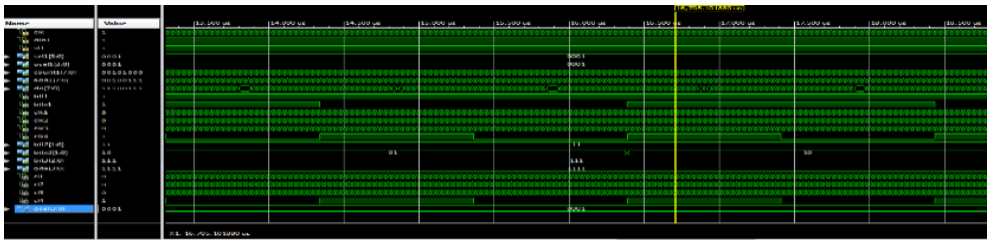
(c) Simulation result of the system design two.



(d) Simulation result of the system design three.



(e) RTL schematic diagram of the optimum overall digital modulation system design.



(f) Simulation result of the optimum overall digital modulation system design.

Fig. 7. RTL schematic diagrams and simulation results for all digital modulation system design.

Table 6. Device utilization summary.

Logic Utilization (Available)	***Design* 1**		***Design* 2**		***Design* 3**		***Overall***	
	Used	**Utilization**	**Used**	**Utilization**	**Used**	**Utilization**	**Used**	**Utilization**
Number of Slices (4,656)	183	3%	324	6%	264	5%	278	5%
Number of Slices FF (9,312)	118	1%	151	1%	101	1%	164	1%
Number of 4 input LUTs(9,312)	352	3%	621	6%	504	5%	534	5%
Number of bonded IOBs (232)	47	20%	47	20%	47	20%	47	20%
Number of G CLK (24)	3	12%	2	8%	3	12%	2	8%

Timing Report				
Min. Period/Max. Freq.	7.279 ns /137.379Mhz	9.54n /104.82Mhz	11.82 ns /84.57Mhz	6.388 ns /156.54Mhz
Min. input arrival time before CLK	5.98 ns	5.98 ns	5.006 ns	5.664 ns
Max. output required time after CLK	4.93 ns	4.948 ns	5.123 ns	4.914 ns

From Table 6, it can be noted that system design 1 consumes lesser resources because it is implemented for the introductory digital modulation type. In comparison, the system design two consumes more resources than system design three because it is implemented for more modulations. The optimum overall system design considers the efficient system design in terms of resources utilization.

Table 7 shows the comparison with the related works. This table shows that the proposed optimum system design is more efficient than other works in terms of the number of modulation types implemented in one system design and the utilization of resources.

6. Real Time Hardware Implementation of the Proposed Digital Modulation System

After finishing the final modifications on the designed system depending on the simulation results, the system design has been realized using the FPGA Spartan 3E (xc3s500efg320-4) board, 8 bits digital to analogue convertor board which has been designed and implemented, especially for this system, variable output power supply, dual channels oscilloscope, and PC with supplementary joints and cables are the overall hardware-implemented system as shown in Fig. 8. The analogue waveforms for all types of modulations have been gotten from the output of the DAC converter board, while the baseband digital input signal can be injected into the DIN signal on the FPGA board.

Table 7. Comparison with the related works.

REF. No	FPGA Type	Modulation Type	Tools	Utilization Area(4inputLUT)
[9]	Spartan 3E	BASK,BFSK,BPSK	Xilinx ISE 8.2I VHDL	35
[10]	-	BASK, BPSK, BFSK and QPSK	Xilinx ISE13.2 VHDL	-
[11]	Spartan-3AN	BPSK, QPSK, 8PSK, 16PSK	-	8852
[12]	-	BPSK, QPSK	VHDL	-
[13]	Nexys2 Spartan3e	BASK,BFSK,BPSK, DPSK	Xilinx ISE 14.7 System Generator	69 EXCEPTBASK

[14]	ZYBO board Zynq-7000	*OOK; BASK;4ASK,4QAM*,16QAM	VHDL	344
[15]	Spartan-3E	QPSK, OQPSK	Xilinx ISE 14.1 VHDL	1001
This work	Spartan-3E	(ASK, FSK, PSK, DPSK, QPSK, DQPSK, 8 PSK, 8 QAM, 16 QAM, 4-ARAY ASK, 4-ARAY FSK)	Xilinx ISE 14.7 VHDL	534

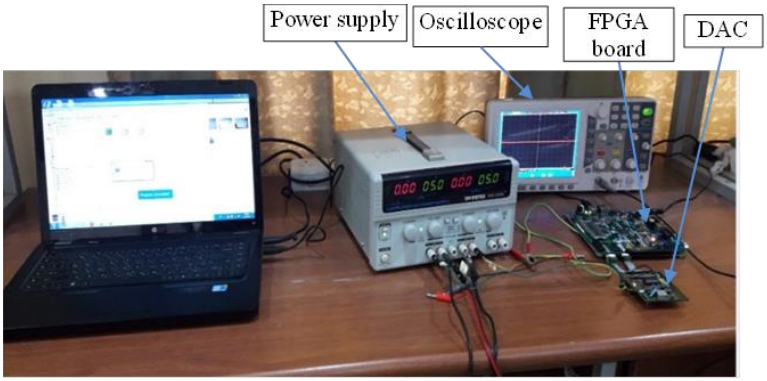


Fig. 8. Hardware implementation system for the proposed digital modulations system.

The implemented system has been tested under variance binary input streams. For all types of digital modulation assigned in this design, the output waveforms for these modulation types and the binary input stream are shown in Fig. 9. Finally, it can be concluded that the hardware results are exactly as expected and similar to the theory.

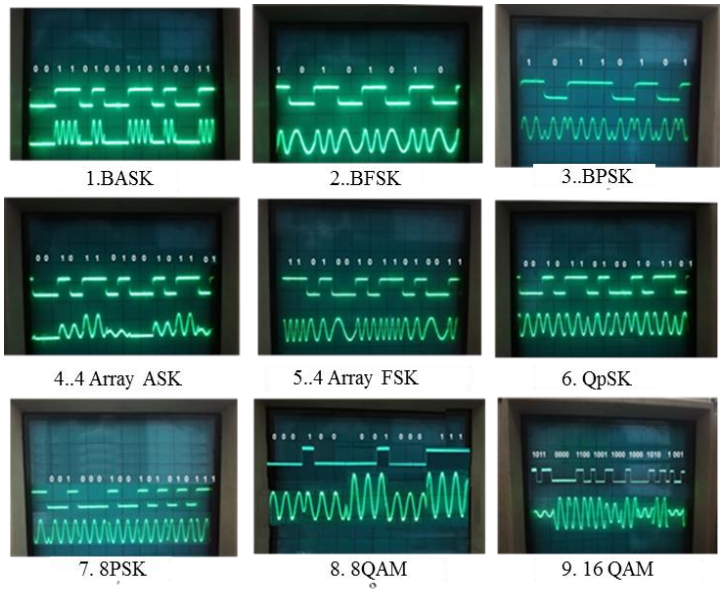


Fig. 9. Real time implementation of digital modulation system.

7. Conclusions

This work achieved a real time hardware implementation of the (ASK, FSK, PSK, DPSK, QPSK, DQPSK, 8 PSK, 8 QAM, 16 QAM, 4-ARRAY ASK, 4-ARRAY FSK) modulations types into one compact system, Knowing that, no previous works have been implemented all of these types of digital modulation signals into one system, in addition, this design realized the minimum area utilization (LUT) per modulation implemented type (534 /11), and minimum time of execution compared with the past similar works. The future works that may be suggested are the design to other kinds of digital modulations such as MSK, GMSK, and others that can be implemented based on FPGA. Also, the real-time demodulation system for multi-type of digital modulation can be designed and implemented. Lastly, the real-time modulation and demodulation systems can be implemented on another version or type of FPGA board with a higher frequency crystal to increase the provided bit rate. FPGA Spartan 6 (frequency crystal is 250 MHz).

Nomenclatures

A	The total amplitude (0-5) volts and in hexadecimal equals 255.
M	The number of samples for each sine waveform generation
n	The value varies from 0 to M-1 when the input clock frequency is fixed

Abbreviations

AM	Amplitude Modulation
Amp	Amplitude
ASK	Amplitude Shift Keying
BASK	Binary Amplitude Shift Keying
BER	Bit Error Rate
BFSK	Binary Frequency Shift Keying
BPSK	Binary Phase Shift Keying
CLBs	Configurable Logic Blocks
CLK	clock
DAC	Digital To Analog
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DSSS	Direct-Sequence Spread Spectrum
FM	Frequency Modulation
FPGA	Field-Programmable Gate Array
FSK	Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
IOBs	Input Output Blocks (IOs),
LUT	Look-up Table
MASK	Multiple Amplitude Shift Keying
MFSK	Multiple Frequency Shift Keying
MPSK	Multiple Phase Shift Keying
MHz	Mega Hertz
MSK	Minimum Shift Keying
nsec	Nano second
OOK	On–off keying
OQPSK	Offset Quadrature Phase Shift Keying

PC	Personal Computer
PSD	Power Spectrum Density
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
ROM	Read Only Memory
RTL	Register Transfer Language
T	Time
VHDL	Very High-Speed Hardware Description Language

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