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NON-VOLATILE BINARY CONTENT ADDRESSABLE MEMORY CELL WITH READ/WRITE SCHEME USING SPIN-POLARIZED CURRENT MODE MAGNETIC TUNNEL JUNCTION

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Abstract

This research work presents a non-volatile Content Addressable Memory (CAM) cell to store/hold1-bit data. The proposed scheme explores the non-volatile nature of the spin-polarized current mode operation of the Magnetic Tunnel Junction (MTJ) device and reports the MTJ model and its modelling parameters utilized in this work. Spin-polarized currents help in engineering the MTJs to exhibit either a high resistance (anti-parallel state) or a low resistance (parallel state) path by flipping its states (either parallel-to-antiparallel or antiparallel-to-parallel).The proposed circuit forms a voltage divider network comprised of MTJs connected in series. The different path resistances of MTJs, in different configurations, determine the logic value of 1-bit information at the storage node (V_O) of the proposed CAM cell. The logic values are evaluated for different configurations of MTJs to illustrate the operation of the proposed CAM cell. The proposed 1-bit CAM cell requires very low switching currents ($I_{CPtoAP} \approx 26.7$ µA and $I_{CAPtoP} \approx -19.4$ µA)to perform the write operation. Modelling of the proposed design has been done using Verilog-A and simulation results have been extensively verified using the SPICE simulator.

Keywords: Anti-parallel state, Content addressable memory, Magnetic tunnel junction, Parallel state, Write operation.

1. Introduction

Non-Volatile Memories (NVMs) have been revolutionizing the storage for high-performance computation. As the leakage power and the overall power consumption is increasing due to rigorous technology scaling, there is a dire need for the development of the next generation of NVMs. Moreover, the conventional (charge-based) memory technologies in CMOS are reaching their fundamental scaling limits which degrade their performances [1-3]. NVMs find their use in long-term information and data storage applications [4, 5]. As NVM uses a non-volatile element in its architecture, it retains data even after switching off the power supply. Recent developments in spin-dependent tunnelling (SDT), circuit elements like spin valve and MTJ are showing their potential impacts on the integrated circuit designs. This technology overcomes several issues of CMOS technology like scalability limits, device variability, and power dissipation [6, 7]. Magnetic properties of the MTJ have been explored in this paper to develop a non-volatile data storage node for a Content Addressable Memory (CAM) cell by tailoring spin-polarized current through MTJ layers [8-12].

In a CAM cell, a data word to be searched is provided to the search data register and the CAM performs its search operation in its entire stored data array simultaneously to find if that the data word being searched is stored anywhere in it or not. If the data being searched matches with a stored data, the CAM returns the storage address of the matched data [13-15]. CAM cell proves to be efficient in minimizing the search time taken to find a match within the stored datasheet. This is achieved by the parallel execution of the search operations [16-18]. Quick execution of search operation makes CAM find its application in high-speed search operations which also includes coding/decoding [19, 20], transmission and reception of data, and so on. However, the high operation speed of the CAM is obtained at the cost of increased area and power consumption [21-23].

Parallel match-line (*ML*) comparisons make CAM a power-hungry device for search operations limiting the CAM implementation for certain important applications where speed plays an important role in the overall performance. Apart from this, CAM, a solid-state memory drive, stores binary data that is accessed by its content. Data that is received at the data input (*DI*) node, is stored in the CAM memory cell during the write operation and sense amplifiers associated with a CAM cell help in reading the content stored in the CAM cell. Finally, a search operation is performed by a CAM to compare search data with the data stored and to return the address of the matched data stored in the data-bank. Thus, the architecture of a CAM cell is designed to execute read, write and search operations. Power consumption, operational speed and the chip area required by a CAM cell largely depend on the components and the circuit design used for implementing a CAM cell.

The different architectures of associative memories have been proposed for search engines and their related applications requiring low power dissipation and fast data retrieval [24-25]. These designs mainly include binary CAM in which the search operation is entirely based on 1s and 0s [3-26]; and Ternary Content-Addressable Memory (TCAM) which allows an additional third matching state of don't care (*X*), along with the binary states [27-29]. Conventional CMOS-based TCAMs store information in an SRAM block to provide fast and reliable search operations [27]. Although the SRAM-based TCAMs have been proposed for a

reliable search operation with high speed, it suffers from high standby power induced by the increased leakage current [27, 28]. As leakage power is a major concern for battery-operated devices, several designs have been proposed to optimize power dissipation in a CAM cell. For instance, a reconfigurable 6-transistor (6T) SRAM design [30] was proposed to improve system performance and efficiency. However, the high standby power dissipation due to the leakage current still remains an open research area, especially for the technology node below 45 nm [28, 31].

To address these challenges, recent studies have proposed to replace the SRAM block with a non-volatile element, such as memristors [27] or spintronic devices [24, 28, 29, 31], in the design so that it can retain the data even if the power supply is turned OFF during the idle mode, thus achieving a zero standby power. Additionally, these non-volatile devices are efficient in terms of chip area utilization [27, 32]. For these reasons, more recently, several magnetic tunnel junction (MTJ) based non-volatile ternary content-addressable memory cells have been proposed to realize zero standby power. However, these designs still suffer from high power consumption during search operations.

In the view of above, in this paper, we propose a novel MTJ-based CAM cell that is composed of 16 transistors (16Ts)and two MTJ devices. Owing to the MTJ, as there is no static current during search operations, the only dynamic current-based operation makes the design achieve ultra-low power consumption. In the proposed design, the differential MTJs with complementary states are exploited to store different states during write operations.

In this research work, we introduce a read/write scheme for a binary CAM cell using spin-polarized MTJs (Magnetic Tunnel Junction) in the proposed design. MTJ, a non-volatile element, can retain the data bit stored in the databank even if the power supply is turned off. Apart from being non-volatile, the proposed MTJ based write scheme possesses many other fertile properties of MTJ desired for memories and storage applications [26, 32]. Research work reported in this work falls in line with the work available in the literature [3]. In the view of above, this paper makes the following contributions:

- Read and write schemes using spin-polarized MTJs have been presented.
- The fertile properties of MTJs are explored in the proposed design to boost the performance of a CAM cell.
- Power, area, and speed comparisons are made with the similar architecture available in the literature.

The rest of the paper is organized as follows. Section 2 presents the modeling of the MTJ device utilized as a non-volatile element in the proposed write scheme for a CAM cell. The proposed circuit-level model of the write circuitry is mentioned in Section 3. Simulation results are discussed in Section 4. Finally, concluding remarks are provided in Section 5.

2. The non-volatile element of the proposed write scheme

MTJ is an imperative element of the write scheme reported in this work. This section presents a detailed discussion of the MTJ model that has been utilized to develop the design. Also, CAM architecture has been included in this section for understanding.

2.1. Modeling of magnetic tunnel junction

The investigation is going on Magnetic Tunnel Junction (MTJ) due to its fruitful dynamics and potential applications [33-37] .MTJ, a spin-based device characterized by non-volatility and scalability, is fully compatible with the present CMOS technology and has proved its significance and capabilities to provide lesser interconnects delay with low power consumption [32]. As compared to the current CMOS technology it possesses important features like scalability and durability which makes it an important candidate for applications in logic circuits such as magnetic adder and multiplexer and magnetic memories like CAM and magnetic RAM (MRAM).

MTJ nanopillar mainly consists of three thin films, namely, a thin oxide barrier (typically aluminum oxide (Al_2O_3 or MgO)) and two ferromagnetic (FM) layers of cobalt, iron, or nickel or full-Heusler alloy such as $Co_2FeAl_{0.5}Si_0$ [32, 38]. The MTJ device structure composed of CoFeB/MgO/CoFeB layers is utilized in this work. Figure 1 shows the cross-sectional view of the MTJ device along with the various layers with their dimensions. Plasma oxidized magnesium (MgO) acts as a tunnel barrier that is sandwiched between CoFeB layers. The fixed layer and free layer of the device are characterized by keeping the fixed layer (2.0 nm) wider as compared to the free layer (1.8 nm).

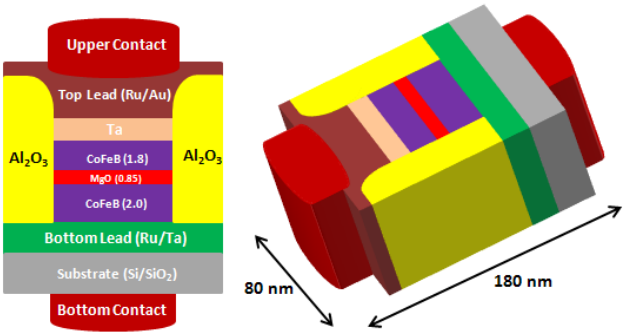

Fig. 1. Schematic of (a) MTJ structure composed of CoFeB/MgO/CoFeB. The thickness of the MTJ layers in nanometres are given in brackets. The pinned layer is separated by the free layer by a tunnelling MgO barrier (b) Lateral size of the MTJ device [32].

The magnetization direction of the wider layer, called a pinned layer (PL) is fixed, and the magnetization of another layer, called the free layer (FL) can be changed with respect to the PL. MTJ can be configured to exhibit either a low resistance path (parallel state) or a high resistance path (anti-parallel state) using spin-polarized switching current (see Fig. 2). Depending on the relative direction of the ferromagnet magnetizations, high or low resistance path is established through the MTJ. On passing a switching current (I_{PtoAP}) greater in magnitude than the device's switching threshold (I_{CPtoAP}), it establishes parallel-to-antiparallel alignment. Similarly, on passing a switching current (I_{APtoP}) greater in magnitude than the device's switching threshold (I_{CAPtoP}), it establishes antiparallel-to-parallel alignment of the free layer with respect to the fixed layer. Now, if the magnetization of the two FM layers is parallel, it offers a low resistance path and it is termed as logic '0' state. Similarly, if the magnetization of the two FM layers is antiparallel,

a high resistance path is created between the two FM layers and is termed as logic '1' state. Thus, the relative magnetization of the layers causes the storage of data, and the magnetizations remain unaffected even if the power supply is removed. This behavior of MTJ to store data in distinct states is utilized in non-volatile applications in memories as well as logic circuits [32, 38-40].

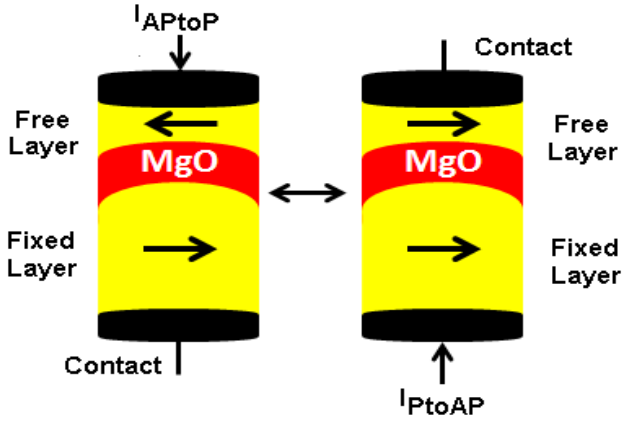

Fig. 2.Basic MTJ structure and its different configurations (parallel and anti-parallel states).

Conventionally, the magnetic field produced due to the flow of electrical current is utilized to flip the state of a magnetic device. However, with the technology scaling, the magnetic field strength required to flip the state is increased [3,11]. This substantial increase in the magnetic field strength demands increased write current and thus, contributes to high power dissipation. For this reason, magnetic switching of the spin-transfer torque (STT) based MTJ is exploited by passing an electrical spin-polarized current through the MTJ device to change the magnetic orientation of the free layer with respect to that of the pinned layer and vice versa [3, 32].

Thus, the MTJ device can be configured to exhibit either a low-resistance state (parallel orientation of free layer with respect to pinned layer) or a high resistance state (anti-parallel orientation of free layer with respect to pinned layer) by utilizing the STT phenomenon in the design. For instance, if an MTJ is initially in a high-resistance state (anti-parallel state), a spin polarised current can be passed from the thin layer (free layer) to the thick layer (pinned layer) to move the electrons from the pinned layer to the free layer. Subsequently, the thin layer exerts a torque on the electrons to align their spin moment toward the magnetic direction.

Meanwhile, as per Newton's third law of motion, the electrons also exert a torque to the thin layer. If the current density is high enough ($>10^6$ A/cm^2), then the torque exerted by the electrons causes the reversal of magnetic alignment of the thin layer. This results in antiparallel (high resistance) alignment to parallel (low-resistance) alignment of the spintronic device, i.e., the MTJ device in the design. Similarly, the reversal of magnetic direction establishing parallel to antiparallel alignment in an MTJ device can be achieved by passing the spin-polarized current from the thick layer to the thin layer.

The value of spin-polarized current required to switch the MTJ model used in this work, from a parallel to antiparallel state (I_{CPtoAP}) and from an antiparallel to parallel state is shown in Table 1. From the values tabulated, it can be noted that the switching from parallel to antiparallel state requires a higher current than compared to the switching from antiparallel to parallel state ($I_{CPtoAP}>I_{CAPtoP}$). Furthermore, the transient response of the MTJ model after the application of different switching currents (I_{CPtoAP} and I_{CAPtoP}) is shown in Fig. 3. As shown in Fig. 3, the MTJ model reported in this work demands low spin-polarized switching currents ($I_{CPtoAP} \approx 26.7$ µA and $I_{CAPtoP} \approx -19.4$ µA) to change the magnetization direction of the free layer with respect to the pinned layer. The works reported in [3, 32], have been investigated to obtain the transient response depicted in Fig. 3 for the MTJ model utilized in this research.

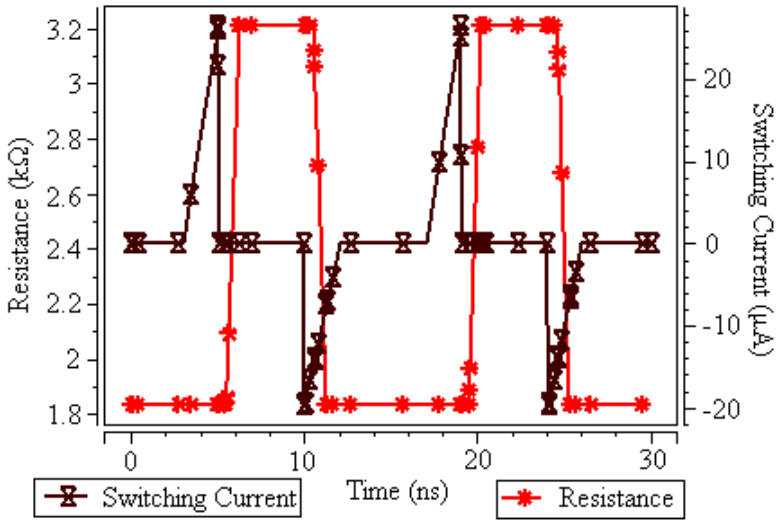

Fig. 3.Transient response of the MTJ model with very low spin-polarized switching currents ($I_{CPtoAP}\approx$ 26.7 µA and $I_{CAPtoP}\approx$ - 19.4 µA).

Table 1. MTJ model parameters utilized in this work.

Parameters	Description	Value
Shape	Shape of MTJ device	Rectangular
Size	Lateral size of the MTJ device	180 × 80 nm^2
t_{FL}	Thickness of the free layer (CoFeB)	1.8 nm
t_{PL}	Thickness of the fixed layer (pinned layer)	2 nm
t_{ox}	Oxide layer height (MgO)	0.85 nm
Area	Area of MTJ surface	40 nm × 40 nm × π /4
Ferromagnetic material	Both free layer and fixed layer material (symmetric MTJ device)	$Co_{0.60}Fe_{0.20}B_{0.20}$
Spacer	Tunnelling barrier material	MgO
R.A	Resistance Area product	9.2 Ω μm^2
K_U	Uniaxial anisotropy energy density	20 ×10^3 erg/cm^3
H_k	Anisotropy field	113.0×10^3 A/m
M_S	Saturation magnetization	456.0 ×10^3 A/m
A	Magnetic damping constant	0.027
E	Elementary charge	1.6× 10^{-9} C
μ_B	Bohr magneton	9.274× 10^{-24} J/T
μ_0	Permeability in free space	1.2566 ×10^{-6} H/m
P	Spin polarization of the tunnel current	0.56

θ	Magnetization angle of the free and reference layer	θ = 0 for parallel magnetization and θ = π for anti-parallel magnetization.
TMR(0)	TMR with 0 voltage bias	150%
$\mathbf{V_{bias}}$	Biasing voltage	0.9 V
$\boldsymbol{R_P}$	Parallel state resistance	1.84 kΩ
$\boldsymbol{R_{AP}}$	Anti-parallel state resistance	4.5 kΩ at (0 bias voltage) 3.21 kΩ at (0.9 V bias voltage)
$\boldsymbol{I_{PtoAP}}$	Switching current from parallel to anti-parallel	≈ 26.7 μA
$\boldsymbol{I_{APtoP}}$	Switching current from anti-parallel to parallel	≈ -19.4 μA

The insulating layer being thin causes electrons to tunnel through the barrier on the application of a bias voltage (V_h) between the two FM layers. In MTJs, the tunnelling current is dependent on the relative orientation of magnetizations of the two FM layers, which can be changed by the application of a magnetic field (Field-Induced Magnetic Switching (FIMS)) or by spin-polarized current (Spin Transfer Torque (STT) or Current Induced Magnetic Switching (CIMS)).

Various important model parameters of the MTJ device utilized to develop the proposed write scheme are tabulated in Table 1. Model equation for the parallel state resistance (R_p) of MTJ device is given by [38]:

$$R_P = \frac{(\tau \times exp(1.025 \times \tau \times \Phi^{1.4}))}{(F \times \Phi^{1.4} \times AREA)} \quad (1)$$

where τ is the thickness of the oxide of the insulating barrier, Φ is the potential barrier height of the insulating barrier, F is a factor calculated from the resistance - area product ($R \times A$),which depends on the material used for three layers. Similarly, the antiparallel state resistance (R_{AP}) is given by [38]:

$$R_{AP} = R_P \times (1 + TMR) \quad (2)$$

Equation (1) represents the model equation to compute the parallel state resistance of the MTJ device, whereas Eq. (2) represents the model equation to compute the anti-parallel state resistance of the MTJ device. Additionally, Table 1 reports the MTJ model parameters utilized in this work.

In the proposed method, MTJ1 and MTJ2 can be replaced with their equivalent resistances R1 and R2 (low resistance or high-resistance state) based on the alignment of the free layer with respect to the pinned layer. Thus, the value ('0' or '1') stored in the CAM cell can be evaluated using Eq. 4. As the parallel state and anti-parallel state configurations depend on the switching current of the MTJ device model, various device parameters are eventually exploited in the proposed circuit to produce the required switching current. Subsequently, the switching current is utilized to configure the MTJ devices and read the stored values using the sense amplifier.

The Tunnel magneto-resistance (TMR) of the MTJ model can be represented as [38]:

$$TMR = \frac{TMR(0)}{\left(1+\left(\frac{V_{bias}}{V_h}\right)^2\right)} \quad (3)$$

where, *TMR* is the real value of the *TMR* ratio, *TMR*(0) is the *TMR* ratio with 0 bias voltage, and V_h is the bias voltage when *TMR* = 0.5×*TMR*(0). When two ferromagnets are separated by a very thin insulating layer, a quantum mechanical effect known as Tunnel magneto-resistance (TMR) is observed. When current pulses are passed through a piece of magnetic material, the atomic lattice starts vibrating. Due to the atomic lattice vibrations, a type of quasi-particles known as magnons is created. The creation of magnons results in the energization of the

electrons present within the atomic lattice. Being energized, these electrons tunnel from one piece of magnetic material to another. This tunnelling effect is referred to as the TMR effect.

2.2. Architecture of CAM cell

The schematic diagram of $m \times n$ (m-words with n-bits per word) CAM system is shown in Fig. 4. A CAM cell itself consists of the storage memory array which stores a single bit of data. Search lines (*SL* and *SLB*) are loaded with the data input in the search register. Each word in a CAM cell is associated with a match line(*ML*) which indicates whether the search word and stored word are the same (the match case) or are different (a mismatch case or miss). Thus, *ML* status i.e. either high logic state (match condition) or low logic state (mismatch condition) is used to find the address of searched data from the stored data array in CAM. CAM system performs its search operation in the entire storage array which sets *ML* status corresponding to match or mismatch conditions.*ML* discharges to logic state '0' in case of mismatch and holds logic state '1' in case of the match [41, 42].*ML* sense amplifiers (MLSAs) connected with each *ML* senses the logic state of *ML*. Finally, the address encoder provides the address of the match location from the output of the MLSAs [8].

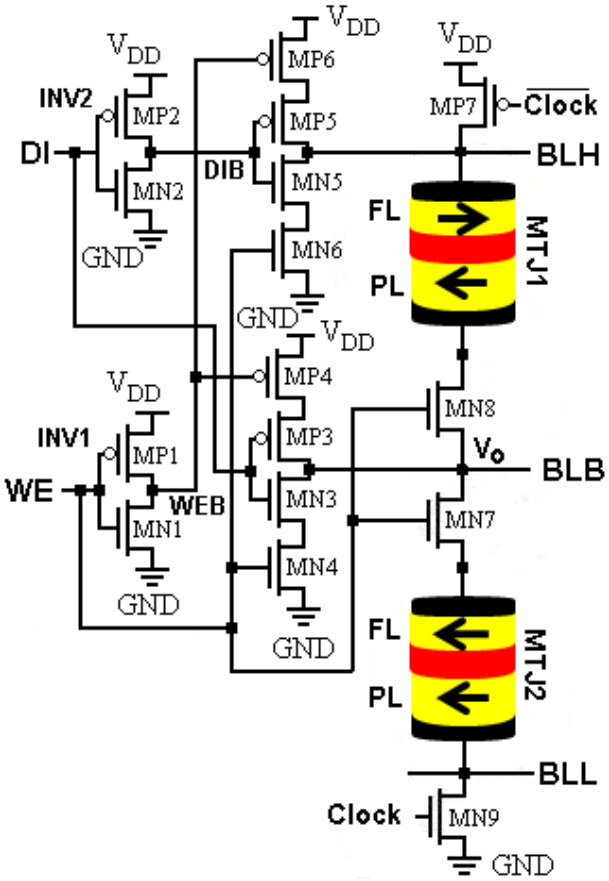

Fig. 4. Spin-polarized MTJ based write scheme for storing 1-bit data at the storage node V_O of the CAM cell.

The MTJ based write scheme proposed in this paper enables to store 1-bit input data in the storage node V_O of the CAM cell (shown in Fig. 5). MTJ device is a non-volatile element in the proposed write scheme and can store data bits in the form of resistances (either high-logic state '1' or low-logic state '0'). The resistance of MTJ depends upon magnetic configuration - parallel (P) or antiparallel (AP). MTJ provides ease of storing data as it requires a very low switching threshold current (I_{CPtoAP}≈26.7 µA and I_{CAPtoP}≈-19.4 µA) which can flip the magnetic orientation of spins. Thus, MTJ proves to be efficient in storing data with low supply consumption and also provides storage for a longer duration [26, 43]. The voltage at the storage node V_O (see Fig. 5) is examined in this work to explain the proposed write scheme.

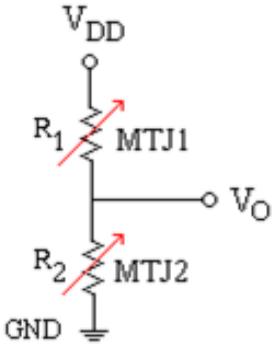

Fig. 5. Voltage divider network formed by the proposed write scheme after replacing MTJ1 and MTJ2, shown in Fig. 4, with their equivalent resistances R_1 and R_2, respectively.

3. Proposed MTJ based write scheme for CAM cell

The non-volatile properties of MTJ are explored in this paper to employ it as a non-volatile element of the proposed write scheme for a CAM cell. The proposed MTJ based write driver can store 1-bit data ('0' or '1') provided to the CAM cell and can also retain data for a longer duration, even if the power supply is turned off, due to the MTJ devices incorporated in the scheme. Storage node V_O of the CAM cell (see Fig. 4) is loaded with 1-bit data based on the inputs provided at the data input (*DI*) terminal of the proposed circuit. Bit lines (*BL* and *BLB*) are complemented by each other. Further, for ease of explanation *BL* is represented as *BLH* (upper section) and *BLL* (lower section) in the circuit shown in Fig. 4. To execute write operation using the proposed circuit, write enable (*WE*) is set to high logic state. During a write operation, the proposed write driver simply sets the MTJs to exhibit either a high resistive (antiparallel state) or low resistive (parallel state) path. Applying proper Clock and Clock-bar signal to the proposed circuit, a simple voltage divider network (if we replace MTJ1 and MTJ2 with their equivalent resistances R_1 and R_2, respectively in Fig. 4) is established as shown in Fig. 5. Based upon the configuration states of the MTJ1 and MTJ2, the logic stored at storage node V_O can be determined as:

$$V_O = V_{DD} \frac{R_{2(MTJ2)}}{R_{1(MTJ1)}+R_{2(MTJ2)}}. \quad (4)$$

Thus, by flipping the states (changing the resistances) of MTJs either logic state '0' or '1' can be written on storage node V_O of the CAM cell.

The write operation is performed by asserting the write enable (WE) signal in the proposed CAM cell. Thus, *WE* are kept at a high logic state and its' complement *WEB* is kept at a low logic state. Here, WEB is used to represent the inverted write-enable. The inverter INV1, composed of MN1/MP1, provides an inverted write enable (WEB) signal. *WE* = '1' turns ON transistor MN7 which connects the MTJ2 with *BLL* and *BLB*. Similarly, *WE* = '1' also turns ON transistor MN8 which connects MTJ1 with *BLH* and *BLB*. Meanwhile, keeping *WE* at high logic also turns ON transistors MN4 and MN6. *WEB* at a low logic turns ON transistors MP4 and MP6. Thus, *WE* and *WEB* initiates inverter circuits composed of MN3/MP3 and MN5/MP5 by providing a connection with power supplies (V_{DD} and GND), to enable the write operation. A detailed explanation of the write operation is provided in the following subsection.

The proposed scheme acts as a magnetic memory for the CAM cell, due to the MTJ present in the design, which can hold data bit even if the power supply is turned off, thus, acting as a non-volatile memory circuit. Simulation results reported in this work also show the non-volatility of the proposed scheme. Apart from the nonvolatility, other performance parameters such as power consumption, delay, PDP, and EDP have been evaluated to establish a proper comparison with the other available designs. Based on various control signals data bits can be stored and retrieved from the storage node V_O. For understanding the write operation of the proposed scheme, various signals and their operations are as follows:

- Clock signal: Circuits operate only if the clock signal is assisted. Thus, transistors MP7 and MN9 act as sleep transistors for the proposed circuit and reduce power consumption when the circuit is not being operated.
- Data Input (*DI*): Data to be stored at the storage node is supplied to this terminal.
- Write enable (*WE*): This signal is kept high to write (store) data from the DI (data input) terminal to the storage node V_O.

Write Operation

Write '1' operation: To perform the write '1' operation for storing logic '1' at the storage node V_O of the CAM cell, MTJ2 is set to exhibit a high resistance path and MTJ1 is set to exhibit a low resistance path. The data input (DI) signal is provided with logic '1' to the input terminal of the inverter (INV2) composed of MN2/MP2 which provides DIB= '0' at the output node of the INV2. DI = '1' at the input terminal of the inverter composed of MN3/MP3 provides inverted logic '0' to be written on BLB.

Meanwhile, DIB = '0' at the input terminal of the inverter composed of MN5/MP5 provides inverted logic '1' to be written on BLH and BLL. Now, as BLH and BLL are at logic '1' and BLB is at logic '0', these initiate a flow of current (switching current) due to the potential difference between the two connecting nodes. The current density ($> 10^6$ A/cm^2) of the switching current (I_{APtoP}) flowing through the FL to PL of MTJ1 (see Fig. 4) is high enough to exert spin-transfer torque (STT)capable to reverse the magnetic polarization of the free layer of MTJ1. Initially, MTJ1 is in an antiparallel state and the switching current configures the MTJ1 from the antiparallel-to-parallel state. This forms a low resistance path through MTJ1 connecting BLE and BLB. Meanwhile, BLL at logic state '1' and BLB is at logic state '0', this results in a flow of current (switching current ((I_{PtoAP})))

due to the potential difference between the two connecting nodes. The current density of the switching current flowing through the PL to FL of MTJ2 (see Fig. 4) is sufficient to provide STT capable to reverse the magnetic polarization of the FL of MTJ2. Initially, MTJ2 is in a parallel state and the switching current configures MTJ2 from the parallel-to-antiparallel state. This forms a high resistance path through MTJ2connectingBLL and BLB. Thus, MTJ2 is set to exhibit ahigh resistance path and MTJ1 is set to exhibit a low resistance path. To initiate the voltage divider network, the clock signal is set to high logic state, and the Clock bar is at a low logic state. From (4), the high logic (logic '1')stored at storage node V_O due to the voltage divider network developed by the high resistance of MTJ2 and low resistance of MTJ1 (see Fig. 6) can be evaluated.

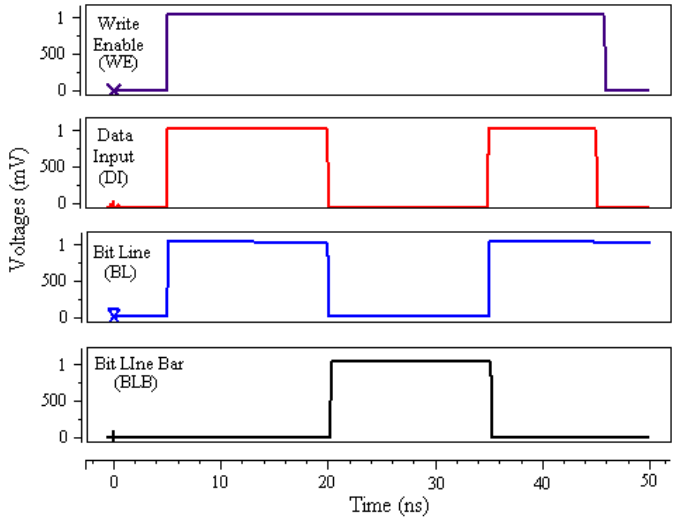

Fig. 6. Write operation of the proposed CAM cell. *BL* indicates the logic state of both *BLL* and *BLH*.

Write '0' operation: As mentioned above, WE = '1' and WEB = '0' initiates inverter circuits composed of MN3/MP3 and MN5/MP5 by connecting them with the supply rail. To perform the write '0' operation on the storage node V_O of the CAM cell, MTJ2 is set to exhibit a low resistance path and MTJ1 is set to ahigh resistance path. The data input (DI) signal is provided with logic '0' to the input terminal of the inverter (INV2) composed of MN2/MP2 which provides DIB= '1' at the output node of the INV2. DI = '0' at the input terminal of the inverter composed of MN3/MP3 provides inverted logic '1' to be written on BLB. Meanwhile, DIB = '1' at the input terminal of the inverter composed of MN5/MP5 provides inverted logic '0' to be written on BLH and BLL. Now, as BLH and BLL are at logic '0' and BLB is at logic '1', this results in a flow of current (switching current) due to the potential difference between the two connecting nodes.

The current density (> 10^6 A/cm^2) of the switching current (I_{PtoAP}) flowing through the PL to FL of MTJ1 (see Fig. 4) is high enough to exert spin-transfer torque (STT) capable to reverse the magnetic polarization of the free layer of MTJ1. Initially, MTJ1 is in a parallel state and the switching current configures the MTJ1 from the parallel-to-antiparallel state. This forms a high resistance path through

MTJ1 connecting BLH and BLB. Meanwhile, BLL at logic state '0' and BLB is at logic state '1', this results in a flow of current (switching current ((I_{APtoP}))) due to the potential difference between the two connecting nodes.

The current density of the switching current flowing through the FL to PL of MTJ2 (see Fig. 5) is sufficient to provide STT capable to reverse the magnetic polarization of the FL of MTJ2. Initially, MTJ2 is in an antiparallel state and the switching current configures MTJ2 from the antiparallel-to-parallel state. This forms a low resistance path through MTJ2 connecting BLL and BLB. Thus, MTJ2 is set to exhibit a low resistance path and MTJ1 is set to exhibit a high resistance path. To initiate the voltage divider network, the clock signal is set to high logic state and the Clock bar is at a low logic state. From (4), the low logic (logic '0') stored at storage node V_O due to the voltage divider network developed by the low resistance of MTJ2 and high resistance of MTJ1 (see Fig. 4) can be evaluated.

4. Simulation Results

Profound simulations are performed with the MTJ model reported in Section 1.Different signals asserted during the execution of write operation are mentioned in Table 2 with their logic state attained in different cases. Figure 6 shows the simulation waveforms obtained while performing the write operation using the proposed MTJ based write scheme. *BL* and *BLB* are set depending upon the value of the *DI* signal.

The high voltage at node V_o is represented as logic high '1' and the low voltage at node V_o as logic low '0'. For the proposed circuit, based on the value of $R_{(MTJ1)}$ and $R_{(MTJ2)}$, the voltage at the storage node V_O ranges from 0.21V to 0.49V (using (4) and the value of MTJ model parameters reported in Table 1), which can be set as logic '0' and logic '1' for 0.21V and 0.49V, respectively. This can be done by incorporating a LO-skewed and High-skewed inverter in the MLSAs. These values of logic '0' and '1' are utilized further to tabulate various logic states reported in Table 2.

Furthermore, the proposed write scheme requires low spin-polarized switching currents ($I_{CPtoAP} \approx 26.7$ µA and $I_{CAPtoP} \approx -19.4$ µA) to perform the write operation in the CAM cell. Sleep transistors MN7/MN9 utilized in the proposed design help us in reducing the power consumption while the circuit is not in operation. Thus, the proposed design addresses one of the major challenges in the write circuit for a CAM cell by reducing the power consumption in the circuit. For TMR% = 150, the proposed design consumes only 61.86 µW of power, and the PDP of the write circuit is 5.311×10^{-14} J, which is very less because of the lower switching current required to flip the states of MTJ. Compared to previous designs using trigger pulse generators [44-49], the proposed design consumes lesser power as demonstrated by the simulation results in this study.

Also, using MTJs as a non-volatile element in the proposed design, it is possible to reduce the power consumption drastically using the power-gating technique. The ability to retain data using MTJ in the design also makes the CAM cell non-volatile and adds novelty to the reported work. Figure 6 illustrates the simulation results of the proposed CAM cell along with the different control signals (Write enable (WI) and Data Input (DI)) used to perform write and read operations. Write operation is demonstrated as the logic values at *BL* and *BLB*, provided at the DI terminal of the CAM cell. All simulations have been extensively verified using SPICE and codes

have been written in Verilog-A. The proposed design produces a switching current as required for the operation of the MTJ device.

Table 2. Various logic states during write operation by the proposed write scheme.

Write enable (WE)	Data Input (DI)	Bit lines (BLH and BLL)	Bit line Bar (BLB)	Clock	Clock bar	Logic state at node V_O
0	×	×	×	×	×	×
1	0	0	1	1	0	1
1	1	1	0	1	0	0

5. Conclusion

This research work reports an MTJ based non-volatile write scheme for a CAM cell for storing 1-bit at storage node V_O. The storage node V_O can be set to hold either low logic or high logic state based upon the *DI* signal provided. The focus of this paper is to employ the MTJ model to store different logic states at the storage node of the CAM cell. Tailoring the spin-polarized switching currents through the MTJ device result in storing either high or low logic states determined by the configuration of MTJs.

The proposed design proves to be power efficient by consuming low spin-polarized switching currents ($I_{CPtoAP} \approx 26.7$ μA and $I_{CAPtoP} \approx -19.4$ μA) to perform the write operation in the CAM cell.

The MTJ based proposed circuit also possesses properties desired for memory application such as non-volatility, low power consumption, high speed of operation, and unlimited endurance. The simulation results obtained during the execution of write operation using the proposed write scheme satisfies the required attributes for storing either low or high logic state at the storage node V_O of the CAM cell.

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