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DESIGN AND OPTIMIZATION OF 0.18 μm CMOS TRANSIMPEDANCE AMPLIFIER FOR 20 Gb/s OPTICAL COMMUNICATIONS USING GENETIC ALGORITHMS

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Abstract

A comprehensive study focusing on the design and optimization of a single stage transimpedance front-end amplifier (TIA) for over 20 Gb/s optical system applications is presented in this paper. The work involves characterizing the most important parameters of the TIA circuit such as frequency bandwidth, transimpedance gain, input referred noise current, group delay and DC power consumption. An optimization procedure exploiting genetic algorithms (GA) technique is employed to improve the TIA performance, obtaining the optimal transistor geometry, which has then led to maximizing the amplifier bandwidth without sacrificing the IRN and group delay parameters. To this end, several multi-objective function formulations are used as fitness function. The simulation results showed that the formulation of the fitness function taking the transistor's transconductance (g_m) and the bandwidth at -3 dB (BW_{3dB}) into account provides a significant performance. The achieved BW_{3dB} value, DC power consumption and input referred noise current were 15.7 GHz, 4.6 mW and 9.7 pA/√Hz, respectively, which are promising compared with the state of the art. A MATLAB environment for the genetic algorithm implementation is utilized along with a radio frequency based advanced design system (ADS) software for the 0.18 μm CMOS transimpedance technology simulation.

Keywords: CMOS based optical receiver, GA, MATLAB, OEIC modeling, Transimpedance amplifier.

1. Introduction

The ever-increasing traffic in telecommunication networks has led to great efforts in developing high data rate optoelectronic integrated circuit (OEIC) and their associated devices. This is becoming even more urgent with the recent advancement in 10 Gb/s Ethernet passive optical network (EPON) systems and the rise in the speed of microprocessors and memory capacity. The required high data rate systems call for cost-effective optical receivers while operating at extremely high frequencies [1]. It is well-known that fiber optic architecture are the most favorable transmission systems over the conventional coaxial cable and waveguide signal distribution for short and long-distance applications. This is due the insensitivity to electrical disturbance with almost no crosstalk impact and the capability to avoid electrical ground loops associated with fiber optic [2].

The front-end transimpedance amplifier (TIA) is a vitally important part in the optoelectronic receiver and is used to convert the electrical photocurrent into an acceptable voltage level. The resulting voltage form is eventually passed on to a decision circuit, providing a synchronized signal within a standard digital format [3]. In modern optical system, the dominant challenge in designing a TIA is to achieve a wide frequency bandwidth while still maintaining a low noise characteristic. This may pave the way towards the use of a single preamplifier stage-based CMOS technology, assisting not solely in minimizing the chip area, but also reducing the DC power consumption [4, 5]. The CMOS amplifier circuit is incorporated with a PIN-photodiode utilizing a hybrid integration scheme. For the whole circuit characterization, the performance can be assessed taking the most crucial parameters into account including the frequency bandwidth and transimpedance gain of the TIA, IRN, group delay and the DC consumed power of the OEIC [6, 7].

The tradeoff among these parameters is carefully investigated, aiming at enhancing the necessary high-speed operations. Hence, to obtain the optimum values for aforementioned design parameters based on analytical solution implies the use of a time-consuming procedure, which could end-up with not achieving the required target specifications [8]. In this paper, an evolutionary genetic algorithm is utilized offering powerful features for integrated circuit design and optimization in terms of taking a short route in computational method to extract the optimum design parameters. In general, the evolutionary algorithm (EA) is a stochastic and repeated process that operates on a population known as a set of individuals (chromosomes). The population is randomly generated and every individual in the population represents one solution to the problem being solved. An evaluating technique is applied to every single individual through a fitness function (i.e., objective function) by examining its quality with respect to the required specifications. The ultimately adopted solution value is the quantitative information that the algorithm uses to guide the search, robustly relying on the use of a selection, crossover, and mutation operators [9, 10].

CMOS based TIA preamplifiers have been extensively demonstrated in recent years [11-13]. Noh was reported [11], a frequency response analysis for a capacitive feedback TIA, concentrating on derived transfer function model for critical design parameter analysis to reduce thermal noise of the circuit. A fully differential-TIA with 65 nm CMOS was also studied and exhibited a transimpedance gain of 54 dBΩ [12]. Other TIA-CMOS technology attempts with multiple peaking scheme

and/or multi-stage amplifiers were proposed as alternative configurations for conventional single stage circuit [14, 15]. However, those techniques are suffering from circuit implementation complexity, leading to high-power consumption and an increase in the ultimate chip size. With pursuing a small TIA geometry, a 10 Gb/s inductorless photoreceiver was implemented exploiting dual feedback loop TIA [16], nevertheless it has a poor high-frequency performance not exceeding 7 GHz and achievable -17.8 dBm optical sensitivity. In general, there are two main TIA categories, namely open-loop and closed-loop architectures.

Due to the stringent trade-off between the transimpedance gain and output voltage level in open-loop circuit, the closed-loop configuration is favored in preamplifier ICs design. Of note, the shunt feedback resistor in closed-loop circuits offers low TIA input impedance without carrying any bias current, significantly easing the compromise between preamplifier gain and output voltage level [14]. A wide frequency bandwidth TIA requires a small photodiode capacitance and/or low TIA input impedance which contributes to localizing the dominant pole introduced by the photodiode at high frequency. An on-chip inductive peaking technique accompanying with shunt-shunt feedback topology can be utilized to extend the frequency bandwidth of the circuit. At this end, proposing an analytical model for integrated TIAs prior to experimental process is indispensable, helping to fulfil the required vendor/end-user specification and performance. Although many recent studies have demonstrated a shunt-feedback and peaking inductive approach in TIA circuits [2, 7, 13, 14], there is a lack of depth-analysis for the results particularly with the use of GA technique.

In this work, a single-stage 0.18 μm CMOS-TIA preamplifier and photoreceiver were analyzed, designed, and optimized using genetic algorithm, offering low DC power consumption feature and small overall IC size capability. The remainder of this paper is organized as follows: Section 2 presents the analysis and design of the Transimpedance amplifier circuit. The step by step design procedure of optimal TIA parameters based on the genetic algorithm optimization technique is covered in section 3. Finally, section 4 constructs from the concluded points.

2. Transimpedance Amplifier Circuit Design and Analysis

2.1. Importance of transimpedance amplifier (TIA)

Despite a very low transmission loss of only 0.2-0.5 dB/km in fiber optics, the power of the travelling light is still exposed to decline over distances exceeding a few tens of kilometers without repeaters. The light is captured by a photodiode at the receiver unit, in which the photocurrent is generated, and the resulting current value is substantially dependent on responsivity of the photodiode itself. For long-haul fiber optics, the use of preamplifiers is paramount in improving the photoreceiver sensitivity. A very low light power of ~ -20 dBm would make the corresponding photocurrent very small particularly with the integrated unity internal gain photodiodes. In such a scenario, it becomes rather difficult for the decision circuits to efficiently reshape the received signal and the widely used TIA preamplifier to boost the electrical signal level is thus invaluable. The high frequency TIA circuit response plays a pivotal role in the overall OEIC performance and to a large extent determine the frequency bandwidth and group delay values. The combination of a photodiode and TIA integrated circuit is called as a front end of optical receiver [17-19]. In recent years, numerous CMOS based

TIA configurations have been reported in the attempt at exploring various input stages suitability to isolate the large input capacitance of the photodiode from loading on the preamplifier thereby maximizing the frequency bandwidth. The influence of the parasitic capacitances associated with the transistor and their effect on the bandwidth response have also been discussed in the literature [20-23].

In this paper, a TIA circuit with the commonly exploited shunt-shunt feedback topology is presented as a case study for 0.18 μm CMOS technology.

2.2. Transimpedance amplifier (TIA) topology

The high impedance (HZ) open-loop TIA circuit configurations were studied to realize front-end amplifiers. A large biasing resistor is often used to implement the HZ amplifier, meaning that the input admittance is governed by the overall input capacitance of the circuit, which tends to further minimize the circuit noise [17]. The HZ configuration occupies a large area in the chip due to the required high resistor value exceeding a few kΩ.

Unlike HZ topology, TIA amplifiers with a moderate feedback resistor value (known as closed-loop architecture) have several benefits including wide bandwidth and dynamic range. A well-designed transimpedance preamplifier can match the noise performance of the HZ amplifier [24]. Therefore, the number of amplifier stages as well as their related passive elements values are the demanding and challenging parameters to control among all system units [25]. A schematic of the preamplifier topologies with an open loop (HZ) and closed-loop (TIA) circuits adopted in this work are depicted in Fig. 1 [26].

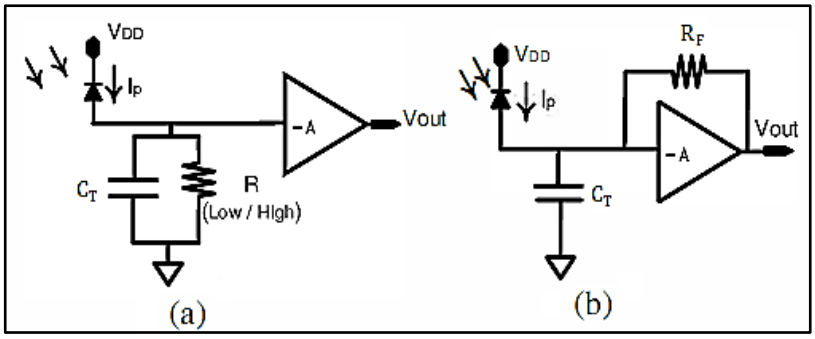

Fig. 1. TIA topology: (a) Open loop, (b) Closed loop.

In Fig. 1 the current (I_P) represents the photocurrent generated by the photodiode, "A" is the open loop gain, C_T is the overall input capacitances of the amplifier and the input and feedback resistances are denoted as R and R_F respectively. In this work, the open loop topology is replaced by a closed loop TIA topology through connecting an R_F resistor. It is worthwhile pointing out that the feedback resistor governs the transimpedance gain (Z_T), noise performance and frequency bandwidth of the amplifier, emphasizing that an effective balance for R_F value is required [17, 26]. The superiority of this topology is also reflected in its capability to provide a high gain without a degradation in the stability of the photoreceiver [27]. Basically, the definition of Z_T is the ratio of the output voltage

to the input photocurrent (V_o/I_{in}). From Fig. 1(b), the gain of TIA can be given as in Eq. (1) [1, 26].

$$\frac{V_{out}}{I_{in}} = -\frac{A}{(A+1)} \times \frac{R_F}{1+\frac{R_F C_D}{A+1} s} \quad (1)$$

According to Eq. (1), the feedback amplifier has a mid-band transimpedance gain of approximately R_F but with a time constant of ($\frac{R_F C_D}{A+1}$) and this may yield a -3dB bandwidth expressed as in Eq. (2).

$$f_{3dB} = \frac{1+A}{2\pi R_F C_T} \quad (2)$$

Owing to Eq. (2), the dominant pole that limits the high frequency operation is attributed to $R_F C_T$ time constant. A small input capacitance of the amplifier and/or downscaling the lateral dimensions of the photodevice is fundamental in extending the frequency bandwidth for high data rate optical systems requirements. With an efficient high frequency preamplifier design, the dominant pole response caused by the total input capacitance C_T including photodiode contribution situated at the input terminal must be shifted to high frequency by the use of a low input impedance configuration as a first stage and/or a properly chosen feedback resistor value.

2.3. Shunt-feedback TIA analysis and realization

2.3.1. Shunt feedback TIA topology

The most common TIA structure is the voltage-current feedback topology (i.e., known as shunt-shunt), in which a negative feedback network is represented by a voltage sensing at the output node and summing a proportional current at the input node. The block diagram of the shunt-feedback TIA is shown in Fig. 2(a). There are many ways to implement the inverting voltage amplifier and one of them is the single stage common source 0.18 μm CMOS amplifier that is used here as depicted in Fig. 2(b) [17].

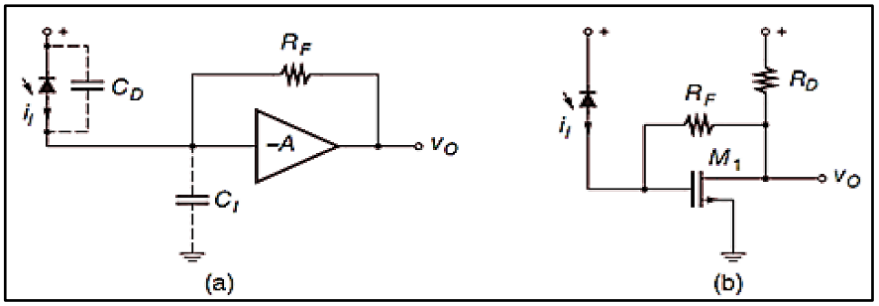

Fig. 2. Structure of shunt feedback TIA: (a) Block diagram. (b) Transistor level implementation with a single MOSFET transimpedance amplifier.

Whilst the primary function of the TIA circuit is to convert a small photocurrent into an amplified voltage form, maintaining a low referred noise in the output is paramount for the subsequent data recovery circuit. To fully characterize the preamplifier circuit, Z_T, bandwidth, group delay (τ_d) and IRN are broadly discussed. From Fig. 2(b) the closed loop transimpedance can be formulated by the following equations [1, 17, 28, 29].

$$Z_T(s) = -Z_T \cdot \frac{1}{1+\frac{s}{W_0 Q}+\frac{s^2}{W_0^2}} \quad (3)$$

where the Z_T is the transimpedance gain and given by Eq. (4):

$$Z_T = \frac{A}{A+1} R_F \quad (4)$$

where W_0 and Q are the angular frequency and quality factor of the pole pair which are expressed in Eqs. (5) and (6) respectively.

$$W_0 = \sqrt{\frac{A+1}{R_F C_T T_A}} \quad (5)$$

$$Q = \frac{\sqrt{(A+1)R_F C_T T_A}}{R_F C_T + T_A} \quad (6)$$

When Q is equal to $(\frac{1}{\sqrt{2}})$, the amplitude response of Eq. (1) is maximally flat (Butterworth response) [17].

T_A: is the amplifier time constant needed for Butterworth response and is given by:

$$T_A = \frac{R_F C_T}{2 \times A} \quad (7)$$

With practical photoreceiver integration, the photodiode is loaded on the preamplifier input impedance, the photodiode capacitance (C_D) and the TIA input capacitance C_I are in parallel, yielding a total input capacitance of:

$$C_T = C_D + C_I \quad (8)$$

The open-loop gain of the common source amplifier, $A = g_m R_D$.

where R_D : is the resistor connected at the drain of M_1 and g_m : is the transistor's transconductance of the M_1 that represented by:

$$g_m = \sqrt{2 \times \mu_n \times C_{ox} \times (\frac{W_1}{L_1}) \times I_D} \quad (9)$$

2.3.2. High frequency evaluation of shunt-feedback TIA

The -3 dB bandwidth of the TIA integrated with the photodiode can be expressed as $BW_{3dB} = W_0/2\pi$. Where W_0 is given by Eq. (5) and a Butterworth response is selected. Hence, the fundamental time constant of the amplifier, T_A is involved here and the bandwidth of OEIC is formulated as in Eq. (10) [28, 29].

$$BW_{3dB} = \frac{\sqrt{2A(A+1)}}{2\pi \times R_F C_T} \quad (10)$$

For a second order system, the transimpedance is constrained by [17, 24].

$$Z_T \leq \frac{A \times F_A}{2\pi \times C_T \times BW_{3dB}^2} \quad (11)$$

where $(A \times F_A)$ is the gain-bandwidth product of the single-pole voltage amplifier which is roughly constant for a given technology. It is evident that the transimpedance value is inversely proportional to the -3 dB bandwidth of the TIA. With advanced CMOS technology devices, a low DC biasing voltage may contribute to a reduction in the attainable open loop gain. A cascaded amplifier to

boost the gain is still not recommended due to a difficulty in ensuring an adequate phase margin for proper circuit operation [17].

For the shunt feedback TIA, the input referred noise current is given by Eq. (12) [28, 30, 31]:

$$\overline{I_{n,in}^2} \approx \left(\frac{4KT\gamma}{g_{m1}R_F^2} + \frac{4KT}{g_{m1}^2 R_F^2 R_D} + \frac{4KT}{R_F}\right) \quad (12)$$

where K and T is the Boltzmann's constant and the absolute temperature in Kelvin respectively. The noise excess factor of the transistors is denoted as γ. Equation (12) reveals that the input-referred noise is passed to the input while scaling it with R^2_F and the overall input-referred noise current is approximately equal to the one of a simple impedance front-end amplifier.

3. Optimal Design Parameters of Shunt Feedback TIA

For a shunt-feedback topology, it is not straightforward to manually optimize the circuit performance because of the existence of several curial parameters dependent on each other commencing from the required wide bandwidth, low IRN, high transimpedance gain alongside with a low DC power consumption and small delay group factor. In tradition design approach, one variable can be pursued while keeping others fixed and is repeated many times until reaching the target specifications. This is undoubtedly a time-consuming procedure and, in most cases, does not lead to the optimum results for a practical circuit implementation. In practice, the ultimate geometry of the TIA amplifier is key in obtaining the desirable circuit performance, which can be formulated as an optimization problem in the genetic algorithm. The target design performance specifications for a 0.18 μm CMOS TIA is summarized in Table 1 using a photodiode capacitance of 50 fF.

Table 1. Performance specifications of the photoreceiver.

Parameters	Specification target
V_{DD} (V)	1.8
BW_{3dB} (GHz)	Max.
Transimpedance gain (Z_T(dBΩ))	Max.
Input refereed noise current (IRN)	Min.
Delay group (τ_d)	Min.
I_D (mA)	Min.
R_F (Ω)	Min.
R_D (Ω)	Min.
W_1 (μm)	Min.
DC Power consumption (mW)	Min.

From Eqs. (3) to (12), it is obvious that the variables of the shunt feedback TIA shown in Fig. 2(b) are the width of the transistor (W_1), the drain current (I_D), feedback resistor (R_F) and R_D resistor. These variables control the overall amplifier performance and are implicitly included in these equations. A genetic algorithm technique based on MATLAB environment is employed to find the optimum values of these variables.

3.1. Proposed optimization steps for TIA design based on genetic algorithm

The design procedure steps using genetic algorithm are presented as follows:

i. Creation of an initial population, the genetic algorithm generates an initial random binary population. Each single individual (chromosome) represents the value of the variables (i.e., I_D, R_F and R_D).

ii. Conversion of the binary population to real values.

iii. Fitness function and constraints, the individual in the population is evaluated to satisfy the desired objective function and constraints.

iv. In this step, each chromosome is tested to obtain the required performances of TIA by a properly formulated fitness function. If one chromosome satisfies the desired performances of the circuit, then the design parameters are obtained, and the algorithm is terminated (jump to step 8).

v. Stop conditions, in here the number of generations is examined as to whether it exceeds the specified number or not? If point number 5 is satisfied, then jump to the end (jump to step 8).

vi. Apply genetic operator (selection, crossover, mutation).

a. **Selection**: the variable solutions with better fitness function have more chance to be chosen for the next step.

b. **Crossover** is achieved by individuals that are selected in the earlier point (a).

c. **Mutation**, this process is applied to attain a minor change in some individuals.

vii. Back to point number 3.

viii. Stop and end the algorithm.

3.2. Design of the optimal variables as chromosomes

Since the drain current (I_D), feedback resistor and the R_D resistor control the electrical behaviour of the TIA circuit, at least in this present study, therefore each chromosome in the population is represented with three genes (I_D, R_F, R_D). The variable parameters, their associated variation range and binary representation are tabulated in Table 2. More importantly, the binary representation is determined by the accuracy of real values corresponding to the selected variables [9]. As a starting point, the variation range of the used parameters are chosen according to recent reported papers in the literatures.

Table 2. Design variables of TIA based on genetic algorithm.

Variable parameters	Variation range	Number of bits in each variable
I_D **(mA)**	[0.1, 5]	13 bits
R_F **(Ω)**	[100, 1000]	10 bits
R_D **(Ω)**	[100, 1000]	10 bits

3.3. Construction of fitness evaluation function

The fitness function value is used for the chromosome (i.e., the second step in the genetic algorithm), in which the evaluation procedure is assigned with its fitness value. Generally, higher fitness value corresponds to an additional optimal

individual, meaning that the function is maximized/minimized and then evaluated for every single individual [32].

Multi-objective optimization problems

Basically, multi-objective optimization problems involve more than one objective function. Such a fitness function is to be minimized or maximized. The general formula of multi-objective function can be expressed as [33, 34]:

$$\begin{aligned} &\text{Min / Max } f_m(x), m = 1, 2, \dots, M \\ &\text{subject to } g_i(x) \geq 0, j = 1, 2, \dots, J \\ &h_k(x) = 0, k = 1, 2, \dots, K \\ &x_i^{(L)} \leq x_i \leq x_i^{(U)}, i = 1, 2, \dots, n \end{aligned}$$

Lower bound Upper bound

The fundamental difference between single and multi-objective optimization is that, in multi-objective optimization problem, the desired result is a set of points that describe the best trade-off between competing objectives rather than a single point representing the extrema of a single objective function. In this paper, four fitness formulation functions are developed to find out multiple optimal solutions in one execution. Table 3 illustrates different multi-objective fitness functions, linear inequality, non-linear inequality, constraint parameter and variation range of variables.

Table 3. Construction various multi-objective fitness function.

FTF$_1$	**FTF$_2$**	**FTF$_3$**	**FTF$_4$**
Max (BW_{3dB}, A)	Max (g_m, BW_{3dB})	(1/R_F, BW_{3dB})	Min (R_F, P)
Subject to :	Subject to :	ct to :	Subject to :
V_{DD} = 1.8 V	V_{DD} = 1.8 V	1.8 V	V_{DD} = 1.8 V
IRN ≤ 25 pA/√Hz	IRN ≤ 25 pA/√Hz	N ≤ 25 pA/√Hz	IRN ≤ 25 pA/√Hz
Z_T ≥ 40 dBΩ	Z_T ≥ 40 dBΩ	40 dBΩ	Z_T ≥ 40 dBΩ
P ≤ 5m W	P ≤ 5m W	mW	P ≤ 5 mW
BW_{3dB} ≥15 GHz	BW_{3dB} ≥15 GHz	BW_{3dB} ≥15 GHz	BW_{3dB} ≥15 GHz
0.1 mA ≤ I_D ≤ 5 mA	0.1 mA≤I_D ≤ 5 mA	0.1 mA≤I_D ≤ 5 mA	0.1 mA≤I_D ≤ 5 mA
100 Ω ≤ R_F ≤1000 Ω	100 Ω≤R_F≤1000 Ω	100 Ω≤R_F≤1000 Ω	100 Ω≤R_F≤1000 Ω
100 Ω≤R_D≤1000 Ω	100 Ω≤R_D≤1000 Ω	100 Ω≤R_D≤1000 Ω	100 Ω≤R_D≤1000 Ω
1 μm≤W_1≤25 μm	1 μm≤W_1≤25 μm	1 μm≤W_1≤25 μm	1 μm≤W_1≤25 μm

where: FTF$_i$: Fitness Function, i= 1,2 ,3, 4. BW_{3dB}: is the -3 dB bandwidth of the photoreceiver as given in Eq. (10). A: is the open loop gain of the common source amplifier. g_m : is the transistor's transconductance and given in Eq. (9). P: is the DC power consumption and given as $P = V_{DD} \times I_D$. IRN: is the input referred noise current as given in Eq. (12). Z_T: is the transimpedance gain in dBΩ as given in Eq. (4).

The aforementioned multi-objective fitness functions in Table 3 are formulated for the purpose of achieving the optimal geometry of the CMOS device and relevant desired performance of the TIA preamplifier. With the analytical consideration, each multi-objective fitness function has an impact on BW_{3dB}, Z_T, IRN and P and/or a combination of two of which. Moreover, the multi-objective fitness function (FTF) is formulated based on one of the most widely used method which

uses the weighted sum approach and is employed to carefully balance the circuit performance trade-offs. This method may be represented in Eq. (13) [33, 35, 36].

$$\mathrm{FTF_{sol}} = \sum_{i=1}^{\mathrm{Nf_i}} \mathrm{Eval.f_i} \times \mathrm{W_{ei}} \quad (13)$$

where: $\mathrm{FTF_{sol}}$: represents the multi-objective fitness function solution. $\mathrm{Nf_i}$: is the number of fitness function. i : is the index of the fitness function. $\mathrm{Eval.f_i}$: is the fitness evaluation function. $\mathrm{W_{ei}}$: is the weight coefficient related to each fitness function

The $\mathrm{FTF_1}$ from Table 3 is selected as an example to explain the way used to formulate the four multi-objective fitness function (FTF). The $\mathrm{FTF_1}$ involves two fitness functions ($f_1=BW_{3dB}$ and $f_2=A$) and it can be given to maximize the overall gain and frequency bandwidth of the TIA. Therefore, the function ($\mathrm{FTF_1}$) is written as $\mathrm{FTF_1} = BW_{3dB} \times \mathrm{W_{e1}} + A \times \mathrm{W_{e2}}$. Where $\mathrm{W_{e1}}$ and $\mathrm{W_{e2}}$ are the weight coefficients of the bandwidth at -3 dB and the open loop gain of the common source amplifier respectively.

3.4. Genetic algorithm results and discussion

The primary parameters related to the TIA design and performance are studied, harnessing various fitness functions formulated based on genetic algorithm. Table 4 shows the optimum finding of the variables obtained through applying four multi-objective fitness functions. A 0.18 μm channel length (L_1) is used for the $\mathrm{M_1}$ CMOS transistor in all simulation routines.

Table 4. Genetic algorithm optimum parameters for TIA circuit.

Variable parameters	$\mathrm{FTF_1}$	$\mathrm{FTF_2}$	$\mathrm{FTF_3}$	$\mathrm{FTF_4}$
I_D (mA)	1.7	2.6	1.8	2.2
R_F (Ω)	500	400	410	390
R_D (Ω)	840	530	800	630
W_1 (μm)	9	12	14	10.5

The resulting multi-objective fitness function parameters were examined in the TIA and photoreceiver circuits and the corresponding findings are tabulated in Table 5. The preamplifier circuit was realized in advanced design system (ADS) software from Keysight technology with a standard characteristic impedance of 50 Ω.

Table 5. Genetic results for desired specifications of design 0.18 μm CMOS OEIC.

Optimized Parameters	Desired specifications	$\mathrm{FTF_1}$	$\mathrm{FTF_2}$	$\mathrm{FTF_3}$	$\mathrm{FTF_4}$
V_{DD} (V)	1.8	1.8	1.8	1.8	1.8
BW_{3dB} (GHz)	Max.	7.7	15.7	10.6	13.8
Z_T (dBΩ)	Max.	40	40.3	40.2	~39
IRN (pA/√Hz)	Min.	8	9.7	11	10
Delay group, τ_d (ps)	Min.	9	7.6	10.6	6.2
DC Power consumption (mW)	Min.	3	4.6	3.3	~3.9

It can be observed that each fitness function has improved certain performance parameters. Since the high frequency response of the amplifier is strongly

dependent on feedback resistor (R_F), the highest R_F value of 500 Ω used in FTF_1 contributed to a reduction in the frequency bandwidth. In general, the input referred noise current, DC power consumption, transimpedance gain of the preamplifier and M_1 channel width are constrained at certain reasonable values. Among the fitness function results, no significant difference was noticed for the DC power consumption. The prominent FTF_2 result does not only lead to maximizing the bandwidth at -3 dB but also to an enhancement of the TIA gain. As a standpoint, FTF_2 provides a significant improvement on the overall frequency response in comparison with other functions.

Figure 3 shows the simulated transimpedance gain response of the TIA employing FTF_2 extracted parameters without the integrated peaking inductor. A 40 dBΩ overall gain was attained along with a ~22 GHz electrical bandwidth (i.e., the bandwidth of the TIA), reflected from the advantage of a single stage amplifier. The TIA findings correspond to a transimpedance gain-bandwidth product of 2.2 THzΩ, which is an outstanding result for a single stage CMOS based preamplifier circuit. The downside of the multistage amplifiers comes from the associated capacitances introduced by integrated transistors and are often loaded on each other, which in turn reduces the -3 dB bandwidth. For the photoreceiver circuit, the large fully depleted capacitance of the photodiode may have a detrimental impact on the frequency bandwidth.

A peaking inductor technique is thus necessary to extend the ultimate optical bandwidth (BW_{3dB}). Note that a reasonable series peaking inductor (L_p) of 2 nH was exploited in the simulation, extending the BW_{3dB} into 15.7 GHz for the FTF_2 function while sustaining a moderate group delay response, τ_d as well. The small variation in τ_d over the operating frequency is of pivotal prominence to accommodate the high-speed data rate system requirements. The group delay response as a function of frequency is depicted in Fig. 4. The simulation data revealed that τ_d varies from 8 to 15.6 picosecond and is practically capable of supporting 30 Gb/s optical data rates.

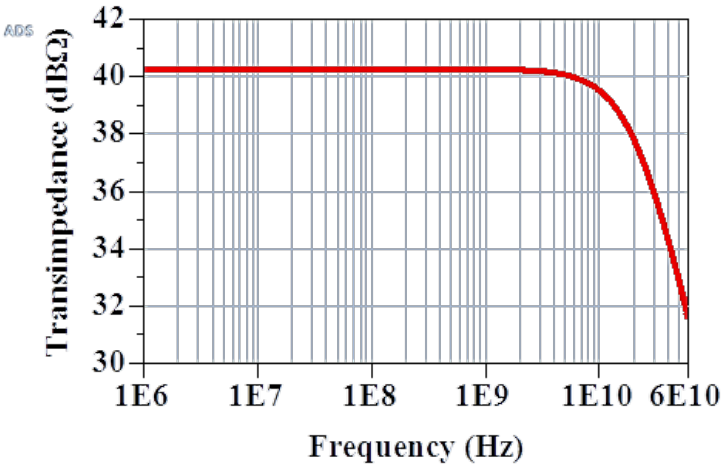

Fig. 3. Transimpedance gain response of the TIA circuit as a function of frequency.

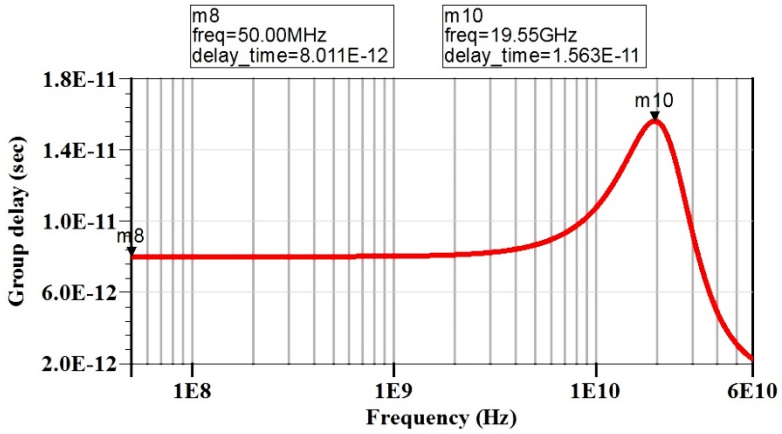

Fig. 4. Group delay variation obtained for the TIA circuit with 2 nH peaking inductor.

The metric measures in assessing an OEIC receiver performance do not solely lay at the BW_{3dB} and group delay parameters, as the referred noise response must also be taken into account, ensuring that the integrated circuit introduces as low noise as possible. Figure 5 shows the input referred noise current (IRN) of the TIA extracted from $V_{out.Noise}/Z_T$, being $V_{out.Noise}$ the simulated output voltage noise. With the use of FTF_2 optimized parameters, a low IRN of 9.7 pA/√Hz was attained at the operating frequency of 15.7 GHz. The achieved input referred noise current in this work is much lower than those reported in [18, 30], highlighting the usefulness of the genetic algorithm results extracted here.

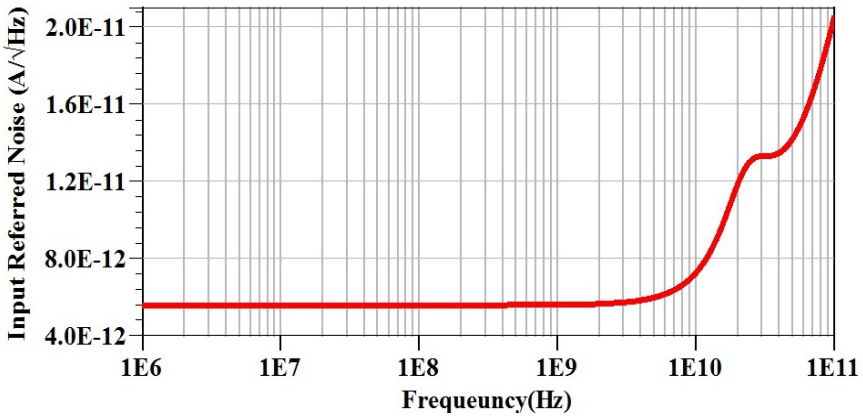

Fig. 5. Input referred noise current density versus frequency.

The shunt-feedback TIA amplifier incorporates the PIN-photodiode equivalent circuit to realize the whole photoreceiver circuit. A detailed analysis of the sophisticated photodiode circuit, highlighting how the input laser is converted into a corresponding photocurrent, a 50fF junction capacitance and other associated parasitic components were previously discussed in [37]. Figure 6 illustrates the

behaviour of the relative optical response for various fitness functions (FTF_1, FTF_2, FTF_3, and FTF_4).

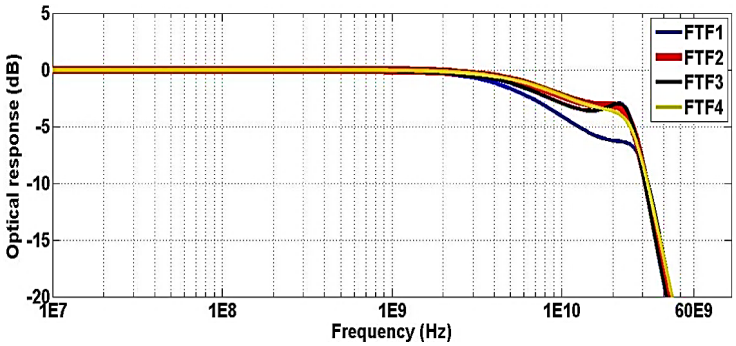

Fig. 6. Relative opto-electrical response for four fitness functions.

The schematic diagram realization using advanced design system (ADS) of the proposed Transimpedance amplifier with the necessary measurement setup to record the opto-electrical bandwidth (BW_{3dB}) is illustrated in Fig. 7.

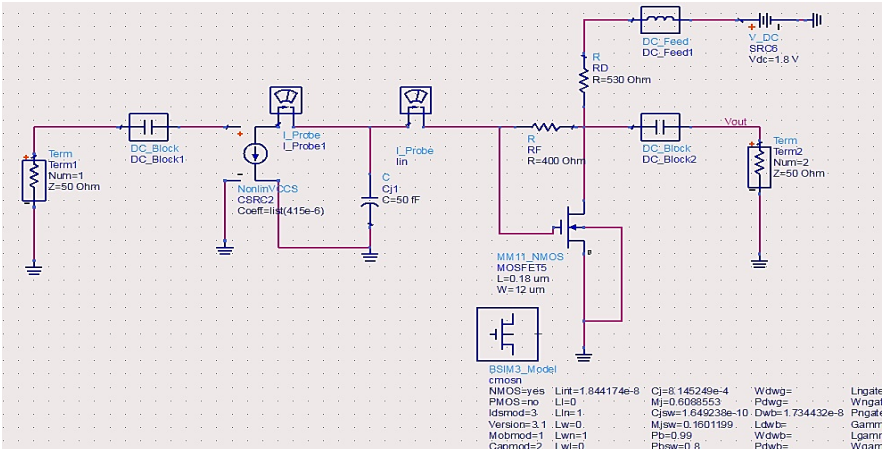

Fig. 7. Schematic of the OEIC circuit in ADS used to obtain the simulated opto-electrical bandwidth.

Figure 8 presents the relative optical result of the ultimate photoreceiver for fitness function number two (FTF_2). As reported earlier that FTF_2 outperforms other fitness functions, providing a significant improvement on the optical response and overall parameter performance. Theoretically, the obtained opto-electrical bandwidth (15.7 GHz) can support an optical system switching at a speed of 20 Gb/s. An embedded bit-stream generator with associated simulation tools was used to assess the photoreceiver performance when transmitting a random bit stream binary code pattern with a length of 2^{15}-1. The simulated eye diagram at a bit rate of 20 Gb/s is shown in Fig. 9. An open eye diagram can be observed without introducing inter-symbol interference (ISI) distortions. Additionally, the results exhibit a trivial overshoot and/or undershoot distortion and the evaluated root mean square jitter of the overlapped bit stream is 4.2 ps. The open eye width which

exceeds 27 ps with an amplitude of ~55 mV, validates the achieved BW_{3dB} for satisfying a 20 Gb/s data rate optical communication system requirement.

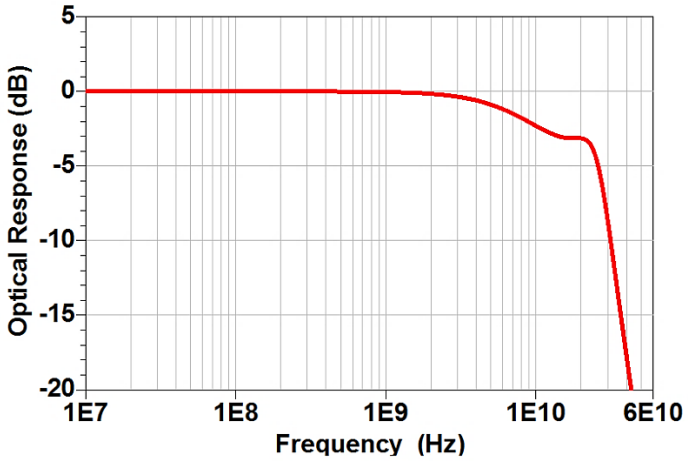

Fig. 8. Relative response of the simulated photoreceiver designed based on GA (FTF_2 fitness function parameters).

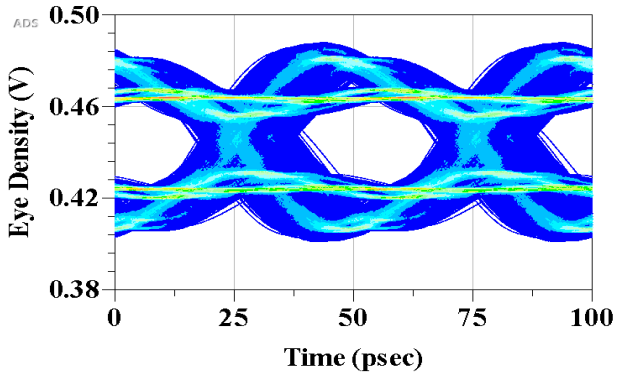

Fig. 9. Eye diagram obtained for the ultimate circuit at a data rate of 20 Gb/s using random bit stream pattern with a binary code length of 2^{15}-1.

In contrast to the genetic algorithm environment developed throughout this study, there are numerous reported works in the literature focusing on photoreceiver based CMOS as illustrated in Table 6. The core benefit presented here laid on exploiting a single stage front-end amplifier circuit, translating into a reduction in the final chip dimensions without sacrificing in the transimpedance gain, frequency bandwidth, group delay response, noise performance and other related parameters.

For an inclusive comparison with other relevant works in the literature, a figure of merit (FoM) formula is proposed based on BW_{3dB}, Z_T, IRN and DC power consumption as given by Eq. (14):

$$\text{FoM} = \frac{BW_{3dB}(\text{GHz}) \times Z_T(\text{dB}\Omega)}{\text{IRN}\left(\frac{\text{pA}}{\sqrt{\text{Hz}}}\right) \times P\ (\text{mW})} \tag{14}$$

Since the aim is to maximize both the BW_{3dB} and Z_T as well minimizing the DC power consumption and noise, the formula numerator is the product of BW_{3dB} and Z_T, whereas the denominator represented the product of IRN and DC power consumption. It is expected that the higher FoM value, the better the amplifier overall performance involving the trade-off among all the important parameters. From Table 6, the optimized TIA parameters contributed to the highest FoM value outperforming relevant amplifiers reported in state of the art in terms of wide BW_{3dB} and high transimpedance gain with maintaining low input refereed noise current and DC power consumption.

Table 6. Comparison results of genetic algorithm used in this study with the recent reported work.

	[18]	[26]	[38]	[39]	[40]	[41]	[42]	This work
Technology	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
C_D (fF)	N/A	N/A	50	250	200	50	50	50
V_{DD} (V)	1.2	1.8	1.8	1.8	1.8	1.8	1.8	1.8
BW_{3dB} (GHz)	15.4	7.9	7	8.5	7	6.03	5.35	15.7
Z_T (dBΩ)	50.6	50.8	54.3	51.7	55	54.3	53.4	40.3
IRN (pA/√Hz)	20	7.7	5.9	10	17.5	10.7	8.15	9.7
Delay group, τ_d (ps)	N/A	N/A	26	N/A	N/A	42	N/A	7.6
DC Power consumption (mW)	5.3	7.2	29	13.97	18.6	2.33	3.48	4.6
FoM	7.35	7.23	2.22	3.14	1.18	13.1	10.07	14

4. Conclusions

A 0.18 μm CMOS transimpedance amplifier integrated circuit was analysed and simulated in this work. The circuit was built in ADS software, highlighting the importance and effect of shunt-feedback parameters on the overall circuit performance. A genetic algorithm with multi-objective fitness functions was developed to extract the optimized circuit parameters, including the channel width of the transistor and other associated resistors. This has helped to effectively balance the common trade-off between the -3 dB bandwidth and transimpedance gain of the preamplifier. A decent gain of ~40 dBΩ with an optical frequency bandwidth exceeding 15 GHz was achieved by integrating a 2 nH peaking inductor, which is adequate for over 20 Gb/s data rate operation. Furthermore, a respective low input referred noise current and group delay variation of 9.7 pA/√Hz and 7.6 picosecond were obtained. The photoreceiver circuit was then tested with a bit stream pattern length of 2^{15}-1 and showed a clear open eye diagram at 20 Gb/s with no observation of ISI distortion issue.

Nomenclatures

A	Open loop gain of the common source amplifier
BW_{3dB}	Bandwidth at -3 dB, Hz
C_D	Photodiode capacitance, F
C_I	TIA input capacitance, F
C_{OX}	Capacitor per unit area of the gate oxide, F/m^2
C_T	Total input capacitance, F
g_m	Transistor's transconductance, S
I_D	Derain current of the transistor , A

$\overline{I_{in,n}}$	Input refereed noise current, A/√Hz
I_P	Photocurrent, A
L_1	Channel length of the transistor, m
L_{SP}	Series peaking inductor, H
P	DC Power consumption, W
Q	Quality factor
R_D	The resistance at the drain of the transistor, Ω
R_F	Feedback Resistance, Ω
V_{DD}	Drain voltage, V
W_{ei}	Weight coefficient
W_1	Width of the transistor, m

Greek Symbols

τ_d	Group delay, Sec.
μ_n	Electron mobility, $m^2/V.$ s

Abbreviations

ADS	Advance Design System
CMOS	Complementary Metal-Oxide Semiconductor
CS	Common Source
EPON	Ethernet Passive Optical Network
FoM	Figure of Merit
FTF	Fitness Function
GA	Genetic Algorithm
HZ	High Impedance
IRN	Input Refereed Noise current
ISI	Inter Symbol Interference
MATLAB	Math Laboratory
NRZ	Non-Return-Zero
OEIC	Optoelectronic Integrated Circuit
PRBS	Pseudo Random Bit Stream
TIA	Transimpedance Amplifier

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