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HIGH SPEED SIGMA DELTA A/D CONVERTER FOR DIGITAL COMMUNICATION SYSTEMS

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Abstract

The high advancement in modern electronic equipment led to the meet for high-efficiency analog to digital (A/D) convertor used for various digital communication systems this convertor must have special characteristics like high speed, low quantization noise, good spectral shaping, and efficient power density. Sigma delta (ΣΔ) modulation is a coding process used to enhance the resolution of a sampled data result from low resolution sampled sequence measurements. Usually, main three processes are employed to increase the resolution, the first step is oversampling to produce the correlated samples, the second step is feedback to shape the noise spectrum, and finally filtering to remove all the out-of-band spectrum harmonics. In this paper, three types of sigma-delta modulation were designed,2nd, 3rd, and 4th order modulator. It is found that increasing the order of the modulator led to improving the overall performance of the system also using high sampling frequency will increase the resolution and reduce out of band harmonics in the 1st and 2nd modulation order.

Keywords: Decimation filter, Incremental ADC, Oversampling converters, SNR, ΣΔ ADC; ΣΔ Modulator.

1. Introduction

Analog to Digital (A/D) converter is openly used in advanced digital electronics circuits like digital communication, video and computer and many other applications [1]. The main objective of A/D convertor in to improve the speed spectrum of different computer and electronic circuits related to this computer and also reduce the total consumed power inside the circuit as well as to produce high precision electronics digital communication circuit [2, 3].

The three basic concepts behind the sigma delta (ΣΔ) A/D converters are the oversampling, noise shaping and the decimation digital filter. The Analog to Digital Convertor (ADC) simple operation is executed as oversampled the input signal first and severally quantized inside the modulator loop, and then filtered, low pass filter (LPF) and decimated to the Nyquist rate. The characteristics are well known: the possibility of efficient circulation quickly for accuracy and conformance requirements is drawn on analogue components. By Nyquist-rate or oversampled converters can be described.

The organization of the manuscript is as follows: Section 2 introduces types of A/D convertor depending on Nyquist-rate and oversampling. While second and third order sigma delta modulation systems are illustrated in Sections 3 and 4, respectively. Higher order sigma delta converter for digital communication systems is described in Section 5. In addition, simulation results and analysis study are presented in Section 6. Finally, Section 7 includes the main conclusions of the work.

2. Analog To Digital Converters Types

There are two type of A/D convertor depending on its principle of operation that whether it's depends on Nyquist-rate or oversampling. In the first type the signal which is fed to input of the digital circuit is sampled at $f_{samp} \geq f_{in}$ as shown in Fig. 1 [4]. To achieve high-accuracy conversions it depends on excessive modulation and noise formation: Nyquist-rate ADC, the signal to quantization noise ratio (SQNR) improvement by increasing the resolution (denoted by N) of the analog to digital convertor.

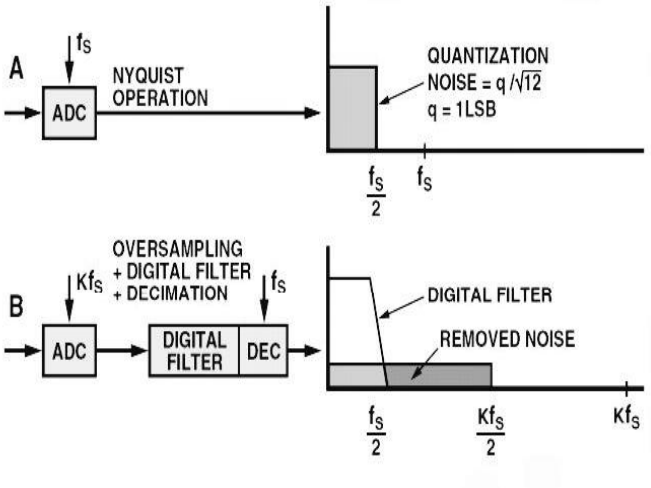

Fig. 1. Nyquist-rate and oversampling ADCs [4].
(f_{samp} is sampling frequency, while f_{in} is input frequency.)

There is a little difference in working between the Nyquist-rate ADC and the ΣΔ ADC. Two parameters play an important role in these differences which are the oversampling one and the noise shaping which decide the amount of noise inside the sampled signal. If the sampling ratio (SR) has a value more than unity than the system is denoted by Over Sampling Ratio (OSR) ADC as shown in Fig. 1(B) [5].

3. Second Order ΣΔ Modulation

The basic second order ΣΔ modulator ADC is used frequently. This modulator achieves, satisfies the z-domain equation.

$$W(z) = K(z) + S(z)(1 - 2z^{-1} + z^{-2}) \quad (1)$$

where: *W*, *K* and *S* are the Z transforms of the output, input signal and the quantization error process, respectively. The first order modulator noise transfer function (NTF) along with the NTF for the second order modulator [6].

Comparing the second order ΣΔ NTF with the first order NTF It turns out that the first order provides less quantization noise restraint over the low signal band frequency. Less noise power is shifted outside the signal band out the bandwidth of the signal if compared with a 2nd order ΣΔ. The second order modulator structure is show in Fig. 2.

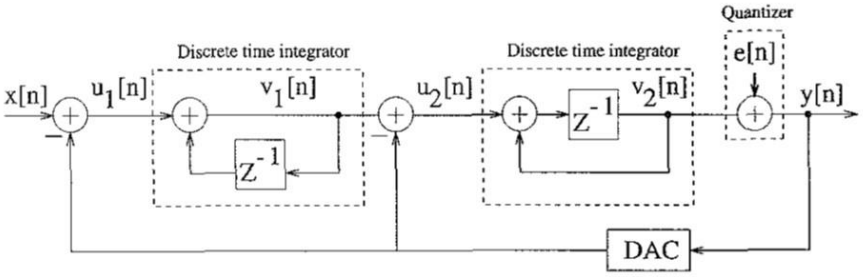

Fig. 2. Second order ΣΔ modulator [7].

The two integrators realizing the structure as shown in Fig. 2 [7]. The signal transfer function of the first one is $1/1\text{-}z^{-1}$ and that of the second one is $z^{-1}/1\text{-}z^{-1}$. If an ideal lowpass is used to filtered modulator output, the signal to noise ratio can be calculate as shown

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L + 10)\log\left(\frac{f_s}{2f_B}\right) \quad (2)$$

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^4}{5}\right) + 50\log\left(\frac{f_s}{2f_B}\right) \quad (3)$$

Again, letting $\frac{f_s}{2f_B} = 2^r$, power is (σ_x^2), L represents the modulator order, then:

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^4}{5}\right) + 15.05r \quad (4)$$

Subsequently, signal to noise ratio (SNR) develops by 15 dB or the equivalent accuracy by 2.5 bits for each increase in r, which is 1-bit better than the development accomplished by a 1st order ΣΔ, its variance σ_e^2 or power [8].

4. Third Order Sigma-Delta Modulation

In order to produce a single without noise power or this noise be out the bandwidth of the signal which result a high accuracy and low noise output system, this can be done using high order noise transfer function (NTFs).

Instead, to get the same accuracy for a given signal bandwidth a low sampling-rate can be used [9]. In this case, the velocity requirements on the analog devices are reduced. A straightforward extended of the first order sigma-delta a signal transfer function given by $H_x=z^{-1}$ and a noise transfer function given by $H_e=(1-z^{1})$ M which includes M zeros at z=1 an order M modulator based on it. By using the second order structure of Fig. 3 and adding an integrator with signal transfer function (STF) $1/(1-z^{-1})$ between the summer node input and the first integrator of the second order modulator and thus can be configured a third order modulator.

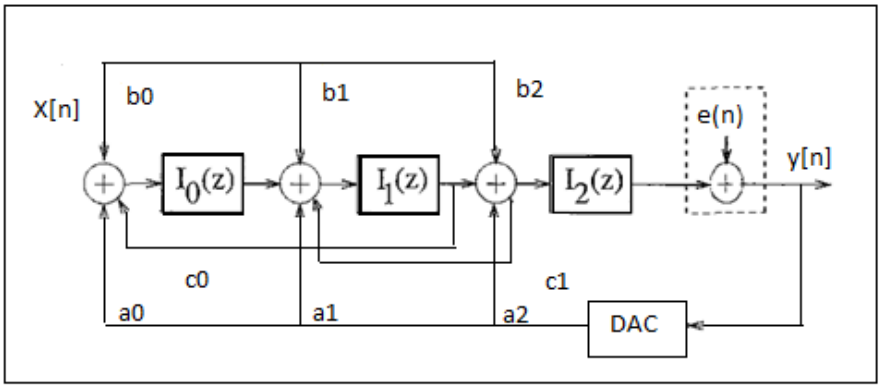

Fig. 3. Third order modulator topology.

The input to the additional integrator is x[n] subtracted from y[n] and the -y [n] it's the new integrator output which is fed as the entry for the feedback.

The Noise transfer function (NTFs) of the third order modulator gives more quantization noise attenuation than the lower modulator orders and more ability to drift the noise to high frequencies away from the interest band [10].

The optimum signal to noise ratio (SNR) within the range achieved by a third order modulator is obtained by:

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^6}{7}\right) + 70\log\left(\frac{f_s}{2f_B}\right) \quad (5)$$

Let $\frac{f_s}{2f_B} = 2^r$, Eq. (5) will be:

$$SNR = 10\log(\sigma_x^2) - 10\log(\sigma_e^2) - 10\log\left(\frac{\pi^6}{7}\right) + 21.07r \quad (6)$$

The third order modulator provides an enhancement of SNR (21) dB for each double in the Over Sampling Ratio (OSR) and the same thing to the resolution bits also enhanced by (3.5) bits.

This new modulator as example needs frequency of input signal (f_B), order of modulator (r) and sampling frequency (fs) of 10.24 MHz to convert a signal of a 20 kHz to 23-bits resolution [11].

5. Higher Order ΣΔ Converter for Digital Communication Systems

The 2nd order ΣΔ of noise shaping cannot give the high accuracy if the oversampling ratio is small, so this low accuracy value can be avoided by using another integrator inside the system [12]. Also, the stability of the overall system can be sufficient because the comparator used in the circuit has usually non-linear characteristics.

Therefore, most designs rely on multiple cascaded 1st and 2nd order ΣΔ converters as an alternative scheme to achieve high order noise shaping. This scheme is known as MASH or cascading ΣΔ ADC convertor.

6. Simulink Modulator Designs

In this section, Fig. 4 shows the proposed ΣΔ modulator used in this paper which includes of a ΣΔ modulator and filtering system which simulated in MATLAB software [13].

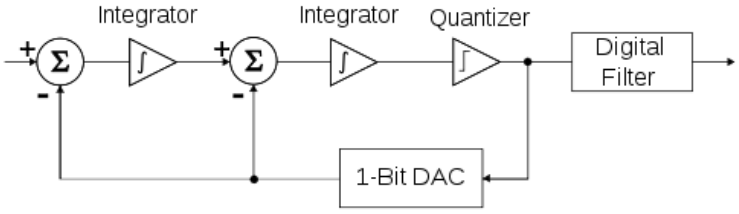

Fig. 4. Design of ΣΔ analog to digital system.

The 2nd order ΣΔ modulator MATLAB model as show in Fig. 4 consists of many digital blocks like integrator, subtractor, quantizer and filter [14]. Table 1 explain the sigma-delta for characteristics of the modulator. A 20-bit for a signal band of 40 kHz is designed in program Simulink.

Table 1. Sigma-Delta for Characteristics of the Modulator

ADC Parameters	Values
Signal bandwidth	40 kHz
Sampling Freq.	40.96 MHz
Over-sampling Ratio	512
Order of Modulator	2
Modulator Bits No.	$B_{mod} = 1$
Filter Output Bits No.	B = 20

The aim is to produce output signal with high-resolution so that the signal to noise ratio (SNR) will be increased as a result. On the other side, it is important to omit the quantization noise from the signal received from the modulator at high frequencies. Therefore, a pass filter is designed to eliminate this noise at high frequencies, as well as to pass the input signal without distorting it. Table 2 shows the specific filter characteristics for noise removal and modelling frequency reduction.

The decimation filter characteristics of OSR 512 is consist of sampling frequency (40.96) MHz, the down sampling ratio is 512, the pass and stop band frequency are 40 kHz and 42 kHz respectively [15].

It's clear from Table 2 that the cut-off frequency of the proposed filter is 41.87 kHz which is sufficient for passing an input signal with a 20 kHz bandwidth and without distortion. In practical terms, it is not possible to implement single filter operating with the mentioned specifications. The filter operates at a high modelling frequency because the order of the filter is very high, therefore more than one filter must be used to improve the performance of the system, as shown in Fig. 5.

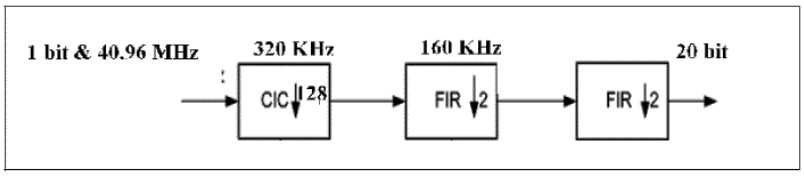

Fig. 5. Decimation filters architecture.

As shown in Fig. 5, the designed filter in this paper consists of three consecutive filters, they are: second order Cascaded Integrator Comb (CIC) filter and two finite impulse response (FIR) filters. CIC filter is used to reduce the sampling frequency by 128 and at the same time to make the output bits 20 bits, also to remove noise at high frequencies [16]. Modelling frequency is reduced by (4) using pulse-specific response filter. The order of the 1st filter was 18, while the rank of the 2nd filter was 150. Filters that operate on a high sampling frequency are practically costly if the filter level is high [17], so the first filter order was chosen to small value [18], so that it works on a high sampling frequency of 320 kHz. On the other hand, the second filter with order of 150 will operate at a lower sampling frequency which is 160 kHz, and this led to reduce the high frequency noise which results in increasing the accuracy of the proposed circuit for digital communication system.

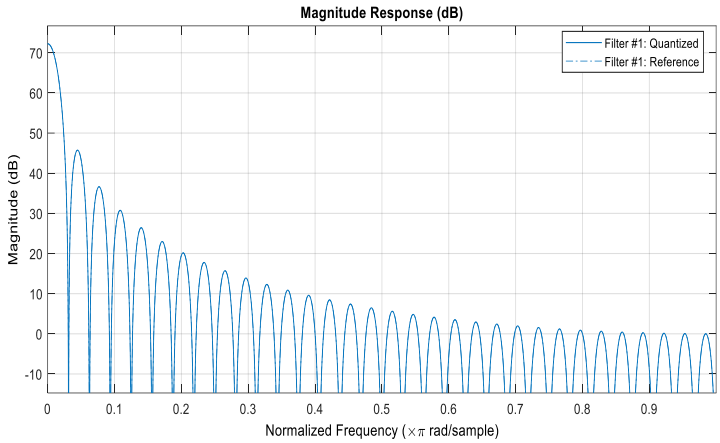

Fig. 6. Third order CIC filter frequency response.

The bit resolution effective number of bits (ENOB) for the design of CIC filter which is needed to make sure that no runtime overflow happens is given by Eq. (7) [18].

ENOB = (1-bit sign) + (no. of input bits) + (no. of stages, N) $\log_2$ (Decimator factor). In this work,

$$ENOB = 1 + 1 + 2 \log_2 (512) \quad (7)$$

That's mean ENOB=20, A (1-bit sign +19 resolution bits) digital output is the output from the (CIC) decimation filter. the magnitude droop in (CIC) filter is achieved by the FIR filters using to control the frequency response correction. The proper FIR filters order is 15 and 180 [19], As shown in Fig. 7.

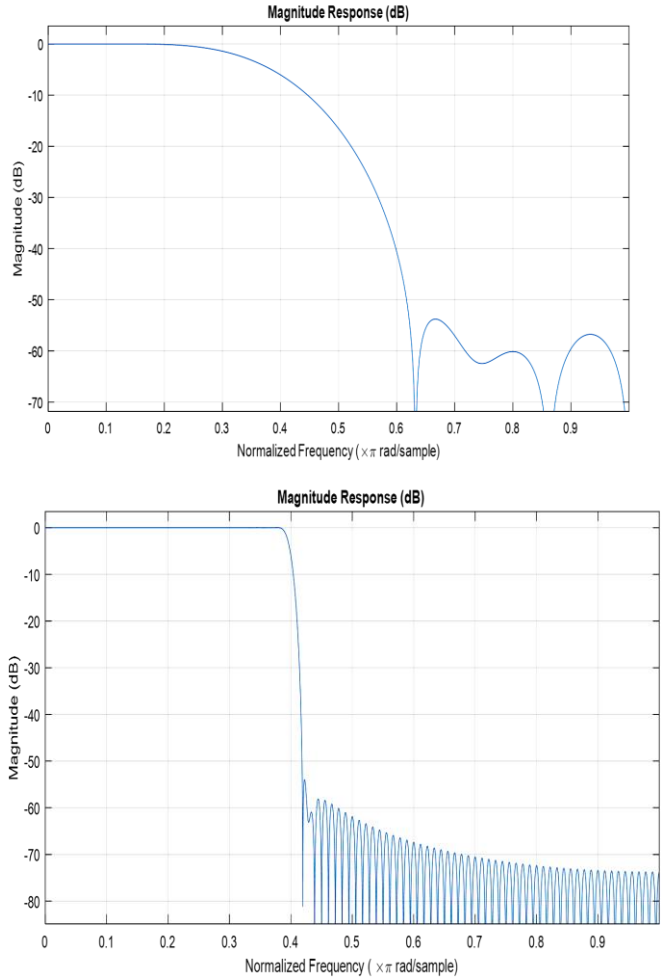

Fig. 7. FIR filters frequency response.

The spectrum analyser is used to display the spectrum of the signal from the A/D converter type ΣΔ. As shown in Fig. 8, the spectrum plotting of the digital signal is coming out from the converter [20].

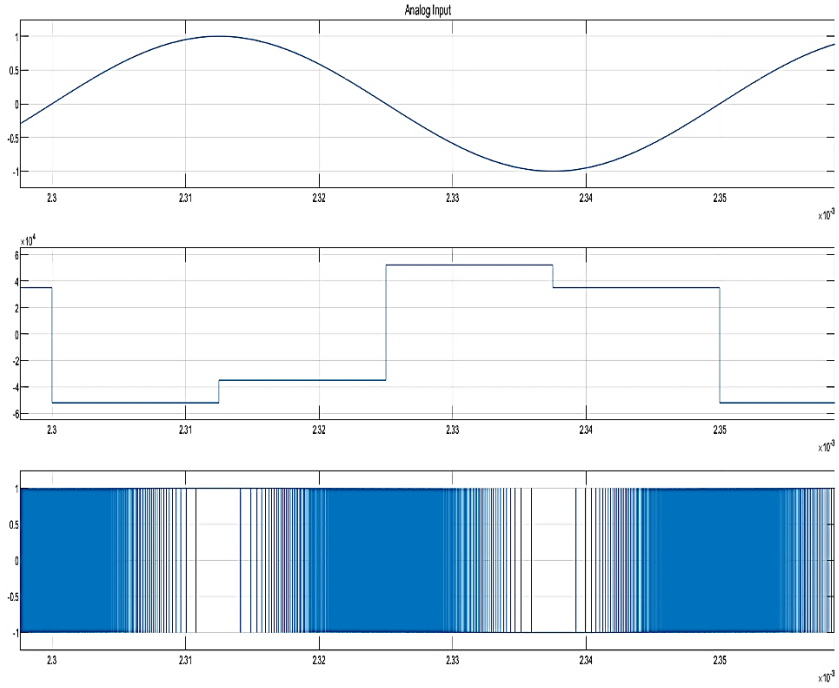

Fig. 8. 2nd order transient response (20 kHz).

It is also shown from Fig. 8 that it includes a ΣΔ modulator that converts the input signal to the pulsed modulation code signal [21]. It can be show from Fig. 8 that the number of "1" increases at the positive peak of the input sinewave, while the number "-1" is more in the negative peak, and there is an equal number of "1" and "-1" at the zero parts of the wave [22]. The spectrum analyser was used to display the designed built-in signal output spectrum. Figure 9 shows power spectral density (PSD) of First FIR Filter Output Signal Spectrum by OSR of 2 designed in the MATLAB and shows the modulation characteristic of the modulator.

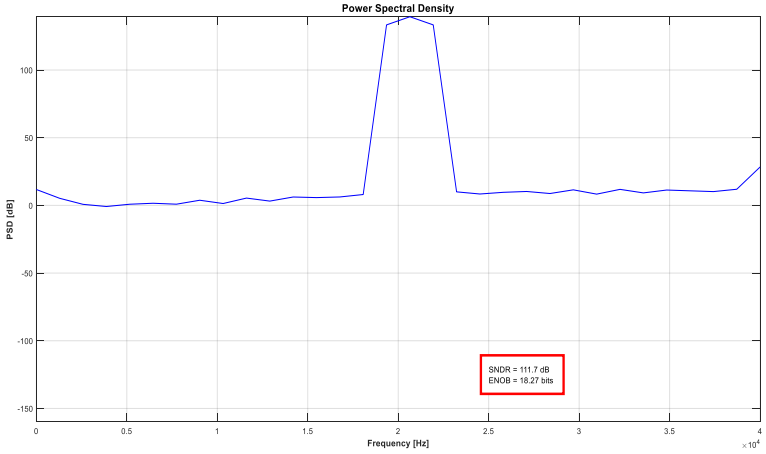

Fig. 9. PSD for the first FIR Filter output signal spectrum by OSR of 2.

It is noted that the main signal bandwidth has small quantization noise because this noise was happening outside the main signal region. The modulator output has an 85.6 dB signal to noise ratio at 512 Over Sampling Ratio, while the value of ENOB is 13.92 bits as shown in Fig. 9.

The simulation results show in Fig. 10 that the S/N is improved to a value equal to 116.5 dB with a frequency equal to 20 kHz which is considered as a good value that give the better accuracy, the value of ENOB is about 19.06 bits.

As summary, as explain from Table 2, there are a difference between the accuracy and the signal to noise ratio, for several modulator designs.

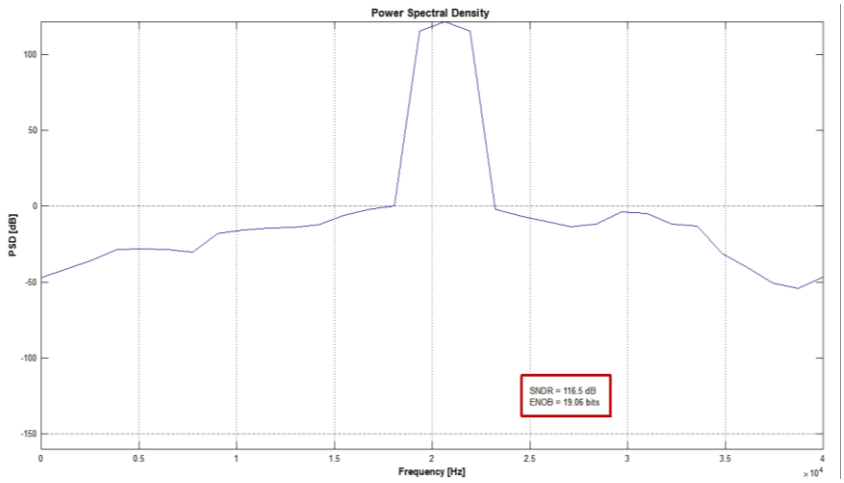

Fig. 10. ΣΔ Output power spectral density (PSD) at 40.96 MHz.

Table 2. Comparison of converters parameters.

	First Modulator	Second Modulator	Third Modulator	Fourth Modulator
Sampling Frequency (*fs*)	10.24 MHz	20.48 MHz	20.51 MHz	40.89 MHz
Modulator Order	1st order	1st order	1st order	1st order
CIC Order	2nd order	2nd order	3rd order	3rd order
SNR	67.5 dB	84.3 dB	106.9 dB	116.5 dB
ENOB	10.92 bits	13.71 bits	18.01 bits	19.06 bits

It's clear from the Table 2 that the improvement in accuracy depends on the *fs* of the modulator, the improvement in accuracy appears clearly when increases the *fs* in the first and second modulator [23]. In addition, also it can be observed that the increase in accuracy depending on the modulator's order, it can also be observed that the signal to the noise ratio for all the proposed designs was good and acceptable [24, 25]. The extent of exploitation of the implementation for third and fourth modulator filter is greater than the rest of the filters because of the CIC filter order.

7. Conclusions

Sigma delta modulators for digital communication system were investigated and studied in this paper. Different applications are employing and use sigma delta ABC with various specifications. For communication application and low-resolution voice data it is better to use single loop sigma delta. On the other side, the applications require sensors and portable devices to improve the accuracy and reduce the power of Sigma Delta ADCs. It is noticed that the signal to noise ratio for the proposed system for 2^{nd},3^{rd} and 4^{th} order modulator was good and acceptable.

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