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LEVEL-UP/LEVEL-DOWN VOLTAGE LEVEL SHIFTER FOR NANO-SCALE APPLICATIONS

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Abstract

Multi supply voltage domain is an ultimate approach for reducing power consumption at system level. To interconnect multi supply voltage designs, and to prevent static current, the Level Shifters (LSs) need to be employed. The design of LSs with least power consumption and delay performance are the primary design constraints. In this research, a new architecture voltage level-up/level-down shifter for Nano-scale applications has been introduced with short circuit aware Complementary Metal Oxide Semiconductor (CMOS) logic, which executes level shifting operation with lower power consumption and delay. The designed circuit is useful to shift from as low as 0.2 V to 1.2 V and vice versa. Apart from operational range, the performance matrices like power, delay, and duty cycle of the circuit were optimized to meet the demands of nano scale applications. The proposed LS simulated using Synopsis tools at 90 nm technology. From the results, it has been observed that, the average "level-up" and "level-down" shift active power consumption is 9 nW and delay 1.5ns at 1 MHz signal frequency. The strength of the design has examined with different load and working conditions. The area occupied by the proposed design from the post-layout simulation is 5.87 μm^2.

Keywords: Area, Delay, Level shifter, Multi-VDD systems, Nano-devices, Power consumption.

1. Introduction

The wide performance requirements of nanoscale devices demand the extreme operating voltages. Different computational performance can be obtained by different operating voltages, leading to the development of multi supply system approach [1]. In CMOS design, lower power supply voltage is an efficient practice to lower the power consumption. This is because it results in a quadratic relation of dynamic power consumption, as per Eq. (1), and the leakage power is governed by exponential law. However, lowering the power supply voltage will degrade the delay. To lower the dynamic, leakage powers and to maintain the required propagation delay, a multi supply system approach is the ultimate solution; it uses multiple power supplies, which use more than one power supply voltage to meet the required power and delay constraints [2].

$$P_d = CV^2 f \tag{1}$$

In multi supply system, the logic gates on the noncritical paths can be operated with low VDD is called as VDDL and gates on critical path can be operated with high VDD which is called as VDDH to maximise the speed performance. This phenomenon is called as clustered voltage scaling [3]. When a logic '1' signal of VDDL block drives the VDDH logic gates block, the P-Channel Metal Oxide Semiconductor Field Effect Transistors (PMOSFETs) of VDDH operating logic gate blocks may not become perfectly ON, may become partially ON or weakly ON, hence there will be large static current flow in VDDH logic gates blocks. This will lead to high static power in VDDH logic gate blocks, as shown in Fig. 1. To prevent this, high static current and static power the level shifter (LS) are needed to be used. The LS is an interfacing circuit which shifts the VDDL signal equal to VDDH signal. When a logic '1' signal of VDDH gates block drives the VDDL logic gates block, MOSFET of logic gate blocks become partially ON or weakly ON, hence no level shifter is needed and even if required, cascading of inverters are enough but additional circuits are needed.

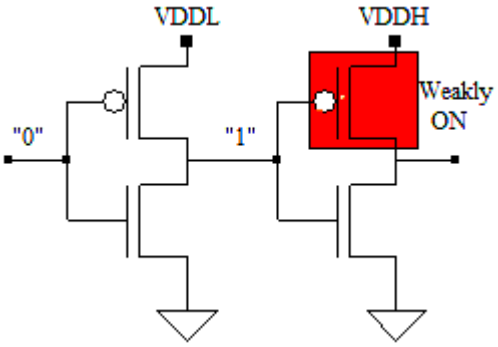


Fig. 1. Cascading of inverters.

However, the use of LSs induces the area overhead with some LS Power consumption and LS delay. The primary challenge in multi VDD system is designing efficient LS to reduce the overheads cause by the inclusion of LSs. In this research we have introduced novel LS, which utilize CMOS topology to design new LS. The introduced "Level-up/level-down Voltage Level Shifter (VLS) for

nano scale applications" performs "Level-up" or "Level-down" shifts based on input voltage (VIN). The remaining chapters are organized as follows. A detailed survey on existing LSs have been discussed in the chapter II, chapter III describes about proposed LS, simulation results are described in chapter IV, and finally the paper is concluded with conclusion chapter.

2. Review on existing LSs

A basic form of a LS is "Differential Cascade Voltage Switch Logic" (DCVSL) LS which is depicted in Fig. 2; the two PMOSs MP2 & MP3 is considered as a "cross-coupled" load. When input VIN is in transition there is a possibility that either MN2 and MP2 or MN3 and MP3 are partially ON. Hence, there may be high dynamic power consumption in this kind of topology. Dual power supply with dual threshold Voltage with the help of NAND logic is used to achieve VDDL/VDDH is experimented [4]. Using this approach, low VDD is applied as one input while the other input is VDDH. An average of 17 % energy is saved in ISCAS'85 benchmark circuit with 70 nm technology model in that work.

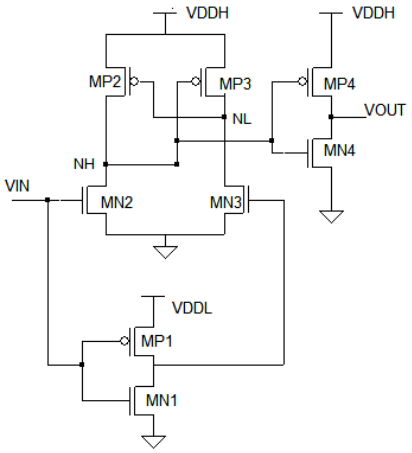


Fig. 2. DCVSL level shifters.

The comparison is done with level shifting logic gates and dedicated level shifters. The DCVSL LS is a ratio circuit which has current contention between MP2-MP3 and MN1-MN2 MOS transistors. As a result "pull-up and pull-down" impedances have to be suitably designed [5, 6]. This circuit is suitable to perform level shifting from threshold level to VDDH, useful to perform voltage level-up or level-down can be done by changing VDDH to VDDL or cascading of inverters are needed to be adopted [7-13].

The LSs [14-16] describe the LSs applications in various applications like IoT, Biomedical and Bio sensors based on the essentiality of LSs in allied applications. The issues pertaining to "Wilson-current mirror-based level shifter" were addressed in [17], which use multi-V_T transistors for attaining wide conversion range. As the focus is on design performance optimization in low voltage operations, the existing work is needed to be optimised for wide range of supply voltages. The LSs in [18, 19] developed using reduced swing inverter, probably which suffers from weak

pull-up and delays are not possible to scale by power supply voltages. In level shifter in [20] is a multi-stage topology that reduces the contention, effectively evades the serious upsizing of pull-down network, which results in increased circuit complexity and delay in comparison with single stage LSs.

The LSs in [21, 22] are also based on DCVSL structure that consumes high static power when the input is stable. However, the current disputation between "pull-up and pull-down" network during output switches is more, which results in more delay and dynamic power, the impact of this is much more when VIN is lower than threshold. Sizing is a very straightforward remedy to stabilise the strength between "pull-up and pull-down" network, which penalties the impractical aspect ratios [23, 24].

Gundala et al. [25] proposed an LS called as : Active Volta Level Shifter" (AVLS) that performs "level-up shift, level-down shift, and blocking". The actual level shifting action takes place by two transmission gates. There is a possibility of both transmission gates ON when VIN equals to VDDL. Hence there may be higher static power consumption at any logic level of its input.

Luo et al. [26] proposed an LS called as "Modified Wilson Current Mirror Hybrid Buffer" (MWCMHB) useful for wide range voltage shifting applications, and incorporated a provision called bidirectional level shifting, balancing transitions, poses current mirror circuit having higher static power consumption, and second stage is a NOR gate with output inverter, employ dual power supplies. Being dual power supplies the routing congestion may occur at physical design. In [11, 27] the source currents are enabled/disabled based on the input transitions, which extensively shrinks the standby power, increase in delay and energy. The LSs proposed in [28-33] have a considerable level of contention between the pull-up and the pull-down circuitry in the logic 'High-to-Low transition' of the VIN leads to increase in delay and power consumption.

3. Proposed Level Shifter

3.1. Basic block diagram

The conceptual diagram of Voltage Level Shifter (VLS) is depicted in Fig. 3. The VDDL and VDDH are the power supply voltages of the Low voltage logic gate module and High voltage logic gate modules respectively. The VLS is a voltage level shifter circuit, which works as "level-up shifter" or "level-down shifter". This interfacing module can also be called as bidirectional level shifter.

The VLS performs shift up when VDDL Module produces logic '1', and down shift when VDDH Module produces logic '1'. In both cases VLS will act as drive circuit.

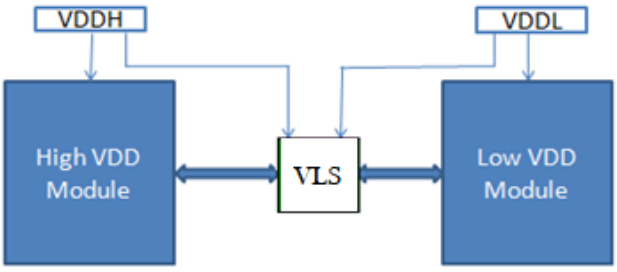


Fig. 3. Basic idea of VLS.

3.2. Circuit description

The proposed design is depicted in Fig. 4. The design utilizes 8 MOS transistors, among which 4 are P-channel MOSs (PMOSs) and 4 are N-channel MOSs (NMOSs). MP1 and MN1 acts as type of level shifting selectors and the remaining transistors performs actual level shifting.

The transistors MP1 and MN1 act as 2X1 MUX. The select signal of 2X1 MUX is input voltage VIN. VDDH and VDDL are two supply voltages having 1.2 V and 0.2 V connected to MP3 and MN3 respectively. Depending on "VIN", either VDDH or VDDL voltage source is selected which will act as virtual bias voltage VDD to the actual level shifter circuit. It is called as 'virtual' because the voltage at VDD is not always constant; it depends on VIN. The possible voltages at VDD are VDDH or VDDL. When VIN =0.2 V then VDDH will be selected and available at VDD, level-up action takes place. When VIN =1.2 V then VDDL will get selected and made available at VDD, level-down action takes place. The analysis of the designed is performed by taking VDDH = 1.2 V and VDDL = 0.2 V. The output of inverter MP2-MN2 is fed as input to inverter MP4-MN4 to avoid static power consumption in MP4-MN4 inverter.

When VIN is 0.2 V, the voltage at VDD is VDDH, the NMOS transistor MN2 turns ON and as MN2 is ON the pull down produces strong logic (VDDH) to the transistor MP2 through feedback & inverter MP4-MN4. Hence strong logic '0' appears at the input of third inverter MP3-MN3. So, MN3 becomes OFF and MP3 turns ON then VOUT get charges to strong VDDH.

When VIN is 1.2 V, the voltage at VDD is VDDL, the NMOS transistor MN2 turns ON and as MN2 is ON, the pull down produces strong logic (VDDL) to the transistor MP2 through feedback & inverter MP4-MN4. Hence, strong logic '0' appears at the input of third inverter MP3-MN3. So, MN3 becomes OFF and MP3 turns ON and then VOUT node will be charged to strong VDDL, which is equal to 0.2 V.

When VIN is 0 V, the voltage at VDD is VDDH, the NMOS transistor MN2 turns OFF and as MN2 is OFF, the pull down produces strong logic '0' to the transistor MP2 through feedback & inverter MP4-MN4. Hence, strong logic '1' appears at the input of third inverter MP3-MN3. So, MN3 becomes ON and MP3 turns OFF and then VOUT node will be discharged to strong '0'.

The Leakage currents of the MOS transistors are influenced by reverse bias current, Gate-Induced Drain Leakage, hot carrier injection and oxide tunnelling, but the dominant component is sub threshold leakage currents which are given by Eq. (2).

$$I_{leakage} = I_o e^{\frac{V_G - V_S - V_{TO} - \gamma V_S - \eta V_{DS}}{\eta V_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)^2 \quad (2)$$

where V_{th} is the thermal voltage, n is the sub threshold swing coefficient constant, η is the Drain-Induced Barrier Lowering coefficient, γ is the linearized body effect coefficient, and I_0 is given by Eq. (3).

$$I_0 = \mu_o c_o \frac{W}{L} V_{th}^2 e^{1.8} \quad (3)$$

However, sub threshold computing is a very effective approach in reducing consumption of energy. However, it affects the performance which gets degraded and also there will be more leakage.

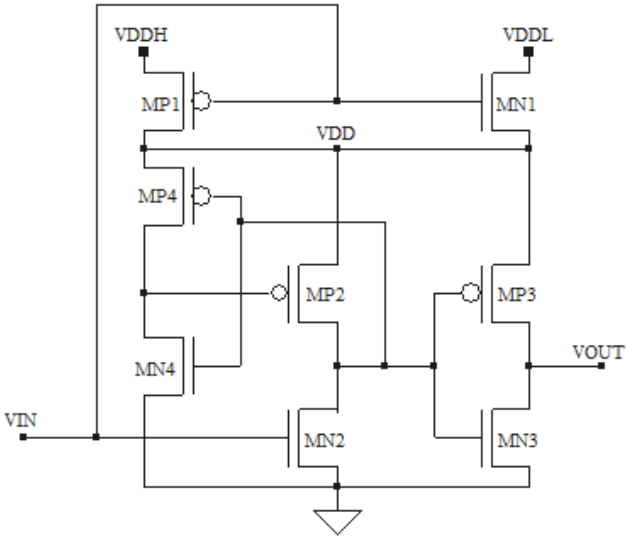


Fig. 4. Proposed VLS.

4. Characteristics of the Design and Analysis

The design has been stimulated by using Synopsis Predictive Technology Model (PTM) model files at 90 nm technology. The W/L ratio of NMOS is 4:1 and PMOS is 8:1 have been maintained. The bias voltages of VDDL and VDDH are 0.2 V and 1.2 V respectively and the load capacitance (C_L) is 40fF is used 1 MHz, 500 kHz and 100 kHz frequencies. As the LSs are key elements in low power applications, it is very much essential to examine its robustness by performing Power analysis, Delay analysis and Load analysis.

4.1. Power analysis

Power consumption by the proposed VLS at "level-up and level-down" is observed at the load capacitance (40fF). Figure 5 shows average power consumption of VLS at level up, as a function of VDDL at constant VDDH = 1 V, and it can be noticed the average power consumption is 16.1nW at 1 MHz. Figure 6 depicts average power consumption of VLS at level down, as a function of VDDH at constant VDDL = 0.2 V, and it can be noticed that the average power consumption is 3nW at 1 MHz.

4.2. Delay analysis

The propagation delay of VLS has been analysed. The delay at level-up and level-down has been observed at the load capacitance (40fF). Figure 7 shows delay of VLS at level up @ VDDL and constant VDDH = 1.2 V and it can be noticed that the delay is 0.4ns. Figure 8 shows delay of VLS at level down @ VDDH and constant VDDL = 0.2 V and it can be noticed the delay is 2.6ns.

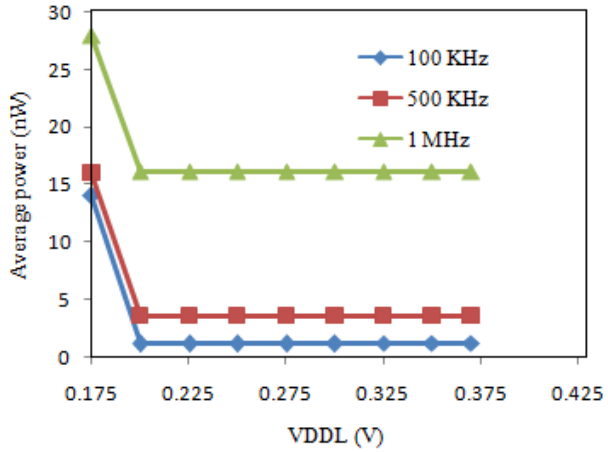


Fig. 5. Average power of VLS @ VDDL and VDDH = 1.2 V.

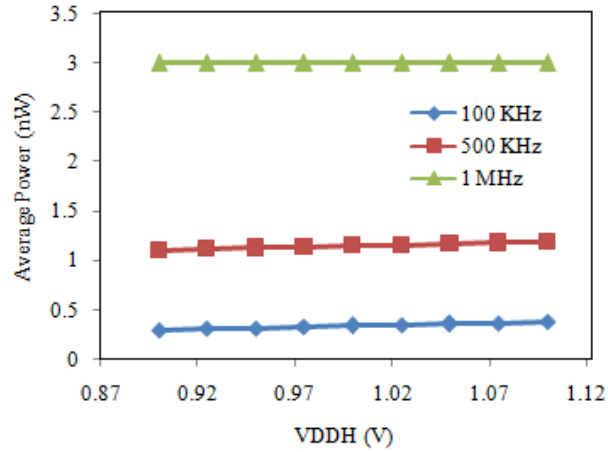


Fig. 6. Average power of VLS @ VDDH and VDDL = 0.2 V.

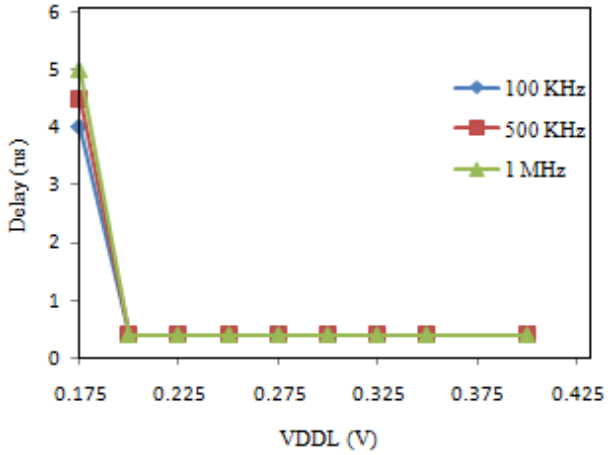


Fig. 7. Delay of VLS @ VDDL and VDDH = 1.2 V.

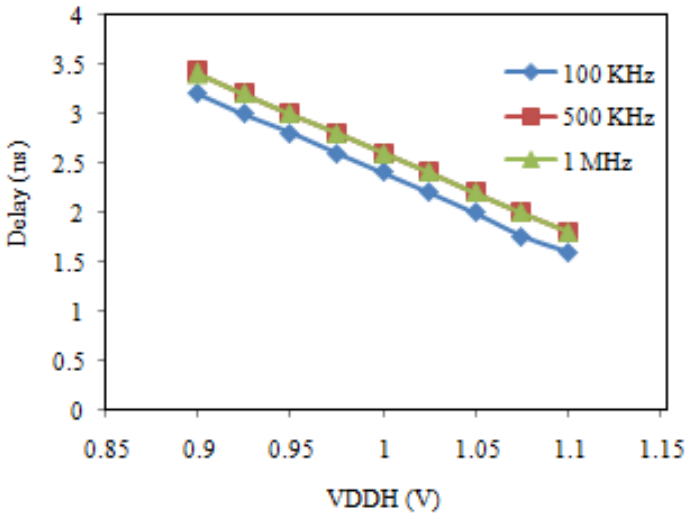


Fig. 8. Delay of VLS @ VDDH and VDDL = 0.2 V.

4.3. Load analysis

The recital of the VLS is studied at varying loads from 10fF to 90fF at the signal frequency of 1 MHz. Figure 9 depicts about average power of VLS while "level-up shift and level-down shift", and Fig. 10 depicts about delay of VLS while level-up shift and level-down shift. It can be observed that the average power and delay of the proposed design are under tolerable limits under varying load conditions.

The fair comparison among all the LSs at different technologies, VDDL and VDDHs and at the signal frequencies of 1 MHz is depicted in the Table 1.

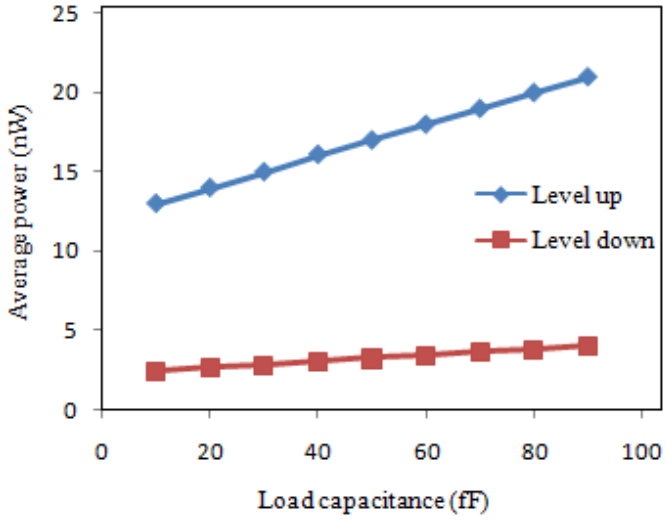


Fig. 9. Average power of VLS @ C_L and VDDH = 1.2 V and VDDL = 0.2 V.

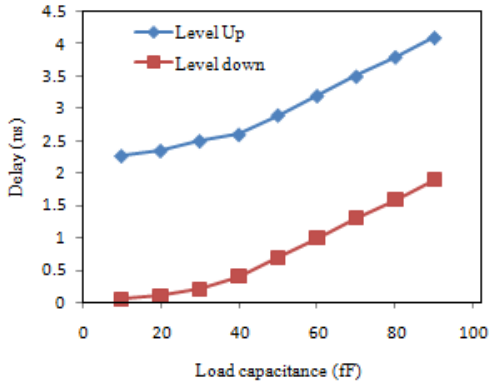


Fig. 10. Delay of VLS @ CL and VDDH = 1.2 V and VDDL = 0.2 V.

Table 1. Comparison of power, delay and PDP of various LSs.

Design	Type of shift	Technology	VDDL (V)	VDDH (V)	Active Power (nW)	Delay (ns)	PDP (fJ)
[28]	Up	90	0.2	1.8	125	3.5	0.154
[29]	Up	180	0.4	1.8	46	180	0.828
[30]	Up	90	0.2	1	79	16	0.126
[31]	Up	65	0.3	1.2	30.7	25.1	0.770
[32]	Up	90	0.16	1	77.5	21.2	0.164
[33]	Up	65	0.21	1.2	82.2	19.4	0.159
Proposed	Up	90	0.2	1.2	15	2.5	0.037
	Down	90	0.2	1.2	3	0.5	0.001

4.4. Layout implementation and area analysis

The layout implementation is performed to compare the area requirement for the designs being considered in this work to compare with the proposed VLS. The Layouts and associate area of Fig. 11 voltage level shifter for dual supply applications [28], Fig. 12 Layout depicts the two-stage level shifter using Wilson Current Mirror [30], and Fig. 13 depicts Layout of the low static power Voltage level shifter [32] that can be comparable with Fig. 14 Layout of the Proposed Voltage Level Shifter.

For a fair comparison, the designs as in [28, 30, 32] are considered to implement layout for area comparison. Because these designs have been implemented with 90nm Technology models as well as these are matching with the proposed approach. 2:1 aspect ratio is followed as it is suitable for analysis, and it is a proven value in analysing inverter which is a standard model as discussed in many literatures [34-37]. Hence width of NMOS is taken twice the channel length and the width of PMOS is twice that of the width of NMOS. This is followed while implementing the layouts of these four level shifters. The area comparison is given in Table 2.

From the Table 2, it is clear that the proposed method uses nearly half of the design space over other methods [30, 32]. As per the lambda-based design like transistor length, spacing between different wells, active edge, contact cut and all the layers are formed [38]. Hence in the area aspect, 50% less design space is occupied by the proposed approach.

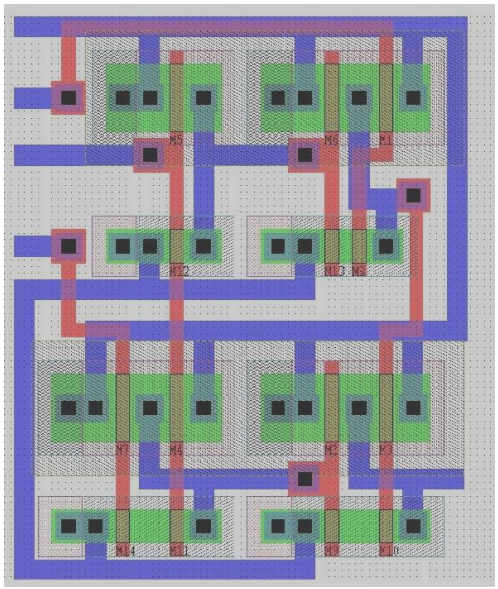


Fig. 11. Layout of the voltage LS for dual supply applications [28].

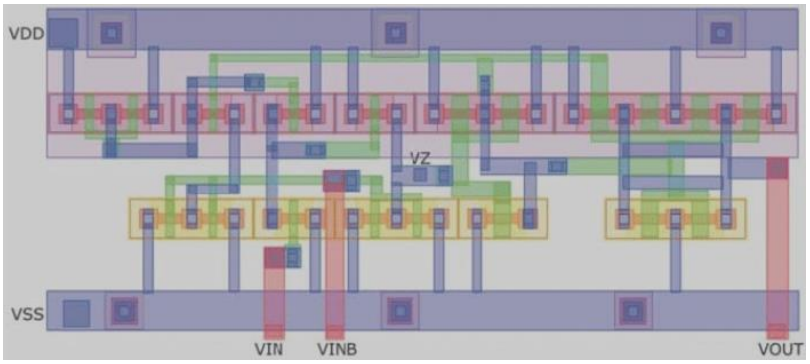


Fig. 12. Layout of the two stage LS using Wilson current mirror [30].

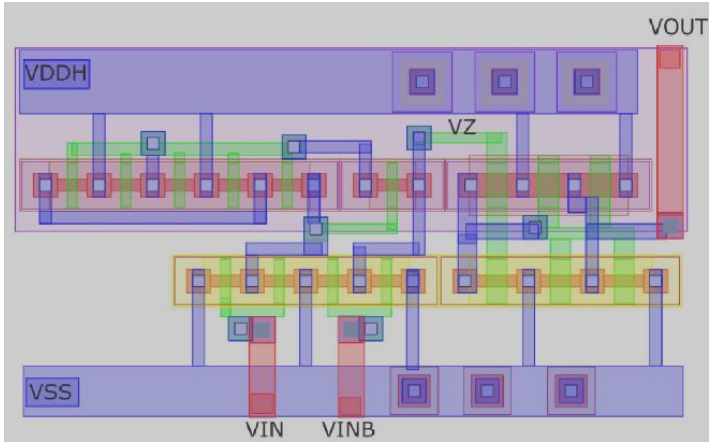


Fig. 13. Layout of the low static power voltage LS [32].

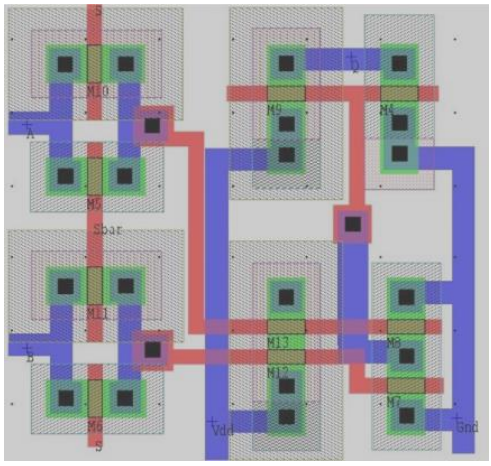
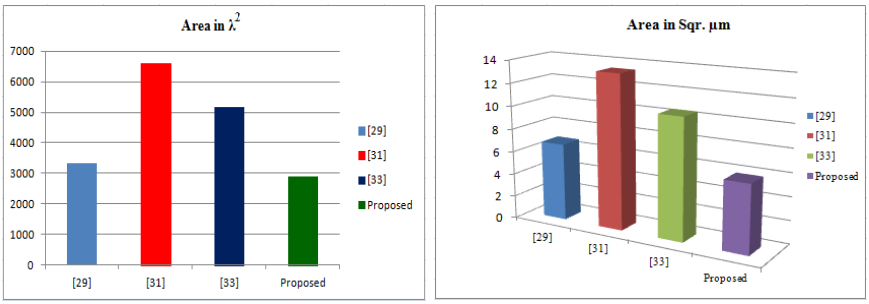


Fig. 14. Layout of the proposed voltage level shifter.

Table 2. Area comparison of various LSs.

Design	Device Count	Width	Length	Area (λ^2)	Area (μm^2)
[28]	14	52λ	64λ	3328	6.74
[30]	13	174λ	38λ	6612	13.39
[32]	8	136λ	38λ	5168	10.46
Proposed	8	50λ	58λ	2900	5.87

From Figs. 15 (a) and (b), it is clear that the area in terms of λ and μm have least values for the proposed method than the other three types due to the smaller device count and the resulting area implementation for the proposed VLS circuit. Here, λ based area is calculated with the help of Lambda based minimum width and spacing rules as specified in many literatures [39-41]. The advantage of lambda-based design rule is that any change in a design to test with lower technology models or scaling down to lower technology makes it easier to use the existing architecture to measure the area with the new (low technology) without any change. Here, only the value of lambda is going to vary (lower). The values in μm are also given in Table 2 for comparison.



(a) Area in λ^2 **(b) Area in μm^2**

Fig. 15. Chart with area in (a). λ^2 (b). μm^2.

5. Conclusion

The proposed Input controlled level-up/level-down voltage level shifter has a capability of performing two types of shifts (Level up or Level down) without any control signal. The type of shifting either up or down takes place automatically just based on its input VIN. The design has been characterized by performing power, delay, and load analysis. These analyses proved that the design consumes very low power and delay, even under varying load conditions. The average up and down shift active power is 9nW, quite appropriate for all nano-scale applications. The average power consumed by the proposed LS is nearly $1/10^{th}$ of design [28]. The designs in [31, 33, 29] have delay of 16ns, 21.2ns and 3.5ns respectively, whereas, proposed design have 2.5ns for level up operation. The overall Power Delay Product (PDP) of the proposed design has 0.03fJ. The proposed design occupies nearly 50% less layout area than [28, 30, 32] at 90 nm technology.

Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
DCVSL	Differential Cascade Voltage Switch Logic
FET	Field Effect Transistor
NMOS	n-channel Metal Oxide Semiconductor FET
PDP	Power Delay Product
PMOS	p-channel Metal Oxide Semiconductor FET
VDDH	Higher supply Voltage
VDDL	Lower Supply Voltage
VIN	Input Voltage
VLS	Voltage Level Shifter
VOUT	Output Voltage

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