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DESIGN OF MODEL PREDICTIVE CONTROL PSEUDO RANDOM PATTERN GENERATOR FOR LOW POWER BIST

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Abstract

During manufacturing tests reduction in a switching operation is a challenge. For power reduction during testing and to ensure the reliability of test circuits, Built In Self-Test (BIST) is introduced in this paper. During scan shifts, greater number of switching activity results into increase in power consumption in the circuit. Model Predictive Control (MPC) has developed significantly over period of time. It is widely used in research application and industries. Performance of system can be optimized using predictions of the output responses of the system considering future control system, with handling constraints of input as well as output states. This paper focuses on the application of MPC within BIST for the purpose of reduction in tests to ensure the reduction of consumption of power and reduction in area utilization of the system. The results of model predictive control system for test compressor are compared with low power (LP) testing pattern generator. This is beneficial for generating pseudo-random testing patterns along with preferential toggling levels and improved gradient of fault coverage as compared with conventional built-in-self-test (BIST). This produces a binary sequence with preselected toggling (PRESTO) activity. High quality tests are achieved by the proposed test compression method. The 8-bit arithmetic logic unit (ALU) is tested using the proposed method, Power consumption and area utilization are observed for the proposed system, and it is compared with conventional methods. The hardware realization is performed on Spartan-6 field programmable gate array (FPGA). It shows reduction in power consumption and area utilization for proposed method compared to the former BIST methods.

Keywords: Fault coverage, Low power Built in Self-Test (LP-BIST), Model predictive control test compressor, Preselected toggling (PRESTO), Pseudo Random Test Pattern Generator (PRPG).

1. Introduction

Power reduction is the major challenge in manufacturing test of VLSI circuits. To reduce power dissipation during testing, the scan testing is widely used due to its economic feasibility, reliability and efficiency. In the scan-based test operations, there is high data activity in a circuit under consideration. Therefore, circuit dissipates more power than it was designed. Reducing switching activity tends to decrease power dissipation [1].

Design tool for testability (DFT) which consists of IC design methodologies is used for enhancing testability feature to the hardware of product design. DFT also consists of test compression methods. Hence, it is used for developing reliable and high-quality semiconductor products. The test pattern generator with pre-decided toggling level is studied to reduce the test patterns and thus reduction in the power consumption by Filipek et al. [2]. In PRESTO generator due to loading of scan chains with various pattern, there are low transition numbers, significantly reduces power dissipation. This helps for automated adoption of its system in a way that the output test patterns are as per the requirement and in line with user defined switching rates [3].

A PRPG for LP BIST applications with a model based predictive control for test compression is being proposed in this paper. The random patterns developed with the help of linear feedback shift register (LFSR) are feed to the design under test (DUT). The result of circuit under test is compared with stored responses of DUT. If they are equal for certain operation of DUT, then the testing for other operations which are dependent on first operations are not needed. Hence it can be skipped. This method reduces test time and hence causes reduction in power consumption. 8-bit ALU is the circuit under test. It is tested with PRESTO, fully operational PRESTO, LP-decompressor and proposed Model based Predictive Control method. Output of the experiment shows that power consumption and area utilization is less for model based predictive control for test compression method than the remaining methods. Reduction in power consumption and testing time can cause improvement in performance of BIST, which is a DFT technique. The advantage of the same would be that the testing will be time and cost efficient and easier for the user. This BIST (as shown in Fig. 1) concept is versatile and can be used for any kind of circuit, therefore its uses may change as per the variety of product.

Model Predictive Control (MPC) has developed significantly over period of time. It is widely used in research application and within industries. Performance of system can be optimized using predictions of the output responses of the system with considering some future control system, with handling constraints of input as well as output states. In this paper, we worked for an introduction to the application of MPC within BIST for the purpose of reduction in tests to decrease the power consumption and area utilization of system.

To perform certain testing with more on-chip test circuits, BIST can be used, that will eliminate the requirement of high-end testers. BIST is an effective tool for the testing of certain very critical circuits which does not have direct linkages like embedded memories. Subsequently, the most advanced testing methods may be inadequate for the fastest chip. Major advantages of implementing BIST are: 1) Economical testing method because external testing using an automatic test equipment (ATE) will not be required; 2) Better fault coverage; 3) Shorter test

times if it is designed to test circuits in parallel; 4) Easy to handle troubleshooting by the customer; and 5) Easy to perform tests onsite. Consumer may test the chips before and after the mounting. BIST is used for online testing of the memory parts and logic of the system.

In developing a BIST technology there are four primary parameters that need to be considered: (1) Fault Coverage, (2) Test set size, (3) Hardware overhead, (4) Performance overhead. (1) Fault Coverage: Fraction of faults that are exposed by the test patterns which are generated by pattern generator. (2) Test set size: The larger the test sets the high the fault coverage. (3) Hardware overhead: This is the extra hardware required for BIST. (4) Performance overhead: This is the result of the BIST circuit on the efficiency of the DUT like the worst-case path delays. The benefits of BIST are reducing maintenance and testing cost as compared to ATPG. BIST can test many circuits when connected in parallel. It takes less time for test application and can test at functional system speed. BIST does not need any expensive test equipment; it tests the circuit during operation. BIST provides a high-speed testing and supports concurrent testing. Although there is a limitation of BIST like area overhead, Pin overhead, Performance overhead, Yield loss, increased time and design effort, increased BIST hardware complexity.

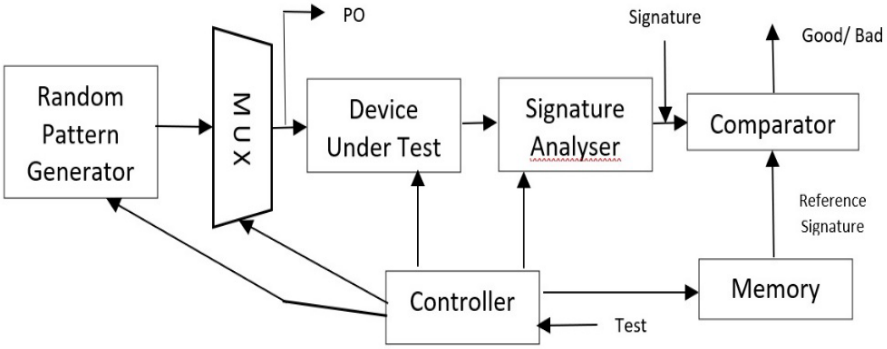

Fig. 1. Basic architecture of BIST.

1.1. Objective of the study:

The objective of the research work is to design a model predictive control pseudo random pattern generator for consuming power using BIST.

1.2. Research question:

Reduction of power consumption of a circuit while testing different power generation possibilities to be checked using Build-in-Self-Test.

1.3. Gap identified:

While designing a chip, it requires long test pattern generation and test application times. Therefore, there is increasing difficulties in performing at speed testing using automatic test equipment. This has led to problem of testability insertions which consumes more power and hence testing efficiency adversely affected. Hence to reduce the testing power, the proposed research work is being studied.

2. Literature Survey

Hatterjee and Pradhan [4] proposed design methodology for a pattern generator developed for on-chip BIST. This pattern generator consists of GLFSR which was under consideration as PRPG and logic, to synchronize the outputs of the PRPG. Using less test pattern along with small area overhead, combinational logic block may be designed to achieve single stuck at fault coverage. Kim et al. [5] introduced a new low strength constructed built in self-test using TPG method. The method makes use of mux and transition monitoring window block. With the use of LFSR satisfy pseudorandom Gaussian distribution, transitions of random pattern are generated. These transitions are replaced by k values derived by means of distribution of TMW. This technique is useful to minimize transitions up to 60%. Li et al. [6] proposed a hybrid BIST approach that extracts the deterministic check patterns. These extracted sequences are saved on-chip. Cluster evaluation is used for sequence extraction, encode deterministic patterns of the stored sequences. Experiments for the ISCAS-89 benchmark circuits show that the strategy proposed often needs much less storage on chip and test information extent than different latest BIST methods.

Due to power droop, signal transitions of the circuit under test are delayed during testing. Sreelakshmi and Reddy [7] focused on weighted pseudorandom test pattern generation for the technique LP-BIST. The signal transitions of the CUT may slow down because of PD during shift and capture phases. Author has proposed other approaches to reduce PD using scan based logic by generating LP-LFSR. With the proposed technique test data is reduced. In this paper, Sarkar and Pradhan [8] has proposed an approach based on Genetic Algorithm. With the proposed approach authors have focused on do not care filling and reordering of test data using benchmark circuits. They have integrated two methods, X-filling and ordering of test patterns for minimizing the power. The authors have achieved 66.36% of power reduction in test patterns. Another approach proposed by Nagma et al. [9] highlights on designing built-in self-test (BIST) for detection of design for fault and fault diagnosis of SRAM. This approach is based on field-programmable gate arrays (FPGAs) concept. Authors have targeted on various faults detection in look up tables. Test vectors are considered as LFSR seeds via fixing a device. The solution space of the linear equations can be considerably large. The proposed approach takes benefit of this solution area to locate seeds which may be effectively encoded by using a statistical code. Different architectures for imposing LFSR reseeding and seed compression are described.

A new scheme for lossless test vector compression that uses LFSR reseeding and coding by statistical method can be done in effective way as researched by Krishna and Touba [10]. Abu-Issa and Quigley [11] presented modified LFSR by using a bit-swapping technique by decrease the count of transitions at the inputs of the CUT by 25%. Final experimental output on ISCAS'85 and 89 benchmark circuits reduce maximum power reduction 45% during test. It has also been mentioned that the proposed design can be amalgamated with other methods to achieve a considerable power reduction up to 63%. A technique, i.e., Random single input change (RSIC) test generation is studied by Girard. It implies high level of defect coverage for low power BIST circuit. Parallel implementation of BIST is done and analysed for RSIC generator [12].

Power reductions can be bought by using micro-controller which reduces toggling quotes when feeding the scan chains, that motives low toggling activity. It reduces Power dissipation and voltage drop. Systems like STUMPS that developed for scan-based build in self-test are analysed. The peak power consuming nodes, modules and designs are revised for getting logic for scan path activity during shifting for power consumption. Deterministic judgment BIST (DLBIST) check method combines the advantages of deterministic external checking and pseudorandom LBIST. DLBIST synthesis method has complexity in computation and memory. Algorithms are tested on industrial designs for maximum 2M gates [13]. Binary decision diagrams are utilised for functional representation results into significant impetus to algebraic CAD techniques. Gate level ATPGs are generated using OBDDs [14]. Hybrid approach is used for testing of data compression scheme, that amalgamated external testing and Built In Logic Test. This approach is based on weighted pseudorandom testing. To store the weights efficiently, two methods are proposed [15]. A modified method for generation of on-chip test pattern is studied. Test patterns are generated by LFSR like PRPG. It is useful to achieve desired fault coverage. Mapping Logic is used to decode the sets of patterns. Combinational mapping logic is placed between PSPR and the circuit under test (CUT). This method decreases the test length which is essential for fault coverage by considering magnitude orders compared using LFSR [16].

To reduce toggling activity of CUT, it was proposed by Girard et al. [17] using test vector inhibiting technique. It helps to reduce switching activity hence reduces power consumption. Vector inhibiting and reseeding techniques are combined to deal with hard-to-test circuit that contains pseudo random resistant faults. These methods help to reduce power consumption during test and help to achieve high fault coverage. A new method referred to as low power test per clock BIST take a look at pattern generator. It helps to decrease switching activity during the check operation. Clock device is modified in this approach to take a look at pattern generation and clock free feeding for TPGs [18].

From the above discussion, it is clear that no one has worked on Model Predictive Control technique for power reduction. Most of the work is based on the benchmark circuits. Using FPGA, the optimum speed on digital data is acquired by Mulani and Mane [19, 20]. Girad et al. [21] proposed a reduction in switching activity while testing using modified clock scheme. While testing, to reduce arithmetic computations, lossy or lossless compression technique is required. Mulani and Mane [22] proposed techniques for image configuration. Fault detection on low power memory BIST is configured by CLBs in FPGAs by Nagama et al. for weighted pseudorandom test pattern generator [23]. Whereas we have implemented Model Predictive Control technique which reduces power by 110.64 mw.

3. Implementation of PRESTO generator

PRESTO generator includes n-bit PRPG which has a LFSR or ring generator which is shown in Fig. 2. The output of PSPR is linked to n-bit hold latches, these hold latches are eventually controlled by n–bit switch control register. The output of hold-latches is linked to phase shifter. Once the input of hold-latch is activated, the data is feed to toggle and when input is disabled, the said data is saved. Therefore, it gives constant value to phase-shifter. The output of phase-shifter is derived from outputs of XOR, which consist of three different hold latches. Only disabled hold latches drive the equivalent phase-shifter output. Then the register of toggle control controls the

hold latches which consist of '0' and '1'. When the value is '1', data can be observed from PSPR to phase shifter. The fraction reveals the scan toggling activity. The content of shift register is reloaded once per pattern to the control register.

Signals are created in an efficient systematised probabilistic fashion, by inserting into the shift register with the help of using the original PRPG with a set of weights which are programmable. These weights are decided by four AND gates developed in a probabilistic fashion by using the original pseudo random pattern generator with the said set of weights. These weights are decided by four AND gates. These gates produce '1's with a probability of 0.5 and afterwards with recurrent multiplication of 0.5 and so on. The OR gate does allow calculating probabilities extended the powers of 2. Switching register with the 4 bit is utilised to select a level of toggling as defined by the user. The AND gates are activated but Toggling register and that selects the level of switching. The switching code, i.e., 0000 is detected by 4-input NOR gates that is used to switched-off the Power functionality.

The switching level selector ensures stable content of a controlled register in context of 1s it carries, while working in the weighted random mode. The same percentage of scan chains will remain stable in the Low Power mode in spite of a set of low toggling chains that keeps switching from one to another test pattern. Hence it corresponds to a specific level of toggling. In the desired 15 different switching codes, the toggling granularity provides the solution too rough.

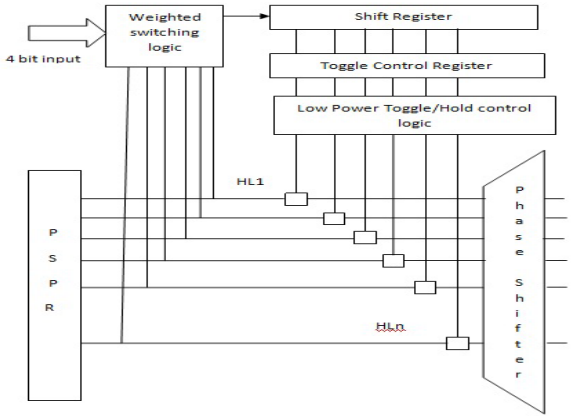

Fig. 2. Block diagram of PRESTO generator.

The toggling code defines probability to feed "1" into the shift register. Toggling codes and its related probability to feed "1" is given in Table 1.

The algorithm adopted for selecting switching code is:

(i) Considering toggling code as *m* (*m*= 1, 2, 3, 4….15), probability of feeding "1" s in the shift register is *Pm*. *P*1 = 0.5 and *P*2 = 0.25.

(ii) The time period of hold-duty cycle is $hm = \mathrm{tm} = \frac{1}{Pm}$

(iii) If '*n*' is considered as a size of PRPG,

In control register, the number of '1's would be $nm = pm * n$

(iv) Finding average count of scan chain (*am*): 1000 n bit random combinations with nm which is generated to get the count of active scan chains in each and every case and am is averaged over 1000 samples.

(v) The required level of toggling is T % and S is total number of scan chains, the Resultant number of active scan chains: $A = (T * \frac{S}{50})$.

(vi) Additional scan chains may be disabled by determining $dm = am - A$

(vii) If 'L' is the scan chain length. In an active scan chains, the value of *dm* is changed into the number of corresponding cells.

$$dm * L = (am - A) * L = am * hm * r$$

$$(hm + tm) * r = L$$

$$r = \frac{hm}{tm}$$

$$r = \left(\frac{am}{A}\right) - 1$$

where *r* = No. of hold-duty cycle

(viii) To find the best matching Ratio '*r*' is calculated for each value of *hm* and *tm* and theoretical value of expression $(\frac{am}{A}) - 1$.

(ix) The amount of toggling hold and toggle codes which produce '*r*' with the small variation from the theoretical value are chosen from the PRESTO setup parameters.

Table 1. Switching codes.

Switching code (hex value)	Switching code	Probability to inject "1" into shift register
1	0001	0.5
2	0010	0.25
3	0011	0.625
4	0100	0.125
5	0101	0.5625
6	0110	0.34375
7	0111	0.671875
8	1000	0.0625
9	1001	0.53125
A	1010	0.296815
B	1011	0.6484365
C	1100	0.1796865
D	1101	0.58984365
E	1110	0.38476553
F	1111	0.69238271

4. Fully Operational Version of PRESTO Generator

To achieve higher flexibility in forming low toggling test patterns, there is need of modification in the basic PRESTO architecture. The alternating hold and toggle interval are derived by switching time of every test pattern. T flip flop is utilized to switch the generator between states of 0 and 1. The latches that rendered he control register needs to enter the test data shifting from PRPG to scan chains if the T flip-

flop is defined to toggle period, i.e., 1. Two more 4-bit registers are applied to maintain parameters of the mode of hold and toggle. This is used to understand for how much time the generator will be in hold or toggle mode. Four two-input multiplexers routes data from toggle and hold register which is controlled by T flip flop. The source of control data that will be used in further cycles to change toggle and hold mode of operation of the generator selected by four two-input multiplexers.

For example: The input multiplexers observe the Toggle register in the toggle mode. When the output of multiplexer is 1, the flip-flop changes from 1 to 0 or vice versa. Hence all hold latches remain stable in the last recorded state. It will remain in the same state until another 1 occurs on weighted logic output. The content of the hold register decides how long it will take to close the hold mode. The random occurrence is dependent on the content of the hold register. Figure 3 indicates the basic block diagram of the fully operational type of PRESTO.

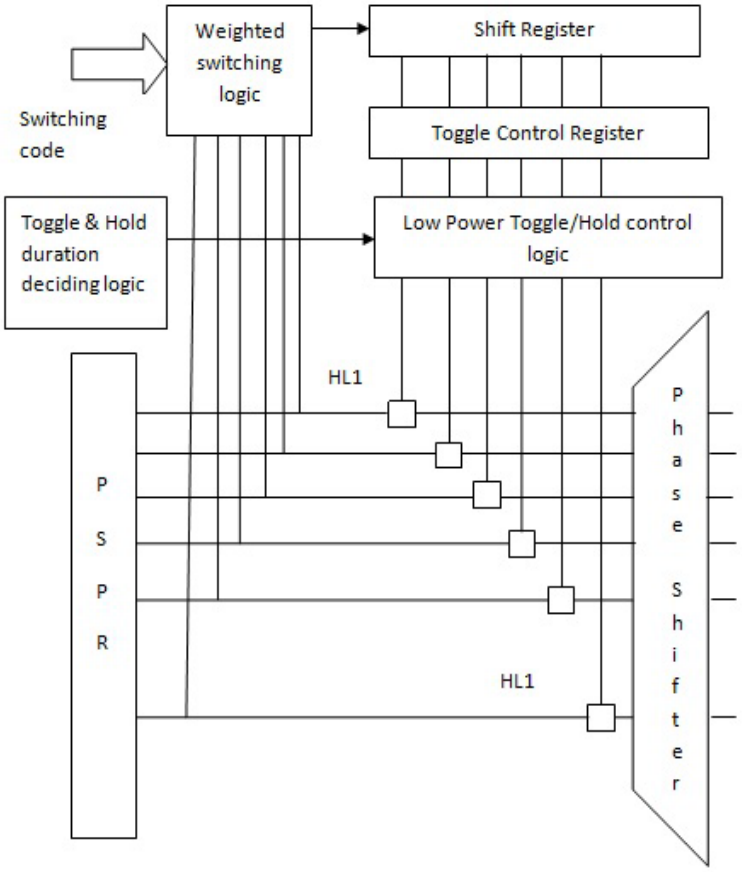

Fig. 3. Block diagram of fully operational version of PRESTO.

5. LP-Decompressor

While preserving original functionality to perform test data decompression, architecture is developed as indicated in the following block diagram of Low Power

de-compressor. The basic principle of de-compressor is disabling weighted logic blocks. When shift register follows the multiplexer, the content of toggle control register is chosen in systematized manner. Four-bit binary down counter determines the period of toggle and hold phase as it alternatively pre-set by toggle and hold registers. T flip flop and down counter are required to be initialized after every test pattern. The status of decompressor to operate either in the toggle mode or hold mode is dependent on initial value of the T flip flop and it determines the mode's duration. Operations of the T flip flops remains the same as the PRPG. External automatic test equipment channels which are providing inputs to the original PRPG allow implementing a continuous flow test data decompression epitome like dynamic LFSR reseeding. The entire de-compressor, the offset and the values of Toggle and Hold registers, the scan chains, value of PRPG, the switching code and the corresponding phase shifter will develop deterministic test patterns. This will have a desired level of toggling if the scan chains are balanced. The compression architecture is tightly coupled with the decompression operation. Figure 4 shows block diagram of LP decompressor.

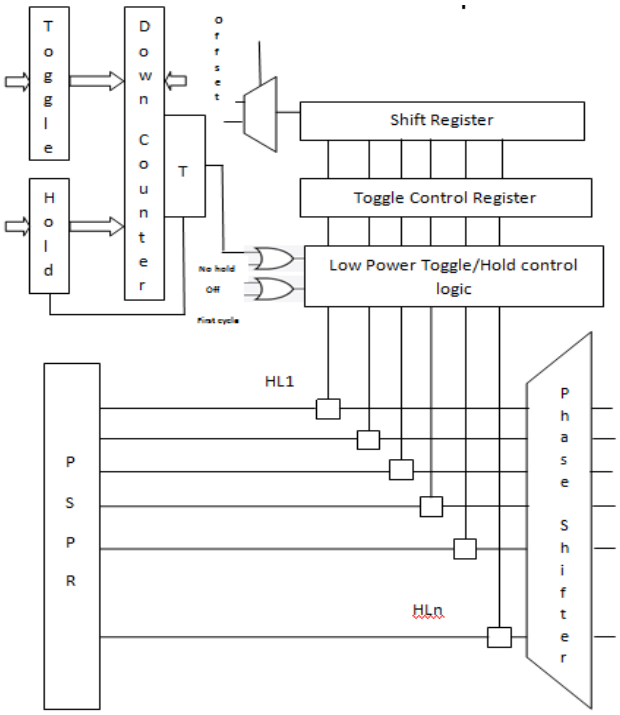

Fig. 4. Block diagram of LP decompressor.

6. Proposed Model Predictive Control for Test Compression

Model Predictive Control (MPC) has developed significantly over period of time. It is widely used in research application and within industries. By handling constraints of input as well as output states and using predictions of the output responses of the system with considering some future control system, the performance of system may be optimized. MPC algorithms are consists of following 3 major components: 1. a model of the controlled plant, 2. an optimizer

which evaluates control actions by using an objective function with an optimization strategy, and 3. a predictor which computes the future changing behaviour of the plant output or controlled variable. In this paper, we have incorporated an introduction to the application of MPC within BIST for the purpose of test compression to decrease the power consumption and area utilization of system. Figure 5 shows basic block diagram of model predictive control system. Output responses are generated by considering past and present inputs and reference signatures of the system responses. Optimizer is control logic for taking action based on present and past input signals and output signals.

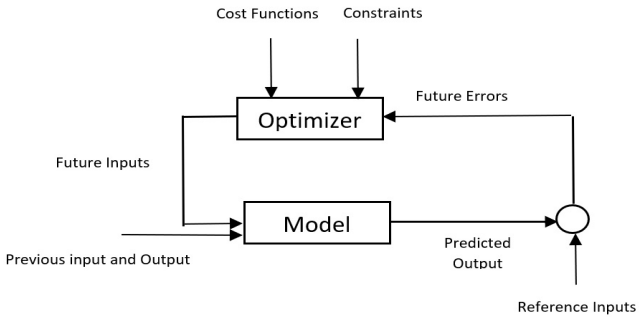

Fig. 5. Block diagram of model predictive control.

This technique uses model predictive approach for reducing the test size and thus the power utilisation is minimized.

Figure 6 shows block diagram for Model predictive control for test pattern compression. CUT is 8-bit ALU to which test patterns are applied. The response of CUT is compared with the results of reference signature generator. ALU performs the arithmetic and logical operations. Operations of ALU are selected by using select lines. If 1000 test patterns for addition operation are tested successfully then, multiplication operation is not tested by the system. It will move towards next operation. This will decrease the test duration and consumption of power of the system. This technique can be applied to the circuits also by identifying redundant test conditions so that it compresses testing procedure and minimizes power consumption.

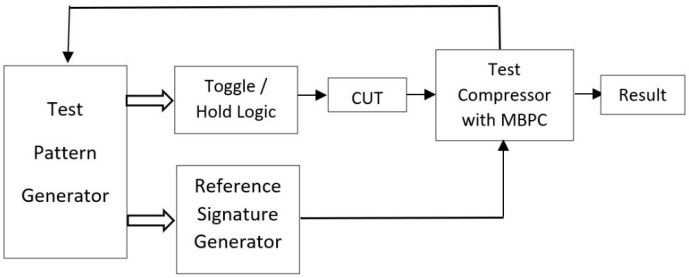

Fig. 6. Block diagram of MPC based test compression technique.

Algorithm/Process flow for test compression procedure using MPC:

i. Generate random test patterns.
ii. Test patterns are applied to the CUT and reference signature generator.

iii. Compare response of reference signature generator and response of CUT.
iv. If equal toggle/hold logic operates in HOLD mode and avoid sending test patterns to CUT to test other redundant operation of CUT.
v. If NOT equal toggle/hold logic operates in TOGGLE mode and sends test pattern to CUT to test other operation of CUT.

The 8-bit ALU is tested using the circuit under test, which performs 8 operations including arithmetic and logical operation based on 3 bits select signal 'op'. As shown in Table 2 for test sequence '000' ALU performs addition operation and for '001' it performs multiplication operation. Test compressor using MPC block checks the test patterns and their response. If responses are matched then flag is set. After checking 1000 samples of addition operation flag is checked, if it is set that means tests are passed for 1000 test patterns then multiplication operation is not tested as it depends on addition operation and hence redundant. Then test other non-redundant operations and generates the results. In this process as redundant operations are not tested testing time is decreased and power consumption is also minimised as test patterns are in hold mode for the redundant operations of CUT.

Table 2. Arithmetic and logic unit operations.

Sequence	Operation
000	Addition
001	Multiplication
010	Subtraction
011	Division
100	Logical shift left
101	Logical shift right
110	Rotate left
111	Rotate right

7. Results and Discussion

The PRESTO based PRPG has analysed in Xilinx platform. The proposed low power model predictive control for test compression system has designed and developed. Hardware realization of the system is performed on Xilinx's Spartan6xl6slx4-3TG144 device. Figures 7 and 8 show RTL schematic basic PRESTO generator with random data generator and phase shifter output psout.

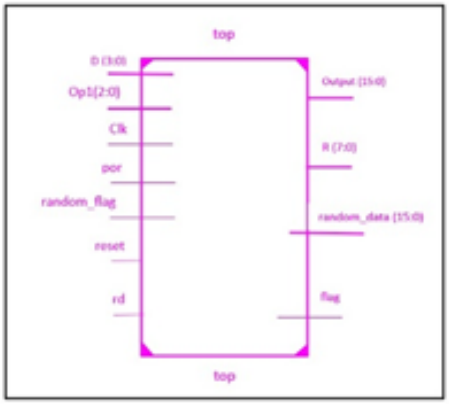

Fig. 7. RTL schematic of basic PRESTO generator.

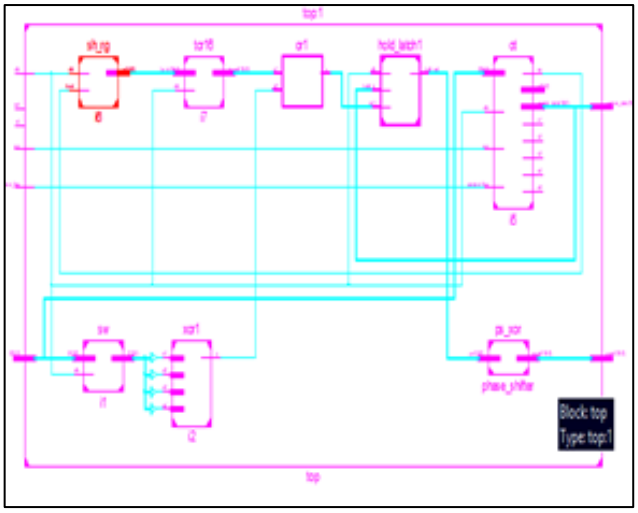

Fig. 8. RTL detailed schematic of basic PRESTO generator.

Device utilization summary of basic PRESTO generator is shown Table 3**,** which gives the PRESTO generator.

Table 3. Device utilization summary of basic PRESTO generator.

Parameters	Used	Available	Utilization (%)
Number of Slice Registers	74	4800	1
Number of Slice LUTs	42	2400	1
Number used as Logic	42	2400	1
Number with an unused Flip Flop	15	89	20
Number with an unused LUT:	47	89	24
Number of fully used LUT-FF pairs	27	89	55
Number of bonded IOBs	27	102	26
Number of BUFG/BUFGCTRLs	1	16	6

Power utilization of basic PRESTO generator is shown in Table 4. It describes the static and dynamic power consumption of basic PRESTO generator. Table 4 shows power utilization summary. It includes static power and dynamic power. It is observed that power consumption is minimum for model prediction control test compressor. Device utilization summary of fully operational PRESTO generator is shown in Table 5 number of input output pins, flip-flops, LUTs used for designing PRESTO generator.

Figures 9 and 10 show RTL schematic of fully operational version of PRESTO generator which shows input and output pins of fully operational.

Table 4. Power utilization summary.

Methodology			Total Power (mW)	Dynamic Power (mW)	Static Power (mW)
Fully operational PRESTO			150.64	135.04	15.60
LP-Decompressor	188.50	172.95	15.55		
MPC			110.64	95.96	14.68

Table 5. Device utilization summary of fully operational PRESTO generator.

Parameters	Used	Available	Utilization (%)
Number of Slice Registers	52	4800	0
Number of Slice LUTs	38	2400	0
Number used as Logic	38	2400	0
Number with an unused Flip Flop	10	17	5
Number with an unused LUT:	24	17	88
Number of fully used LUT-FF pairs	28	17	5
Number of bonded IOBs	27	102	26
Number of BUFG/BUFGCNTRLS	1	16	6
Number of DSP4A1s	3	8	37

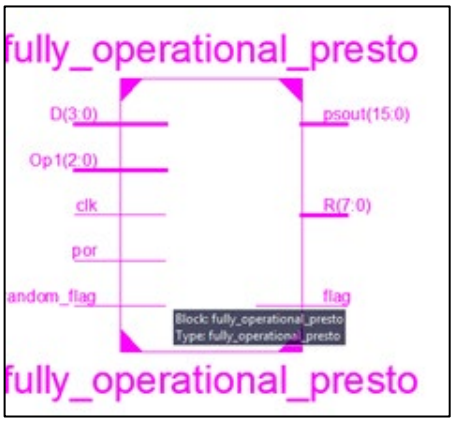

Fig. 9. RTL schematic of fully operational PRESTO.

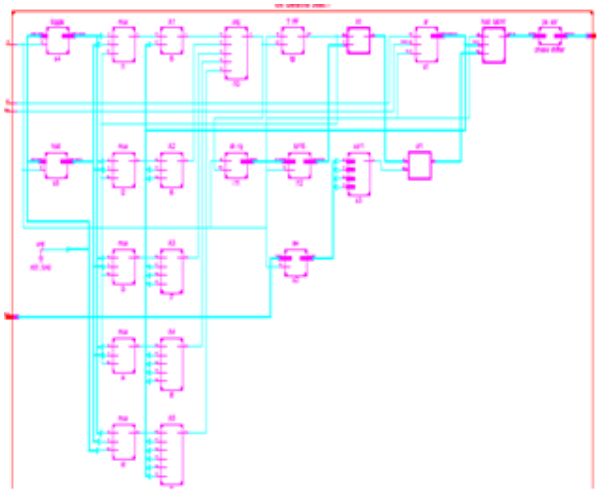

Fig. 10. RTL schematic of fully operational version of PRESTO generator.

Figures 11 and 12 show RTL schematic of basic PRESTO generator with random data generator and phase shifter output psout, which is applied as input to the CUT (ALU). Device utilization summary of LP-Decompressor is as shown in Table 6.

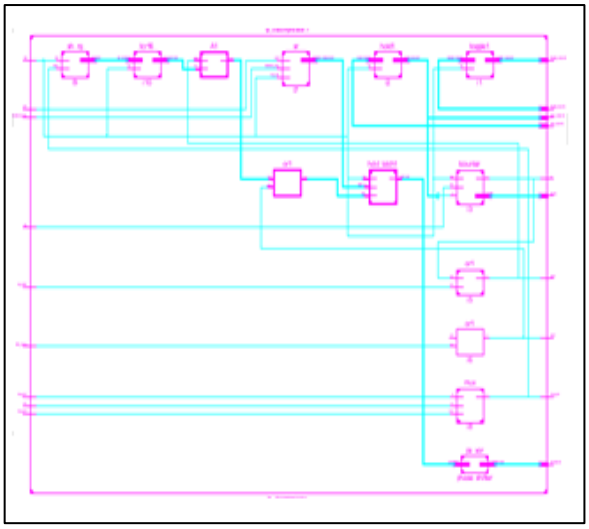

Fig. 11. RTL schematic of LP-Decompressor.

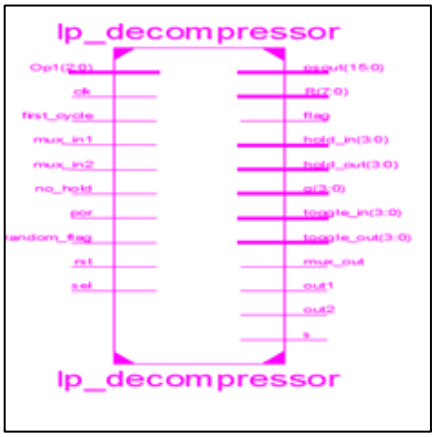

Fig. 12. RTL schematic of LP-decompressor.

Table 6. Device utilization summary of LP-decompressor.

Parameters	Used	Available	Utilization (%)
Number of Slice Registers	66	4800	1
Number of Slice LUTs	52	2400	2
Number used as Logic	52	2400	2
Number with an unused Flip Flop	19	85	22
Number with an unused LUT:	33	85	38
Number of fully used LUT-FF pairs	33	85	38
Number of bonded IOBs	61	102	59
Number of BUFG/BUFGCNTRLS	1	16	6
Number of DSP4A1s	3	8	37

Figure 13 shows the simulation output of MPC test compressor and Fig. 14 shows RTL schematic of MPC test compressor. Device utilization summary of model predictive control test compressor is shown in Table 7.

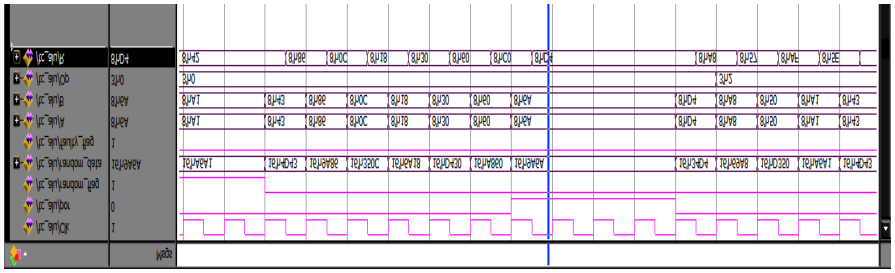

Fig. 13. Simulation output of MPC test compressor.

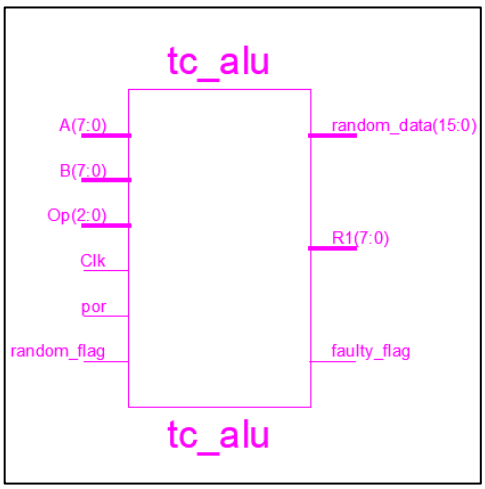

Fig. 14. RTL schematic of MPC test compressor.

Table 7. Device utilization summary of MPC test compressor.

Parameters	Used	Available	Utilization(%)
Number of Slice Registers	16	4800	0
Number of Slice LUTs	2	2400	0
Number used as Logic	2	2400	0
Number with an unused Flip Flop	1	17	5
Number with an unused LUT:	15	17	88
Number of fully used LUT-FF pairs	1	17	5
Number of bonded IOBs	19	102	18
Number of BUFG/BUFGCTRLs	1	16	6

Table 8 shows the result comparison of existing system and the results of Wang and Gupta [24] and Jagadeesh and Swamy [25] with proposed system.

Table 8. Result comparison.

Parameter	Existing System [25]	Existing system [26]	Proposed System
Power Consumption (W)	0.089	0.088	0.110
Path Delay (ns)	7.061	7.183	7.528
No. of slices (CLB)	10	14	42
Frequency (MHz)	141.6	139.2	132.84

In Table 8, the existing system was implemented for 3-bit input data (i.e., for 8 combinations) and their power consumption was 0.089 and 0.088 W respectively. In the proposed system, the power consumption is 0.110 W, because of 16-bit (i.e., for 65,536 combinations) input data. This shows that our system is more efficient in terms of power consumption. Also, it is more efficient in terms of operating frequency.

8. Conclusions and Future Scope

Experimental results of model based predictive control test compressor are compared with PRESTO LP PRPG. The proposed generator permits loading scan chains with the test patterns with low transition test patterns considerably reduce the power dissipation. The power consumption and area utilization of the system is lesser than the PRESTO, fully operational PRESTO and LP-decompressor. Thus, the proposed Model predictive control test compression method helps to reduce testing time by skipping the redundant operations of the CUT, thereby reducing the power dissipation during testing.

Abbreviations

BIST	Built In Self Test
CUT	Circuit Under Test
LP PRPG	Low Power Pseudo Random Pattern Generator.
MPC	Model Predictive Control
PRESTO	Preselected Toggling

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