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COMPARATIVE ANALYSIS OF NOVEL PHASE DELAY TIME ADJUSTMENT METHOD AND EQUAL PHASE DELAY TIME DEVELOPMENT METHOD ON THE THD REDUCTION OF TPVMI SYSTEM

M. IRWANTO[1,2,*], M. HADDIN[3]

[1]Department of Electrical Engineering, Faculty of Industrial Technology, Medan Institute of Technology, Medan, Indonesia
[2]Fellow of Centre of Excellence for Renewable Energy, Faculty of Electrical Engineering Technology, Universiti Malaysia Perlis (UniMAP), Perlis, Malaysia
[3]Department of Electrical Engineering, Universitas Islam Sultan Agung, Jalan Kaligawe Raya Km. 4, Semarang, Indonesia
*Corresponding Author: mhd-irwanto@itm.ac.id

Abstract

Multilevel inverters have been developed by various topologies, one of the topologies is cascaded full bridge inverter that generates multilevel output voltage waveform. However, it needs a lot of numbers of switching component and pulse wave generator. It also has high total harmonic distortion (THD) still. It is due to the multilevel inverter has no pure sinusoidal output voltage waveform. A method to reduce the number of pulse wave generator and also to adjust the voltage level on the multilevel inverter is very important to be considered to achieve the lowest THD and fulfil the condition of good power quality. This paper presents a transformerless photovoltaic multilevel inverter (TPVMI). Kaneka G-SA060 amorphous silicon (a-Si) PV module as main direct current (DC) source is modelled by SIMULINK MATLAB. The model results of photovoltaic (PV) module performance are validated using the statistical analysis, they are root mean squared error (RMSE), coefficient of residual mass (CRM), percentage error (*e*) and Nash-Sutcliffe equation (NSE). A novel phase delay time adjustment method and equal phase delay time development method are proposed on the TPVMI system to achieve the lowest THD. 7-level output voltage waveform of the TPVMI is generated as an output of three cascaded inverters. The inverters are constructed by four switching components (four MOSFETs), but only two types of pulse wave generator to drive the gate terminals of MOSFET. Thus, these methods have advantage to reduce the number of pulse wave generator compared to the existing methods. The results show that the PV module performances (short circuit current and open circuit voltage) are valid to the data sheet of PV module based on the statistical analysis. The THD of 20.76 % generated by the novel adjustment method of phase delay time is lower than the THD of 40.92 % generated by the equal phase delay time development method. It indicates that the novel adjustment method of phase delay time has a better performance compared to the equal phase delay time development method.

Keywords: Multilevel inverter, Phase delay time, Photovoltaic, Switching time.

1. Introduction

The reservation of fossil fuel is felt by every country in the world. The limitation of coal, gas and oil cause the scientist and government look for the alternative energy. It is due to the fossil fuel will be empty at one time. Renewable energy is very good alternative energy to change the conventional energy. Photovoltaic (PV) is one part of the renewable energy and it is very huge application in the world because the main energy source comes from the sun, and it is easy to be converted become DC electrical energy. Normally, the loads need alternating current (AC) source, thus the DC electrical energy can be converted to be AC electrical energy using inverter circuit. It means that one of PV applications is in the inverter system [1].

There are some topologies to vary the inverter gain. The pulse width modulation (PWM) is the most efficient method to control the output voltage of inverters. Five basic PWM methods are always applied in the inverters, the first PWM method is linear modulation, the second one is saw tooth PWM, the third one is single pulse width modulation, the fourth one is multiple pulse width modulation (MPWM) and the last one is sinusoidal pulse width modulation (SPWM) [2]. The inverter can be classified into three types based on its output voltage waveform. They are square voltage waveform inverter, multilevel voltage waveform inverter and sinusoidal voltage waveform inverter. The term of multilevel inverter is started with 3-level voltage waveform as introduced by Nabae et al. [3] and the mention of multilevel is always by odd levels (3-level, 5-level, 7-level, 9-level and so on). There are three difference topologies of multilevel inverter that have been constructed, they are neutral clamped (diode clamped) [3], flying capacitor (capacitor clamped) [4] and cascaded full bridge inverter [5-7].

Neutral clamped (diode clamped) inverter is composed by main switching devices with their driver terminal are driven by pulse waves. Auxiliary switching devices (diodes) are applied to clamp the potential of output voltage terminal to the neutral terminal potential. 3-level neutral clamped (diode clamped) inverter has been developed by Nabae et al. [3], and Banerjee et al. [8] with four transistor or MOSFET components and two diode components as neutral point. A 3-level voltage waveform is generated by the inverter, but it is still not pure 3-level (it still contents some pulse waves in the 3-level waveform). A combination of transistor and diode clamped inverter is developed by Singh et al. [9]. The main function of combination circuit is to boost the 5-level output voltage waveform. Nine switching components are needed to generate the 5-level voltage waveform. It needs more switching components compared to the normal inverter to generate same level voltage waveform. Also, it is still not pure 5-level (it still contents some pulse waves in the 5-level waveform).

The structure of flying capacitor (capacitor clamped) inverter is alike to the neutral clamped (diode clamped) inverter. The different is only that the diode clamped in the neutral clamped (diode clamped) inverter is changed to the capacitor clamped in the flying capacitor (capacitor clamped) inverter. In term of switching component number to generate a same level voltage waveform is same for both multilevel inverters. A m-level flying capacitor (capacitor clamped) inverter is constructed by Koshti and Rao [10] with the number switching component is $2(m-1)$, the number DC-link capacitor is $(m-1)$ and the number of auxiliary capacitor is $((m-1)(m-2))/2$. 7-level voltage waveform has been developed with eight switching components, four DC-link capacitors and six auxiliary capacitors.

The cascaded full bridge inverter is connection of some inverters that connected in series and needs more than one DC voltage source to generate multilevel voltage waveform. An m-level cascaded full bridge inverter needs the number switching component of 2(*m*-1) which is the same number of switching component for the neutral clamped (diode clamped) and flying capacitor (capacitor clamped) inverters [11, 12]. 5-level cascaded full bridge inverter has been developed by Javvaji and Varaja [5], Tayab and Al-Humayun [7], Koshti and Rao [10], and Rodriguez et al. [13] which needs eight switching components and two separated DC voltage sources.

An equal phase method with equal magnitude of output voltage waveform on the m-level cascaded full bridge inverter is constructed by Javvaji and Varaja [5], and Mohideen and Kajaan [14]. A mathematical modelling bases on the expansion of Fourier Series is conducted. The developed mathematical function contains the switching angles, $\Theta_1, \Theta_2, \ldots, \Theta_n$, where n follows the number of switching component or n=2(m-1). The switching angles are developed to generate the m-level output voltage waveform with an equal phase for every level. The developed mathematical function also contains a parameter of DC voltage, V_{dc} with one division factor to obtain the equal magnitude of m-level output voltage waveform.

A simple mathematical modelling of equal phase method is created by Tayab et al. [6], and Jalkanuru and Kiber [15] for m-level cascaded full bridge inverter that it is given by $\Theta_i = i(180°/m)$. It is developed for half cycle of the m-level output voltage waveform or in the angle range of 0° to 180°. The factor, i is given by i = 1, 2, 3, …, m, it means that the model needs m-switching angle to generate the half cycle of the m-level output voltage waveform. This model is also still supplied by the main DC voltage source number of (m-1)/2 to generate the equal magnitude for each level on the m-level output voltage waveform.

An equal phase method based on quadrant division is proposed by Tayab and Al-Humayun [7] on the m-level cascaded full bridge inverter. It is based on one cycle of the m-level output voltage waveform which it is divided by four quadrants (the first quadrant, q_1; second quadrant, q_2; third quadrant, q_3 and fourth quadrant, q_4). Each quadrant has an angle scope of 90º, it means the first, second, third and fourth quadrant have the angle range of $0^\circ \leqslant q_1 \leqslant 90°$, $90° < q_2 \leqslant 180°$, $180° < q_3 \leqslant 270°$ and $270° < q_3 \leqslant 360°$, respectively. The switching angle formulation of $\Theta_i = i(180º/m)$ is applied by Tayab and Al-Humayun [7], thus the first quadrant has switching angle of $\Theta_1, \Theta_2, \ldots, \Theta_{(m-1)/2}$, the second quadrant has switching angle of $180° + \Theta_1$, the third quadrant has switching angle of $180° + \Theta_{(m-1)/2}$ and the fourth quadrant has switching angle of $360° - \Theta_1$. The quadrant division with their created switching angle can generate the m-level output voltage waveform.

The separated DC voltage sources of cascaded full bridge inverter can come from batteries, wind power, fuel cells or PV modules [11, 16, 17]. PV modules are always applied compared to the other renewable energy sources, it is due to easy to convert solar energy to be DC electrical energy and the DC output of PV module is stable. The PV modules as DC voltage source have been applied in the 3-level transformerless photovoltaic inverter (TPVI) [18-25] and multiple pulse width modulation TPVI by Masri et al. [26]. The TPVI does not use transformer, thus in term of structure is to be small, light and cheap. No transformer means it has eliminated transformer losses, thus the efficiency of TPVI is relatively high. But its output voltage waveform is three level, thus its THD is relatively high. One effort is very important to reduce the THD of the TPVI and a transformerless photovoltaic multilevel inverter (TPVMI) is suitable to

solve this problem. Based on the IEEE standard 519™-2014, the maximum THD required is 8% for the lower voltage system of 1 kV [27].

This paper presents a modeling of TPVMI system with Kaneka G-SA060 amorphous silicon (a-Si) PV module as separated DC voltage source. It consists of three full bridge inverters that connected in series or cascaded full bridge inverters. Each full bridge inverter is supplied by one or three PV modules to generate a 7-level output voltage waveform. The number of switching component is twelve MOSFETs, but the pulse driver to drive the driver terminal of switching components is only eight pulse drivers (it is a half of the total number of pulse driver on the normal multilevel inverter). A development of equal phase delay time method and novel adjustment method of switching time (phase delay time) on the TPVMI are proposed to achieve the lowest THD.

2. Methodology

2.1. Proposed modelling of PV module

A simulation modelling of PV module is created based on the data sheet that contents the electrical parameters as stated in Table 1. The electrical parameters of PV module are needed to be entered into the block parameter of PV module in SIMULINK MATLAB as shown in Fig. 1. A constant block as solar irradiance value is needed to be connected to the PV module, also the current and voltage sensor are needed to measure the short circuit current and open circuit voltage of PV module. The multiplication of voltage and current produces the power of PV module.

Table 1. Electrical parameters of PV module.

Electrical parameters	Value
Maximum power	60 W
Voltage at maximum power	67 V
Current at maximum power	0.9 A
Short circuit current	1.19 A
Open circuit voltage	91.8 V

A complete simulation modelling of PV module as shown in Fig. 1 is simulated to observe the PV module performance for constant temperature of 25°C and various solar irradiance. The resistance of resistor value that connected in parallel to the PV module is adjusted to obtain the suitable PV performance in the data sheet.

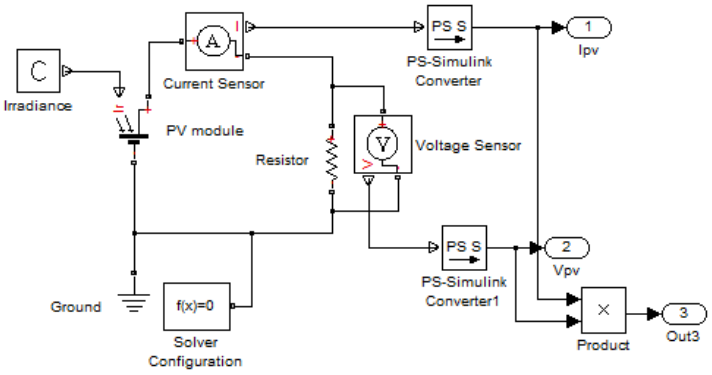


Fig. 1. Simulation modelling of PV module.

The comparison between simulation and data sheet of PV module performance is validated by using statistical analysis. The statistical analysis is conducted in term of root mean squared error (*RMSE*), coefficient of residual mass (*CRM*), percentage error (e) and Nash-Sutcliffe equation (*NSE*)as explained below which uses Eq. (1), (2), (3) and (4), respectively [28, 29].

$$CRM = \frac{\sum_{i=1}^{n} V_{dat,i} - \sum_{i=1}^{n} V_{sim,i}}{\sum_{i=1}^{n} V_{dat,i}} \quad (1)$$

$$RMSE(\%) = \frac{\sqrt{\frac{\sum_{i=1}^{n}(V_{sim,i} - V_{dat.i})^2}{n}}}{\overline{V_{dat}}} \times 100 \quad (2)$$

$$NSE = 1 - \frac{\sum_{i=1}^{n}(V_{dat,i} - V_{sim,i})^2}{\sum_{i=1}^{n}(V_{dat,i} - \overline{V_{dat}})^2} \quad (3)$$

$$e(\%) = \frac{V_{dat,i} - V_{sim,i}}{V_{dat,i}} \times 100 \quad (4)$$

where $V_{dat,i}$ is the data sheet of PV module open circuit voltage at *i* data, $V_{sim,i}$ is the simulated open circuit voltage of PV module at *i* data.

2.2. Proposed transformerless photovoltaic multilevel inverter

Figure 2 shows a modelling of TPVMI system that it consists of PV module, inverter circuit that it is driven by pulse generator, and it is loaded by the AC load.

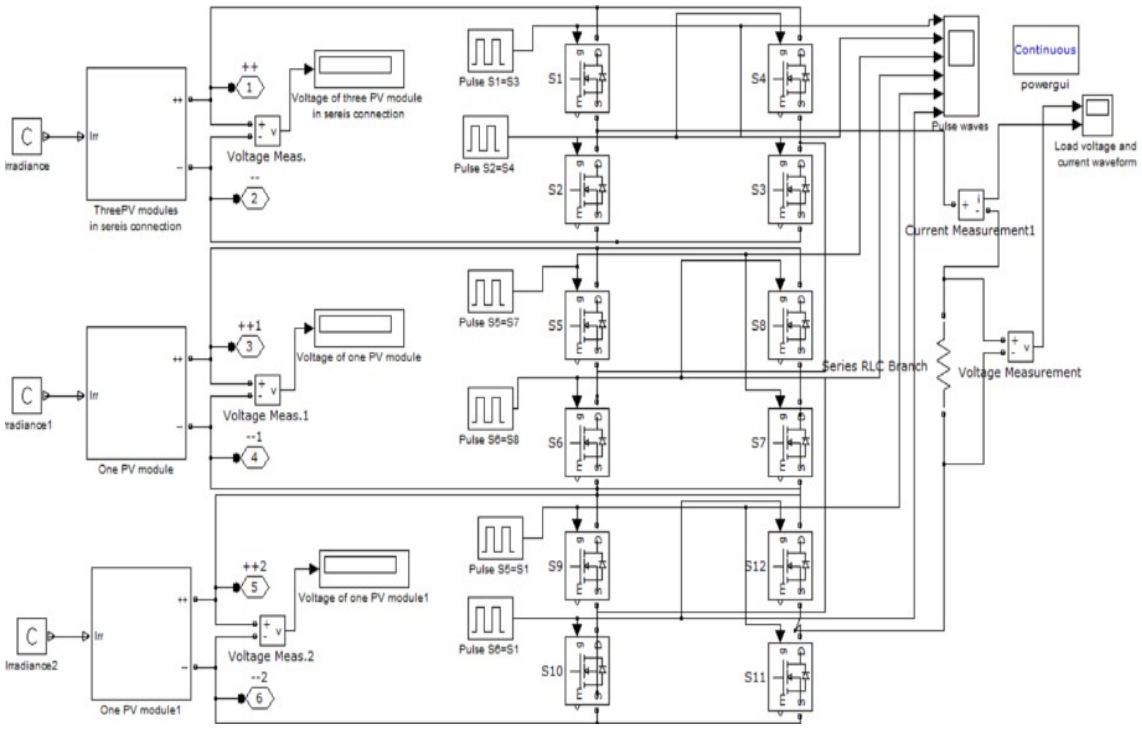


Fig. 2. Modelling of TPVMI.

The creation procedure of block set of TPVMI system is stated below:

- PV module block set is created by following the simulation modelling of PV module as shown in Fig. 1.
- A pulse generator block set is created to drive the four MOSFETs on the inverter circuits as shown in Fig. 3. A novel adjustment method of MOSFET switching time is explained in section 2.3. The 7-level inverter are modelled in this paper. The proposed model is based on the cascaded inverter circuit. The 7-level voltage waveform can be generated by cascading three inverter circuit. Each pair of switching component as shown in Fig. 2 (S_1 and S_3, S_2 and S_4, S_5 and S_7, S_6 and S_8, S_9 and S_{11}, S_{10} and S_{12}) that in a cross-section position of each inverter circuit is driven by a same pulse wave. This proposed method has an advantage to reduce the number of pulse generator or pulse driver circuit compared to the existing method which each switching component should have a pulse generator as explained by Tayab et al. [6], Tayab and Al-Humayun [7], and Jalkanuru and Kiber [15].

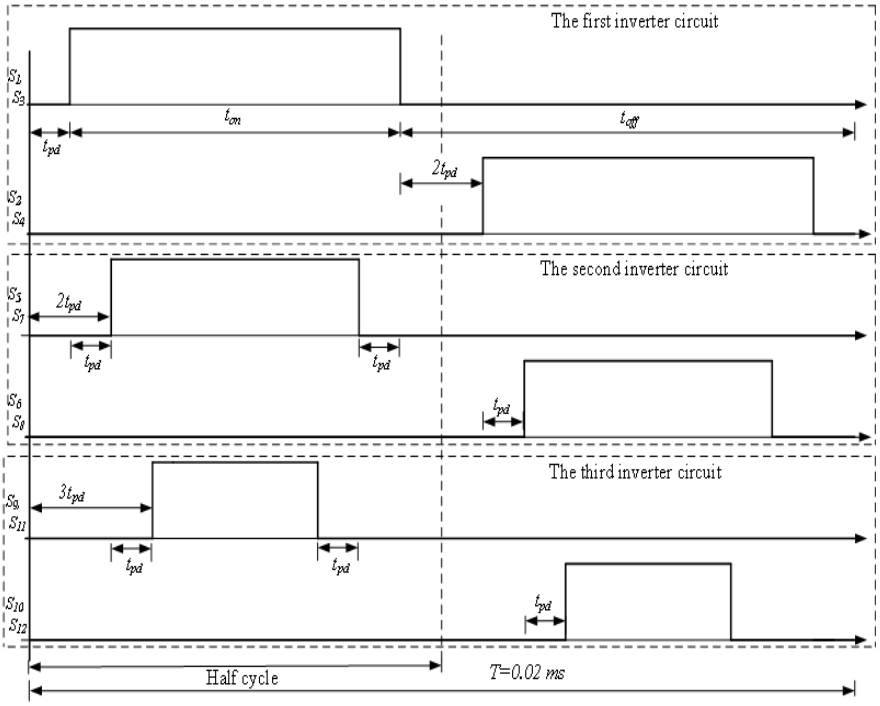


Fig. 3. Novel adjustment method of phase delay time on the TPVMI.

- A resistance of 25 Ω is applied as AC resistive load. Simulate and analyse the performance of TPVMI system including the 7-level AC voltage waveform and *THD*. The *THD* can be calculated following the Eq. (5).

$$THD = \frac{\sqrt{V_2^2+V_3^2+V_4^2+\ldots+V_n^2}}{V_1} \quad (5)$$

where V_n is the voltage magnitude of n^{th} harmonic.

2.3. Proposed modelling of multilevel inverter

2.3.1. Equal phase delay time development method

Phase delay time, t_{pd} is a time which change the AC voltage level. It is very important to decide the number of voltage and THD level related to the AC loads. Figure 4 shows a m-level output voltage waveform of the proposed TPVMI for the period system of 0.02s or the frequency system of 50 Hz. It is created by the positive and negative half cycle which both are symmetrical and divided by four quadrants (0 to 0.005 s; 0.005 s to 0.01 s; 0.01 s to 0.015 s and 0.015 s to 0.02 s). There are 2(m-1) phase delay times (t_{pd1}, t_{pd2}, t_{pd3}, … , $t_{pd(m-2)}$, $t_{pd(m-1)}$) are needed to generate the m-level output voltage waveform. It is due to the waveform of second quadrant is mirror symmetrically to the waveform of first quadrant and also the waveform of negative half cycle is centrally symmetrical to the waveform of positive half cycle. Thus, the phase delay times in the first quadrant (0 to 0.005 s) are as the main phase delay times, whereas the other phase delay times in the second, third and fourth quadrant are calculated following formulation below.

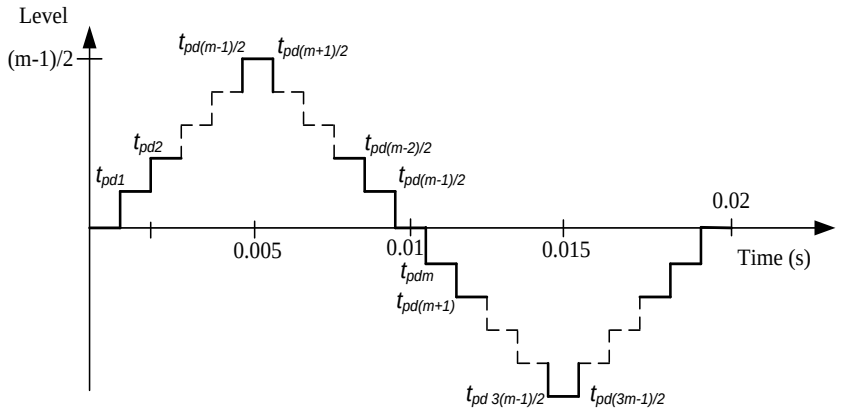


Fig. 4. m-level output voltage waveform.

The main phase delay times in the first quadrant (0 to 0.005 s) as shown in Eq. (6). The other phase delay times in the second, third and fourth quadrants are calculated based on the main phase delay times. The phase delay times in the second quadrant (0.005 s to 0.01 s) as shown in Eq. (7). The phase delay times in the third quadrant (0.01 s to 0.015 s) as shown in Eq. (8). The phase delay times in the fourth quadrant (0.015 s to 0.02 s) as shown in Eq. (9).

$$t_{pdi} = ix\frac{0.01}{m}, where\ i = 1,2,3,\dots,\frac{m-1}{2} \tag{6}$$

$$t_{pd(m+1)/2} = 0.01 - t_{\frac{pd(m-1)}{2}};\ 0.01 - t_{\frac{pd(m-2)}{2}};\ \dots;\ 0.01 - t_{pd1} \tag{7}$$

$$t_{pdm} = 0.01 + t_{pd1};\dots;\ 0.01 + t_{pd(m-1)/2} \tag{8}$$

$$t_{pd(3m-1)/2} = 0.02 - t_{pd(m-1)/2};\dots;0.02 - t_{pd1} \tag{9}$$

Table 2 shows phase delay time, t_{pd} and the time of switching component for the ON condition, t_{on} for each switching components on the TPVMI based on the equal phase delay time development method and related to the pulse generator in Fig. 3.

Table 2. The phase delay time, t_{pd} and the time of switching component for the ON condition, t_{on}.

First inverter				**Second inverter**				**Third inverter**			
S_1, S_3		S_2, S_4		S_5, S_7		S_6, S_8		S_9, S_{11}		S_{10}, S_{12}	
t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}
0.001	0.007	0.011	0.007	0.003	0.004	0.013	0.004	0.004	0.001	0.014	0.001

2.3.2. Adjustment method of phase delay time on TPVMI

The proposed adjustment method of phase delay time on TPVMI is shown in Fig. 3. A pulse wave is generated by the pulse generator or pulse driver circuit for two switching components (S_1 and S_3, S_2 and S_4, S_5 and S_7, S_6 and S_8, S_9 and S_{11}, S_{10} and S_{12}). This method based on the analysis of the generated pulse wave in one cycle for the period of 0.02 ms or the frequency of 50 Hz. The period, T of one cycle is given by the Eq. (10).

$$T = t_{pd} + t_{on} + t_{off} \tag{10}$$

$$t_{pd} + t_{on} + 2t_{pd} = 3t_{pd} + t_{on} \tag{11}$$

$$t_{on} - t_{pd} - t_{pd} = t_{on} - 2t_{pd} \tag{12}$$

$$t_{pd} + t_{on} + 2t_{pd} + t_{pd} = 4t_{pd} + t_{on} \tag{13}$$

$$t_{on} - 2t_{pd} - t_{pd} = t_{on} - 3t_{pd} \tag{14}$$

$$t_{pd} + t_{on} + 2t_{pd} + t_{pd} + t_{pd} = 5t_{pd} + t_{on} \tag{15}$$

where T = period (s); t_{pd} = phase delay time (s); t_{on} = time of switching component for the ON condition (s); t_{off} = time of switching component for the OFF condition (s). Each switching component of the first inverter circuit (S_1 and S_3) is driven by a pulse wave with phase delay time, t_{pd} and the time of switching component for the ON condition, t_{on}. The switching components (S_2 and S_4) is driven by a pulse wave with a phase delay time as mentioned by the Eq. (11). The switching components (S_5 and S_7) of the second inverter circuit is driven by a pulse wave with a phase delay time, $2t_{pd}$ and the time of switching component for the ON condition as mentioned by the Eq. (12). The switching components (S_6 and S_8) is driven by a pulse wave with a phase delay time as mentioned by the Eq. (13). The switching components (S_9 and S_{11}) of the third inverter circuit is driven by a pulse wave with a phase delay time, $3t_{pd}$ and the time of switching component for the ON condition as mentioned by the Eq. (14). The switching components (S_{10} and S_{12}) is driven by a pulse wave with a phase delay time as mentioned by the Eq. (15).

The Eq. (10) to (15) are applied to calculate the phase delay time, t_{pd} and the time of switching component for the ON condition for each switching component on the TPVMI. The phase delay time is adjusted 0.00005 ms to 0.0045 ms for the time interval of 0.0005 ms. The result of the phase delay time, t_{pd} and the time of switching component for the ON condition, t_{on} for each switching component is shown in Table 3. Each time adjustment of switching components on the TPVMI is observed for the value of THD and decided a required time adjustment for the lowest THD.

Table 3. The phase delay time, t_{pd} and the time of switching component for the ON condition for each switching components on the TPVMI.

First inverter				**Second inverter**				**Third inverter**			
S_1, S_3		S_2, S_4		S_5, S_7		S_6, S_8		S_9, S_{11}		S_{10}, S_{12}	
t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}	t_{pd}	t_{on}
0.0005	0.009	0.0105	0.009	0.001	0.008	0.011	0.008	0.0015	0.007	0.0115	0.007
0.001	0.008	0.011	0.008	0.0015	0.007	0.0115	0.007	0.002	0.006	0.012	0.006
0.0015	0.007	0.0115	0.007	0.002	0.006	0.012	0.006	0.0025	0.005	0.0125	0.005
0.002	0.006	0.012	0.006	0.0025	0.005	0.0125	0.005	0.003	0.004	0.013	0.004
0.0025	0.005	0.0125	0.005	0.003	0.004	0.013	0.004	0.0035	0.003	0.0135	0.003
0.003	0.004	0.013	0.004	0.0035	0.003	0.0135	0.003	0.004	0.002	0.014	0.002
0.0035	0.003	0.0135	0.003	0.004	0.002	0.014	0.002	0.0045	0.001	0.0145	0.001
0.004	0.002	0.014	0.002	0.0045	0.001	0.0145	0.001	0.005	0	0.015	0
0.0045	0.001	0.0145	0.001	0.005	0	0.015	0	0.0055	0.001	0.0155	0.001

2.3.3. Comparison between equal phase delay time development method and novel adjustment method of phase delay time on TPVMI

The equal phase delay time development method and novel adjustment method of phase delay time on TPVMI system are based on the phase delay time, but there are some differences as stated below:

- In one cycle of *m*-level output voltage waveform, period, *T* is divided by four quadrants for the equal phase delay time development method. While, the period, *T* is as submission of phase delay time, time of switching component for the ON and OFF condition for the adjustment method of phase delay time.
- For the switching time of switching components, the period, *T* is divided by 2 and it is minus and added by phase delay time for the equal phase delay time development method. While, for the adjustment method of phase delay time, the switching components of each inverter circuit is driven by a pulse wave with a phase delay time and the time of switching component for the ON and OFF condition.

3. Results and Discussion

3.1. Validation of PV module modelling

The validation between PV module modelling and the data sheet of PV module as shown in Table 1 is conducted. The implementation of PV module in the TPVMI system needs one and three PV modules that they are connected together in series connection. The required voltage level in the TPVMI system is around 240 V. Therefore, one PV module and three PV modules connected in series are needed to be validated. The comparisons of simulation result and data sheet for three PV modules are shown in Figs. 5 and 6. The simulation results of open circuit voltage, V_{oc} and short circuit current, I_{sc} as PV module performances are compared to the

data sheet of PV module for the condition of constant temperature of 25 °C and various solar irradiance.

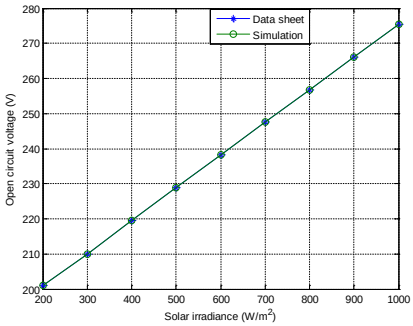


Fig. 5. Open circuit voltage of three PV modules connected in series.

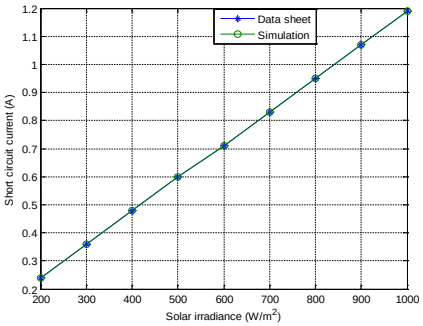


Fig. 6. Short circuit current of three PV modules connected in series.

The validations of open circuit voltage of three PV module connected in series show that *CRM* is very closer to zero, it indicates that the validation has high accuracy. The value of *CRM* is negative, it indicates that the tendencies of the simulation to over-estimate the data sheet of open circuit voltage. The value of *RMSE* is low value, it indicates that the validation has minimal value and better performance. The value of *NSE* is closer to 1, it indicates that the simulated open circuit voltage of three PV modules connected in series has high accuracy value with the data sheet. The value of *e* is 0.0772 %, it indicates that the simulated open circuit voltage of PV module connected in series is acceptable. The value of *e* is negative, it indicates that the tendencies of the simulation to over-estimate the data sheet of open circuit voltage. The validations of short circuit current of three PV module connected in series show that the value of *CRM* is zero, the value of *RMSE* is zero, the value of *NSE* is zero and the value of percentage error is zero. They indicate that the simulation is perfect (there is no different value between the simulation and data sheet).

3.2. Analysis of 7-level AC voltage waveform on TPVMI system

The TPVMI system generates 7-level AC voltage waveform for the AC load of 25 Ω. Three PV module voltage levels are needed to generate the 7-level AC voltage waveform. As shown in Fig. 3, the first inverter circuit is connected to the three PV modules that connected together in series with the output voltage of 275.4 V as the first voltage level. The second and third inverter circuits are connected to one PV module with the output voltage of 91.8 V as the second and third voltage level, respectively. The both proposed methods of equal phase delay time development method and novel adjustment method of switching time are applied to the TPVMI system to generate the 7-level AC voltage waveform. The performances of TPVMI are analysed in term of the AC voltage waveform and the THD.

3.2.1. Equal phase delay time development method

Figure 7 shows a 7-level AC voltage waveform of TPVMI system based on the equal phase delay time development method. It has $2(m\text{-}1) = 2\ (7\text{-}1) = 12$ phase delay times, t_{pd} that it is suitable with the number of switching components needed

to generate the 7-level AC voltage waveform. The name of equal phase delay time is that the level of 7-level AC voltage waveform is divided by the same time. It is due to the frequency of 7-level AC voltage waveform is 50 Hz or its period of 0.02 s and 7-level can be observed for half cycle, thus the half cycle or half period of 0.01 s is divided by seven equals 0.00143 s. It means every voltage level needs 0.00143 s. It is signed by the first phase delay time, t_{pd1} = 0.00143 s and t_{pd12} = 0.01716 s as shown in Fig. 7.

Five PV modules are needed to generate the seven level AC voltage waveform of TPVMI system with output voltage for one PV module following the Table 1. Three PV modules are connected in series to generate 3 times 91.8 V for the first inverter circuit and one PV module for the second and third inverter circuit, respectively as shown in Fig. 3. It generates four AC voltage levels (0 V, 90.935 V, 270.874 V and 448.25 V) for the first quadrant (0 to 0.005 s) as shown in Fig. 7.

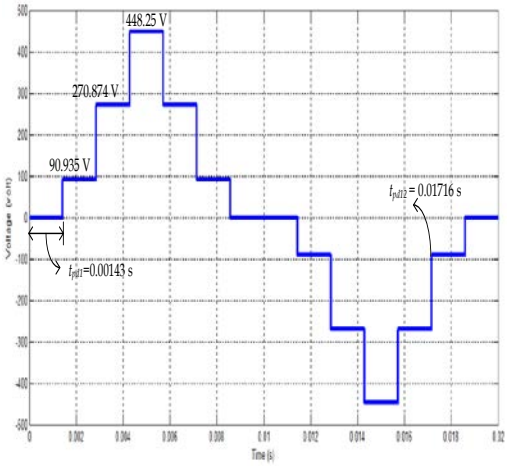


Fig. 7. Seven level AC voltage waveform of TPVMI system based.

The total harmonic distortion (THD) is observed until the harmonic order-19 for the of 7-level AC voltage waveform of TPVMI system based on the equal phase delay time development method as shown in Fig. 8. It contents the even and odd harmonic order whereas that the percentage of odd harmonic order is higher than the magnitude of even harmonic order. The fundamental voltage or the voltage magnitude on the harmonic order-1 is 300.7 V as shown in Fig. 8.

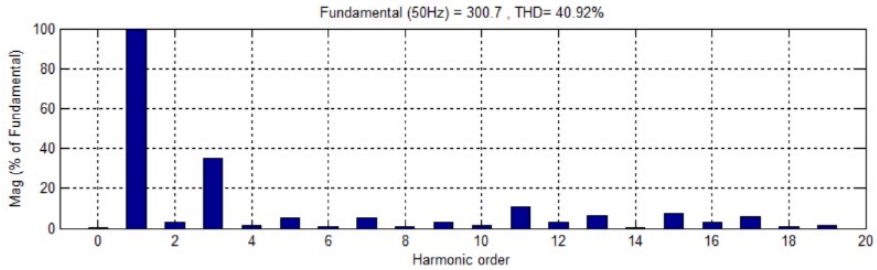


Fig. 8. Harmonic order of seven level AC voltage waveform of TPVMI system based on the equal phase delay time development method.

Figure 9 shows the voltage magnitude on each harmonic order which it is interpreted from the percentage of harmonic order in Fig. 8. The main objective of Fig. 9 is to calculate the THD for applying the Eq. (5). The calculation THD of 39.59% is almost same with the simulation THD of 40.92%. Its error percentage is -3.25%, the negative sign indicates that the calculation THD is lower than the simulation THD.

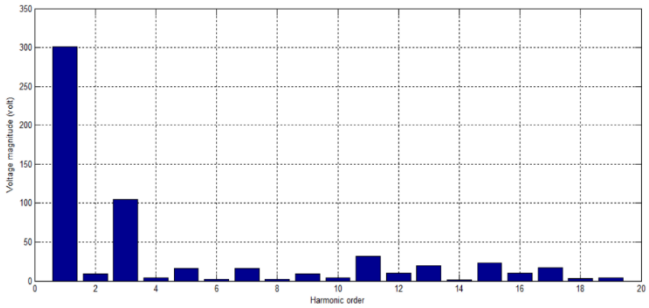


Fig. 9. Voltage magnitude of each harmonic order of seven level AC voltage waveform of TPVMI system based on the equal phase delay time method.

3.2.2. Novel adjustment method of phase delay time

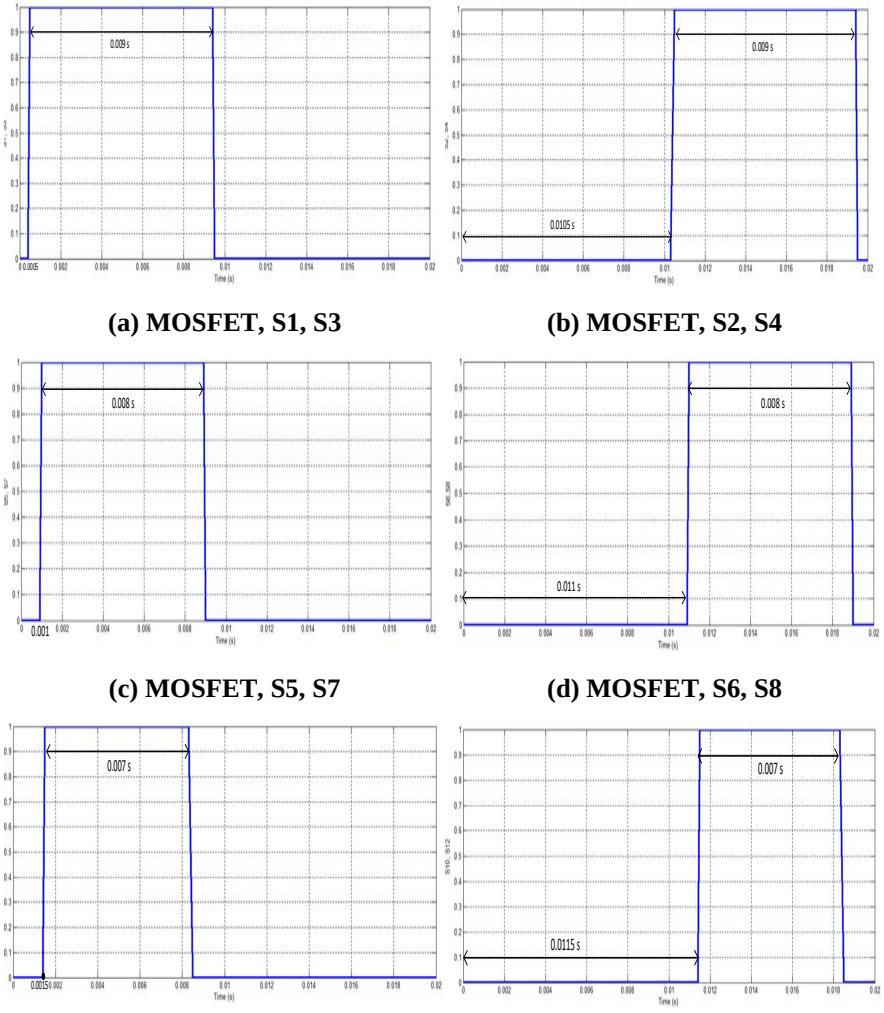
The novel adjustment method of phase delay time, t_{pd1} and the time of switching component for the ON condition, t_{on} as shown in Table 3 have been tested into the modelling of TPVMI system as shown in Fig. 2. Its main objective is to analyse the performance of TPVMI system in term of the pulse generator, 7-level AC voltage waveform and THD. The best performance is achieved for the lowest THD. One by one of the phase delay time of MOSFET S1 is tested to obtain the lowest THD following the phase delay time and the time of switching component for the ON condition of the other MOSFETs. For this condition, the lowest THD is achieved for the phase delay time, t_{pd1} = 0.0005 s of MOSFET S1. It is used to analyse the performance of TPVMI system.

Figure 10 shows the pulse generators for each switching components of the TPVMI system based on the novel adjustment method for the phase delay time of 0.0005 s. There are two pairs of switching components (MOSFETs) that have same pulse generator. It means that the number of pulse generator has been reduced if it is compared to the conventional cascaded multilevel inverter.

The pair of switching components that has the same pulse generator are MOSFET1 (S1) and MOSFET3 (S3), MOSFET2 (S2) and MOSFET4 (S4), MOSFET5 (S5) and MOSFET7 (S7), MOSFET6 (S6) and MOSFET8 (S8), MOSFET9 (S9) and MOSFET11 (S11), MOSFET10 (S10) and MOSFET12 (S12).

The pair MOSFET1 (S1) and MOSFET3 (S3), MOSFET5 (S5) and MOSFET7 (S7), MOSFET9 (S9) and MOSFET11 (S11) generate the positive half cycle of seven level AC voltage waveform.

The pair of MOSFET2 (S2) and MOSFET4 (S4), MOSFET6 (S6) and MOSFET8 (S8), MOSFET10 (S10) and MOSFET12 (S12) generate the negative half cycle of seven level AC voltage waveform. The different between the phase delay time in one MOSFET and the others generate the level time range of 7-level AC voltage waveform.



(a) MOSFET, S1, S3 **(b) MOSFET, S2, S4**

(c) MOSFET, S5, S7 **(d) MOSFET, S6, S8**

(e) MOSFET, S9, S11 **f) MOSFET, S10, S12**

Fig. 10. Pulse generators for each switching components of the TPVMI system based on the adjustment method for t_{pd1} = 0.0005 s.

By applying the novel adjustment method of phase delay time for t_{pd1} = 0.0005 s with the pulse generators as shown in Fig. 10, thus the TPVMI system generates a 7-level AC voltage waveform as shown in Fig. 11. It is due to the three PV modules are connected to the first inverter circuit and one PV module for the second and third inverter circuit, respectively, thus the TPVMI system generates four AC voltage levels (0 V, 90.935 V, 270.874 V and 448.25 V) for the first-time quadrant (0 to 0.005 s) as shown in Fig. 11. The AC voltage level of 448.25 takes a long time of 0.007 s for the half cycle of 7-level AC voltage waveform and it affects the performance of TPVMI system, especially on the THD.

Figure 12 shows the harmonic order of 7-level of the TPVMI system based on the adjustment method of phase delay time for various t_{pd1} on the MOSFET1 (S1). The

harmonic order is observed until the harmonic order-19. It also shows that the percentage of odd harmonic is higher than the percentage of even harmonic order. Figure 12 (a) shows the harmonic order for t_{pd1} = 0.0005 s. The harmonic order-1 shows the fundamental harmonic with its percentage of 100%, it represents the fundamental voltage magnitude of 533.8 V. The percentages of odd and even harmonics are achieved as comparison of the fundamental harmonic order. The percentage of THD is 20.76 % as shown in Fig. 12(a). It shows that the percentage of THD for the adjustment method of phase delay time for t_{pd1} = 0.0005 s is lower than the percentage of THD for the equal phase delay time development method on the TPVMI system. It also shows that the performance of TPVMI system for the novel adjustment method of phase delay time for t_{pd1} = 0.0005 s is better than the performance of TPVMI system for equal phase delay time development method.

Figure 13 shows THD of 7-level TPVMI system for various phase delay time of MOSFET1 (S1). The phase delay time is adjusted and applied into the modelling of TPVMI system as shown in Fig. 2 with interval range of phase delay time of 0.0005 s. It shows that if the higher of the phase delay time causes the higher of THD of the TPVMI system. It is caused by the longer time of AC voltage level of 0 V and the shorter time of AC voltage level of 448.25 V. The lowest THD is achieved for the phase delay time, t*pd1* = 0.0005 s and it indicates the best performance of TPVMI system.

A result comparison between the equal phase delay time development method and novel adjustment method of phase delay time is shown in Table 4. It is compared for the novel adjustment method with the phase delay time on the first level of 0.0005 s. Some parameters are shown in Table 4 which they are related to the THD generation in the TPVMI system. The results show that both methods have same maximum voltage of 448.25 V, it is due to each method is supplied by the same PV module as main DC voltage source.

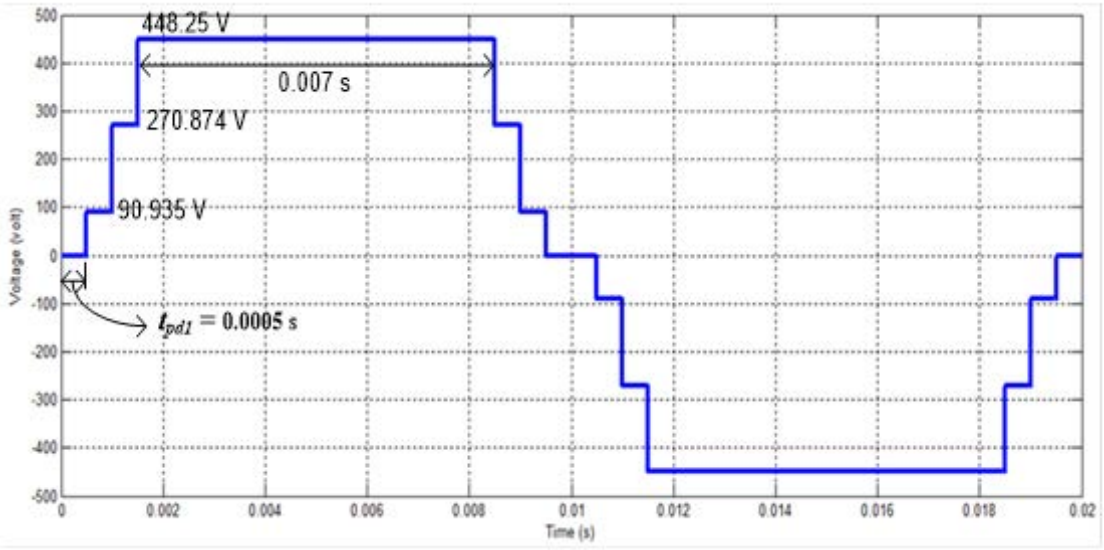
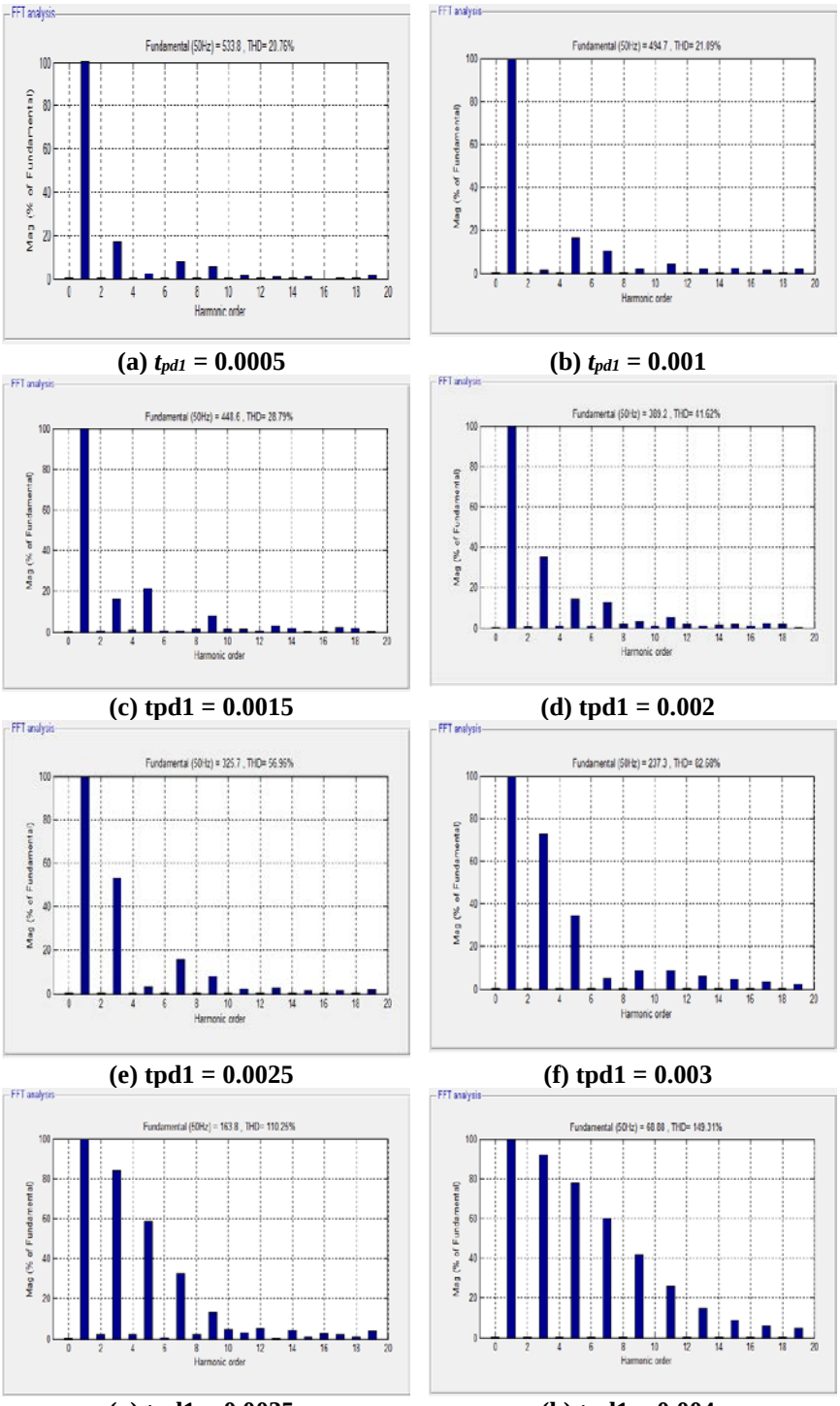


Fig. 11. Seven level AC voltage waveform of the TPVMI system based on the adjustment method for phase delay time for t_{pd1} = 0.0005 s.



(a) t_{pd1} = 0.0005 **(b) t_{pd1} = 0.001**

(c) tpd1 = 0.0015 **(d) tpd1 = 0.002**

(e) tpd1 = 0.0025 **(f) tpd1 = 0.003**

(g) tpd1 = 0.0035 **(h) tpd1 = 0.004**

Fig. 12. Harmonic order of seven level of the TPVMI system based on the novel adjustment method of phase delay time with various t_{pd1}.

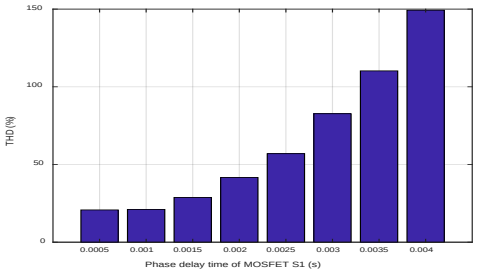


Fig. 13. THD of seven level TPVMI system for various phase delay time of MOSFET1 (S1).

Table 4. Result comparison between equal phase and adjustment of phase delay time

Parameters	Method	
	Equal phase delay time	Adjustment of phase delay time
Maximum voltage (V)	448.25	448.25
Phase delay time on the first level (s)	0.00143	0.0005
Maximum phase delay time (s)	0.00143	0.007
Voltage magnitude of the first harmonic (V)	300.7	533.8
THD (%)	40.92	20.76

The output voltage waveform generated by the equal phase delay time method has same time of 0.00143 s for the phase delay time on the first level and maximum phase delay time, it shows that the method is correct. While the output voltage waveform generated by the novel adjustment method of phase delay time has the phase delay time on the first level of 0.0005 s and maximum phase delay time of 0.007 s. The phase delay time on the first level generated by the novel adjustment method of phase delay time is shorter than the equal phase delay time method. Inversely, the maximum phase delay time generated by the novel adjustment method of phase delay time is longer than the equal phase delay time development method.

A longer maximum phase delay time gives a better capability in the voltage magnitude generation of the first harmonic. Therefore, the voltage magnitude of the first harmonic of 533.8 V generated by the novel adjustment method of phase delay time is higher than the voltage magnitude of the first harmonic of 300.7 V generated by the equal phase delay time development method.

A higher voltage magnitude of the first harmonic also gives a better capability in the THD reduction of TPVMI system. It is due to the voltage magnitude of the first harmonic is inversely proportional to the THD as stated by the Eq. (5). Therefore, the THD of 20.76 % generated by the novel adjustment method of phase delay time is lower than the THD of 40.92 % generated by the equal phase delay time development method. The THDs generated by the both methods do not fulfil the IEEE standard 519™-2014, it is due to the modelling of TPVMI systems do not include a LC filter to eliminate the individual harmonics. In the condition without LC filter shows that the THD of 20.76 % generated by the novel adjustment method of phase delay time is still better than the THD of 27.55 % proposed by Hamzah et al. [30] and THD of 27.70 % proposed by Yarlagadda et al. [31] for the same 7-level inverter.

4. Conclusions

This paper presents a novel adjustment method of phase delay time and equal phase delay time development method on the TPVMI system for reducing the THD. Three inverter circuit are constructed and connected in the cascaded connection to generate 7-level AC voltage waveform. The first inverter circuit is connected to three PV modules connected in series. The second and third inverter circuit are connected by one PV module, respectively. The TPVMI system is modelled using SIMULINK MATLAB and can be concluded as stated below.

- A novel phase delay time adjustment method and equal phase delay time development method are proposed on the TPVMI system to achieve the lowest THD. These methods have advantage to reduce the number of pulse wave generator compared to the existing methods.
- The PV modelling is compared between simulation result and data sheet. It shows that the simulation result is valid with the data sheet based on the statistical analysis (root mean squared error (*RMSE*), coefficient of residual mass (*CRM*), percentage error (*e*) and Nash-Sutcliffe equation (*NSE*)).
- The equal phase delay time development method and novel phase delay time adjustment method are proposed to generate the 7-level AC voltage waveform. They show that the novel phase delay time adjustment method is better compared to the equal phase delay time development method because the novel phase delay time adjustment method for t_{pd1}=0.0005 s on the MOSFETS1 (S1) produces the lower THD than the equal phase delay time development method.

Nomenclatures

m	m-level of multilevel inverter
T	Period
t_{off}	Time of switching component for the OFF condition
t_{on}	Time of switching component for the ON condition
t_{pd}	Phase delay time
$t_{pd(3m-1)/2}$	Phase delay times in the fourth time quadrant
$t_{pd(m+1)/2}$	Phase delay times in the second time quadrant
t_{pdm}	Phase delay times in the third time quadrant
$V_{dat,i}$	Data sheet of PV module open circuit voltage at i data
V_n	Voltage magnitude of n^{th} harmonic
$V_{sim,i}$	Simulated open circuit voltage of PV module at i data
Θ	Switching angle

Abbreviations

AC	Alternating Current
CRM	Coefficient of Residual Mass
DC	Direct Current
NSE	Nash-Sutcliffe Equation
PV	Photovoltaic
PWM	Pulse Width Modulation
RMSE	Root Mean Squared Error
THD	Total Harmonic Distortion

TPVI	Transformerless Photovoltaic Inverter
TPVMI	Transformerless Photovoltaic Multilevel Inverter

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