

BER-SNR PERFORMANCE OF NOMA SYSTEMS OVER RAYLEIGH FADING CHANNELS USING REAL- TIME FPGA

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Abstract

In this paper, non-orthogonal multiple access (NOMA) system for two-users communications is designed and implemented using a real-time field-programmable gate array (FPGA) technique. The generated NOMA signals are assumed to be passed through Rayleigh fading channels along with additive white Gaussian noise (AWGN) at each user's terminal. Furthermore, successive-interference cancellation (SIC) is applied at each terminal to remove the interference caused by other user's signals. This is achieved by detecting the interfered signal, after zero-forcing (ZF) channel equalization, and then subtracts it from the overall NOMA signal. Moreover, the performance analysis of this system is measured by obtaining the bit-error-rate (BER) against different values of signal-to-noise ratio (SNR). Moreover, the BER-SNR results are compared with the results obtained by Monte-Carlo simulation via Matlab showing exact-close matching.

Keywords: Additive white Gaussian noise (AWGN), Non-orthogonal multiple access (NOMA), Rayleigh fading channels, Successive interference cancellation (SIC), Zero-forcing (ZF).

1. Introduction

Non-orthogonal multiple access (NOMA) is one of the promising techniques that suggested for the next generations of wireless communication, the 5th generation (5G), and beyond. NOMA can increase the capacity of the system, reduce the latency, and improve the connectivity and the user-fairness [1]. Moreover, NOMA outperforms conventional schemes of multiple accesses (MA)'s as frequency division/time division multiplexers, which are used in the global system of mobile communication (GSM) [2]. Furthermore, NOMA with successive interference cancellation (SIC) has better performance and higher throughput comparing to the conventional orthogonal frequency division multiplexing (OFDM) [3]. Different techniques are proposed for NOMA in the code and the power domains [4], in which the latter is the main focus of this paper. The theory of power domain NOMA can be summarized by sharing the available power at the transmitter between the users under the coverage [1, 5]. However, the power is not divided equally among the users, as a power allocation criterion is utilized to manage this process. In other words, the users with high attenuation channels, i.e., the furthest users from the source, are given a higher portion of the total power, while the user near to the transmitter, which has low attenuation channels, are allocated less power. This is to satisfy user-fairness and acceptable connectivity for all users [5, 6]. Furthermore, SIC is required to be accompanied by the power domain NOMA to mitigate and reduce the effect of interferences which are caused by other users [7].

In the previous works related to NOMA-based wireless communications, NOMA is employed in [8] to be the technique of utilizing millimetre-wave over massive multiple-input multiple-output (MIMO), to enhance the throughput of the next generation of wireless communications. In [7], the performance analysis of power-domain NOMA for multiple users over Rayleigh fading channels, in which the outage probability and the probability of errors are evaluated and showed exact-close matching with simulations. Moreover, the uplink and downlink NOMA over fading channels is considered in the presence of SIC errors, in which the bit-error-rate performance is evaluated in [9]. Simulink via Matlab is implemented for NOMA over AWGN and Rayleigh fading channels in [10] and the performance is evaluated. In [11], the authors have implemented an FPGA realization of maximum ratio combining along with exponent optimization for adaptive antennas array. Moreover, Rayleigh and Rician propagation channels are obtained in [12] by using an FPGA simulator, in which independent samples having Gaussian distribution with zero mean are passed through a spectrum shaping filter.

We exploit a field-programmable gate array (FPGA) to design and implement real-time NOMA. FPGA is a promising and attractive mechanism that offers ease and flexible modification for the designed systems with higher throughput [13, 14]. In the literature, FPGA is utilized to design and implement different real-time communications and signal processing algorithms. In the literature, MIMO with OFDM is implemented based on FPGA with iterative detection in [15] and for multi-users as in [16]. In [17], the consumed power and the performance of wireless communications based-FPGA are evaluated by employing efficient and modern algorithms. In our previous work in [1], NOMA is designed and implemented for two users over AWGN channels only. This means that there are no fading channels between the source and the users, which consequently leads to a low complex receiver that does not require equalization at each terminal.

The main contributions of this research paper are to extend our previous work in [1] by evaluating the BER-SNR performance for a single-input single-output real-time NOMA system over Rayleigh flat fading and AWGN channels using FPGA and compare the proposed system's performance with the results obtained by Monte-Carlo simulations via Matlab. Moreover, the required circuits to implement the overall system achievement are designed and implemented such as the multiplication process for simulating the passing of NOMA signal over the flat fading channels and the division process for equalizations at each receiver. To the best of our knowledge, these contribution aspects have not been covered thoroughly in the previous state-of-the-art as NOMA over Rayleigh fading channels is presented in this work for different scenarios. Moreover, the system is implemented using FPGA and the results are validated using Matlab showing exact-closed matching. Moreover, it noteworthy that the main goal of this paper is to build hardware architecture using FPGA for multi-user NOMA systems over the Rayleigh fading channel, which is the real channel for wireless communications. Furthermore, dealing with a more realistic wireless channel, which is the Rayleigh fading channel requires using the multiplication process to multiply the transmitted symbols with the modelled complex values of the Rayleigh fading channel. At the receiver, the division process is used to equalize the symbols using a zero-forcing equalizer. In this work, the complex multiplication and division operations are designed for these purposes, which were not utilized in [1].

2. System Modelling and Assumptions

Single-input single-output NOMA system is assumed in this paper, in which the transmitter serves two-users with different channels conditions, i.e., the channels between the transmitter and the two receivers are assumed as flat Rayleigh fading channels with different attenuation factors. For user-fairness and optimum connectivity, the NOMA technique is applied by allocating a particular power factor for each user to participate in the available power at the transmitter. More specific, the furthest user from the transmitter denoted as U_F is given a higher value of the total transmitted power P_T , while the rest of the power is given to the nearest user U_N . Moreover, we assume quadrature phase-shift keying (QPSK) is utilized as a modulation scheme. Additionally, the presence of independent AWGN is assumed to be added to the received signals at each user's terminal. The power allocation factor for the far and near users are denoted as, β_F and β_N , respectively, where $\beta_F + \beta_N = 1$, and $\beta_F > \beta_N$.

The received signal at the i^{th} user can be expressed as

$$r_i = h_i(\sqrt{\beta_i P_T} s_i + \sqrt{\beta_l P_T} s_l) + n_i \quad i, l \in \{F, N\}, i \neq l, \quad (1)$$

where $h_i \sim CN(0,1)$ represents the channel between the source and the i^{th} user, which is assumed as a flat Rayleigh fading channel with zero mean and variance equal to one.

Furthermore, $n_i \sim CN(0, \sigma_n^2)$ is to represent the AWGN added to the received signal at the i^{th} user's terminal with zero mean and variance equal to σ_n^2 . Additionally, we assume that $|h_N|^2 > |h_F|^2$, which means that the furthest user has a higher attenuation factor than the nearest user. The transmitter data are mapped using a QPSK modulation scheme to create the symbols s_F and s_N , which are belongs to $\{\pm 1 \pm j\}$. Furthermore, the signal-to-interference-plus-noise ratio at the i^{th} user, which denoted as γ_i , can be expressed from Eq. (1) as

$$\gamma_i = \frac{\beta_i P_T |h_i s_i|^2}{\beta_l P_T |h_l s_l|^2 + n_i^2} = \frac{\beta_i P_T |h_i|^2}{\beta_l P_T |h_l|^2 + \sigma_n^2} = \frac{\Omega_i |h_i|^2}{\Omega_l |h_l|^2 + 1}, \quad (2)$$

where $\Omega_l = \frac{\beta_l P_T}{\sigma_n^2}$ and $\Omega_i = \frac{\beta_i P_T}{\sigma_n^2}$ represent the interference-to-noise ratio (INR) and the signal-to-noise ratio (SNR), respectively.

NOMA for downlink communications:

Figure 1 shows the NOMA system in the downlink mode, in which a base station (BS) is used to serve two users with different channels circumstances. Moreover, Rayleigh flat fading channels with different attenuation factors are considered to be the wireless media between the BS and the two users. The notation h_N and h_F are used to represent the channels between the BS from the side and the near and far users from another side, respectively, where $|h_N|^2 > |h_F|^2$, which means that lower attenuation is assumed for the near user due to path loss phenomena.

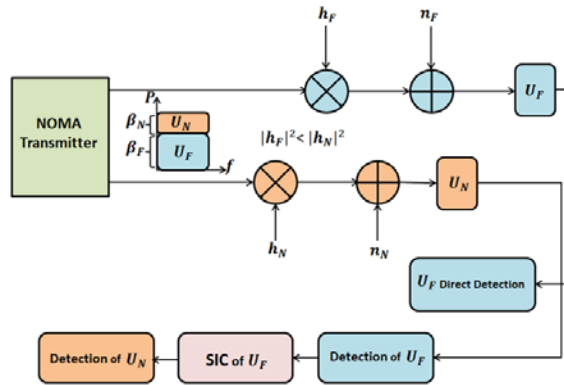


Fig. 1. NOMA in the downlink phase for two users $|h_N|^2 > |h_F|^2$.

Figure 2 shows the block diagram of the design architecture, which is designed using Spartan 3e, with a slice number Xc3s500e. The family of this starter kit contains a convenient development embedded board that can implement different signal processing and communications systems. This is since this kit has a large volume of electronic circuits with very low-cost [13, 18].

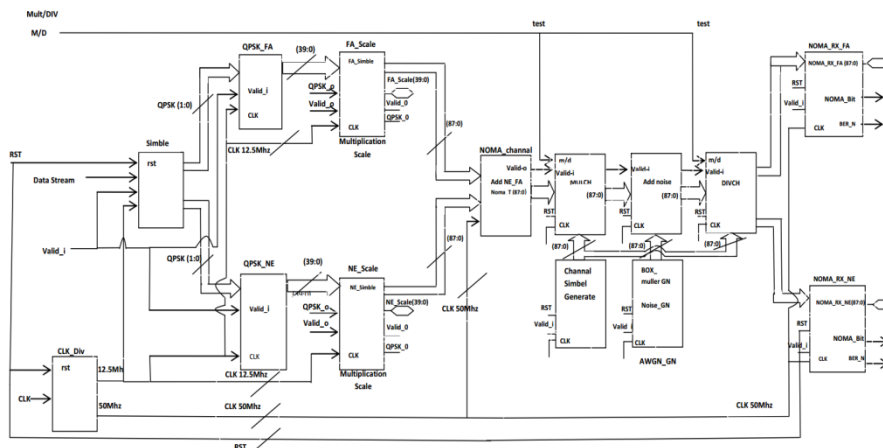


Fig. 2. The block diagram of the NOMA system over Rayleigh fading channel in the presence of AWGN as designed using FPGA. All notations are explained in Table 2 in Appendix A.

As most of the communication and signal processing applications require the multiplication process, especially for floating numbers, we use the IEEE arithmetic standard for floating-point, which is denoted as IEEE-754. The designed multiplication process is achieved by utilizing the Xilinx ISE design suite, which is used to multiply two floating numbers, each of which may have two decimal digits only. Figure 3 shows the designed multiplication process which contains the control circuit that is used for synchronization purposes and to control all the processing signals. The circuit is accompanied by a register to process 64-bits denoted as multiplicand Reg.64 in the figure.

Moreover, the arithmetic logic unit ALU is responsible for adding the current and previous process after shifting the multiplicand register one decimal digit to the left. The shifting process is achieved depending on the 32-bits multiplier inherent and controlled by the shift right register. The latter is used to shift the multiplicand one bit to the right every cycle of the multiplication process, which is controlled as mentioned previously by the unified clock of the circuit.

Finally, it is required to accumulate all the results in the 64-bit accumulator to obtain the final result. It is noteworthy that the accumulator is controlled by three signals which are load, shift and clear to enable loading of a new number, shifting the multiplicand every cycle of multiplication, and clearing at the end before new data is entered, respectively. This operation is used in our FPGA simulation for multiplying the NOMA signal, which was created from the QPSK signals of the two users after applying the power allocation factor, with the Rayleigh flat fading channel coefficients. Moreover, the shifting and accumulation processes are shown in Fig. 4.

Furthermore, a division is required at each user's receiver to apply zero-forcing (ZF) equalization, where the received NOMA signal at each node, which is passed through the Rayleigh flat fading and AWGN channels, needs to be equalized by passing through a division process. This is to divide the NOMA signal by the channel passed through it, which is known to the receiver as we assume in this paper. We implement this processing by shifting the float decimal number one bit to the right. It is noteworthy that the IEEE arithmetic standard for floating-point (IEEE-754) is used to calculate the multiplicands of the floating-point numbers.

Moreover, the designed division circuit is suitable for two decimal digits only. Figure 5 shows the designed algorithm utilized for this purpose, in which the control circuit generates a timing clock to ensure the synchronization of all processes. The division is started by dividing a dividend (z) by a divisor (d) to produce the quotient (q) and the remainder of the division (s).

To resume the process the dividend is shifted one bit to the left every division cycle by the 64-bits shifter, to be ready for the subtraction process of the new result from the previous one. These steps are taken place inside the 64-bit ALU to produce the division remainder and the quotient. To complete this process, the quotient is shifted one bit to the left every division cycle too. Additionally, the quotient is examined by the end of the division by using the equation, $z = q \times d + s$, to confirm the result. Two signals which are denoted as load and clear are used to control loading and clearing the remainder every cycle of division.

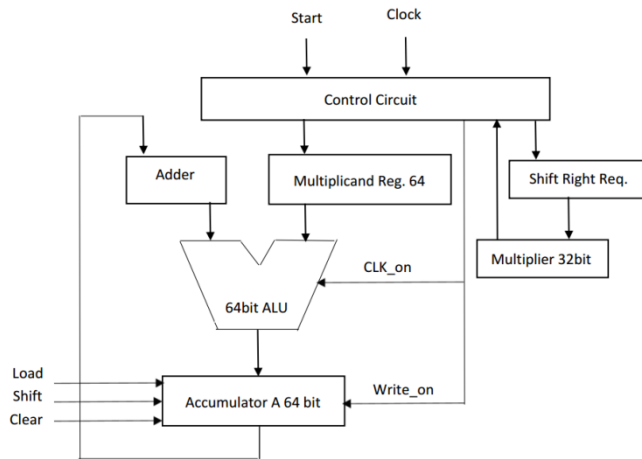


Fig. 3. Multiplication process circuit.

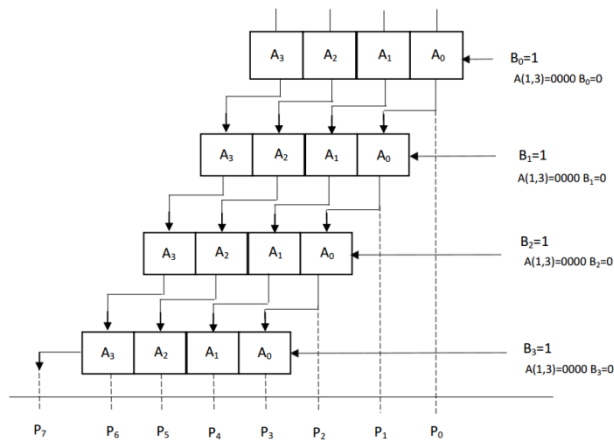


Fig. 4. Multiplication flow diagram by applying the shifting and accumulation process.

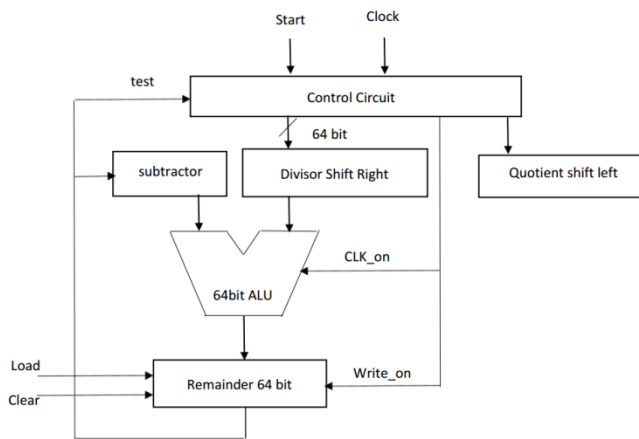


Fig. 5. Division process in FPGA.

3. Simulation Results

In this paper, the real-time single-input single-output NOMA system is designed and implemented over a flat Rayleigh fading channel, along with the AWGN channel. Two users are considered to be served by a transmitter in the downlink mode. We assume the furthest user with a power allocation factor of $\beta_F = 0.6$, while the near one has given $\beta_N = 0.4$, where the absolute powers of the channels between the transmitter and two users are assumed as $|h_F|^2 = -3$ dB and $|h_N|^2 = 0$ dB for the far and near users, respectively. For synchronization, two frequencies are used in our FPGA design, which is 50 MHz and 12.5 MHz, both are obtained by using the frequency divider of the main clock source.

Figure 6 shows the generation of NOMA signal created by combining two scaled QPSK signals for two different users, i.e., near and far users with the above channel specifications. The QPSK signal for the near user is scaled by using the power allocation factor of $\sqrt{\beta_N} = \sqrt{0.4} = 0.63$, while the signal of the far user is scaled by $\sqrt{\beta_F} = \sqrt{0.6} = 0.77$. The newly created NOMA symbol is then passed through different Rayleigh flat fading channels to reach the targeted receiver of those users as shown in Fig. 7. The passing through these channels is achieved in our FPGA design by multiplying the NOMA symbols with a vector of these channels which have the same length, i.e., point by point multiplication using the circuit explained in the previous section. Moreover, Fig. 7 shows also the AWGN denoted by *noise*, which is generated by using the Box-Muller approach utilized and explained in detail in our previous work in [1] and more details about this approach can be read in [19, 20]. It is noteworthy that the AWGN for each user is generated independently.

In Fig.8, the NOMA symbols of the far and near users after passing through the channels are denoted as *rayleigh-fa-rx* and *rayleih-ne-rx*, respectively. Moreover, the noises are added to these two vectors at each user's terminal to create the received symbols which denoted in our FPGA design as *mul-add-noise*. To detect the symbols in each user's terminal, equalization by employing the ZF method is exploited by dividing the received signal by channel, i.e., h_F and h_N for the far and near the receiver, respectively. In this paper, we assume that the channels as known to their corresponding receivers as channel estimation are out of the scope of this paper. At the near user's receiver, the equalized symbols after applying ZF is denoted as *div-ch* are used to detect first the symbols related to the far user by applying the Euclidean distance formula with the four symbols of QPSK constellation. This is to find the minimum distance demonstrating the original transmitted far symbols. The detected far symbols are then subtracted from the overall equalized NOMA symbols to yield the transmitted near signals. This mechanism is what is called SIC as mentioned in the introduction section. The Euclidean distance process is repeated after subtraction to find the correct symbol position in the QPSK constellation.

It is worth to note that due to NOMA definition, direct detection of the received symbols might be implemented at the furthest user without applying SIC, due to the higher value of its allocated power, and by considering the small portion of near user power as just noise. Therefore, the receiver at the far user has less complexity than the receiver near to the source.

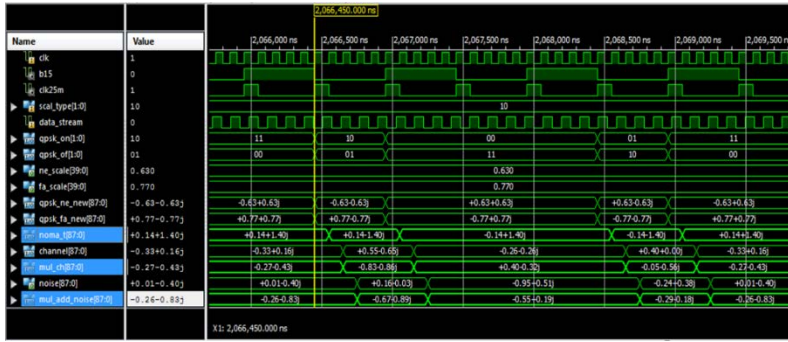


Fig. 6. NOMA generation at the transmitter for downlink mode, along with multiplication process with the generated Rayleigh fading channel and adding Gaussian noise with SNR=15 dB to the received signal.

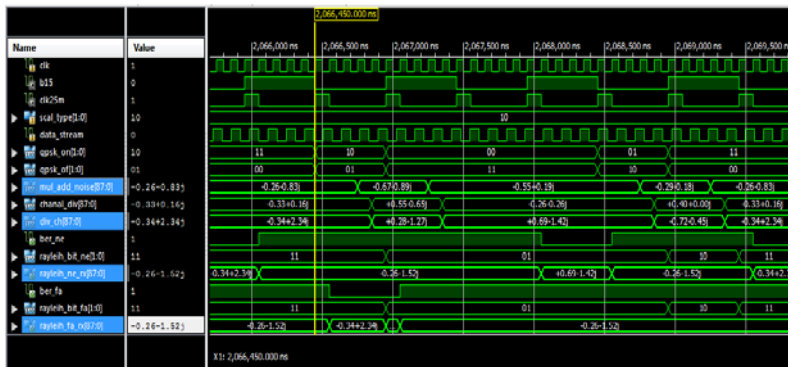


Fig. 7. NOMA generation at the transmitter for downlink mode, along with multiplication process with the generated Rayleigh fading channel and adding Gaussian noise with SNR=15 dB to the received signal.

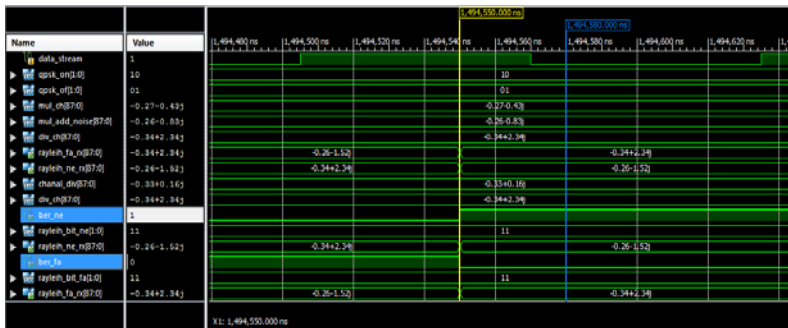


Fig. 8. The NOMA of two users signal after passing through two uncorrelated Rayleigh flat fading channels.

To confirm the ability of our designed receiver, which works at limited-interference circumstances, we put the bottom called md which has two cases defined as $md \in \{0,1\}$. When $md = 0$, this makes the AWGN=0 to confirm that the equalization and the SIC achieve accurate performance with zero error. We found that all symbols are positioned in their correct location on the QPSK

constellation. Moreover, when $md = 1$ as shown in Fig. 9, the receiver adds noise as usual depending on the required signal-to-noise ratio to measure the bit error rate (BER). The BER at the far and near users, which are denoted as ber_{fa} and ber_{ne} , respectively, are obtained by counting the number of symbols received erroneously and divide the result by the total transmitted symbols, then by dividing this value by $\log_2(4)$, for QPSK, to obtain the exact BER.

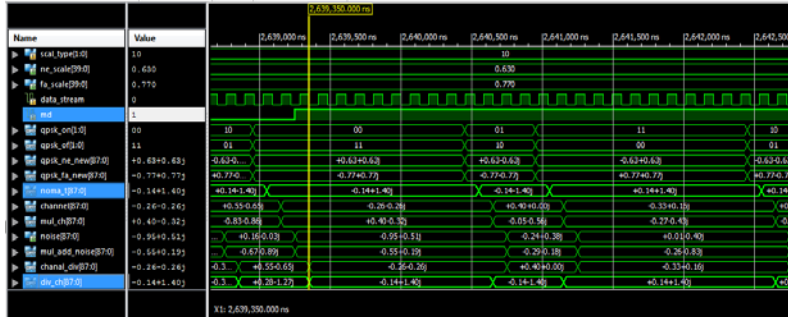


Fig. 9. The multiplication process of NOMA signal with the Rayleigh flat fading channel, adding AWGN followed with channel equalization via division process.

Table 1 shows the used, available, and consumed percentage of the logic utilization for our NOMA design over Rayleigh fading channels by using the Xc3s500e Spartan-3e kit. This logic utilization contains the number of slices, slice flip-flops, a look-up table for 4-inputs, the bounded input-output blocks (IOB)s and the global clock (GCLK). It can be seen that the utilization percentage is below the maximum availability of the kit capacity.

Table 1. Approximation summary of device utilization for the Xc3s500e Spartan-3e FPGA kit.

Logic Utilization	Used	Available	Utilization
Number of slices	1486	4656	31%
Number of slices Flip Flops	145	9312	1%
Number of 4 input LUTs	2684	9312	28%
Number of bonded IOBs	184	232	79%
Number of GCLKs	2	24	8%

The FPGA simulation is run several times to evaluate the BER at SNR=0 dB to 80 dB with a step of 10 dB and for two values of the power allocation factor (β), i.e., $\beta_F = 0.6$ and $\beta_N = 0.4$ for the far and near users, respectively. Furthermore, we run a Monte-Carlo simulation by using Matlab to simulate the designed system under the same conditioned mentioned above for validation purposes. It is worth noting that the same real-time proposed NOMA system, which was achieved in FPGA, with all considered parameters are taken into account in this simulation to prove the results obtained by the FPGA simulator. As shown in Fig. 10, the results show exact-close matching with the results obtained via Matlab simulation. In this figure, we have made comparisons with our previous work in [1], in which the latter was for the same system but over AWGN channels only, whereas in this work we extend the system to be more realistic by working over Rayleigh fading channels and in the presence of AWGN channel too. Although the performance over

Rayleigh fading channels looks worse, this is due to the effect of the fading of the channel in the real-world of wireless communications.

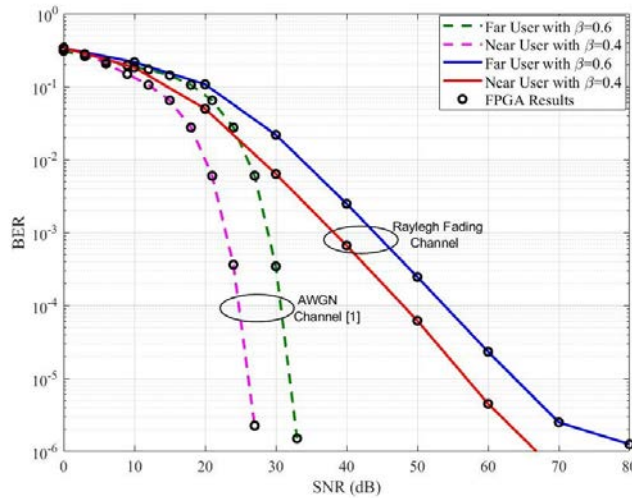


Fig. 10. BER vs. SNR for the designed NOMA system with the results obtained by FPGA simulation showing exact-close matching over Rayleigh fading and AWGN channels as in [1]. Far and near channels are with attentions -3 dB and 0 dB, respectively.

Finally, Fig.11 shows the constellations of 16-NOMA symbols, which created from adding two QPSK symbols for two users each of which is scaled with $\beta_F = 0.6$ and $\beta_N = 0.4$. The figure shows the constellation before and after the effects of Rayleigh flat fading channel and 40dB of AWGN. Additionally, the QPSK for the near user symbols after applying SIC at its receiver is shown too. It is noteworthy that the far and near channels are with attenuation power equal to -3 dB and 0 dB, respectively.

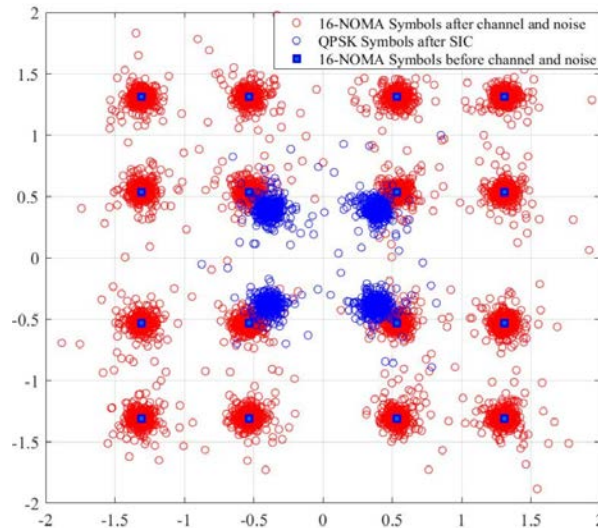


Fig. 11. The constellations of 16-NOMA symbols before and after the channel and noise, along with the QPSK for the Near user symbols after applying SIC.

4. Conclusions

In this paper, two users communicate with a BS in the downlink mode has been considered, in which the designed and implemented system has been achieved via real-time FPGA technique. The signal of NOMA, which contained the summation of the two users, has been assumed to be passed through two independent Rayleigh fading channels then uncorrelated AWGN is added to this signal at each receiving terminal. The effects of the channels have been removed at each receiver by utilizing ZF equalization, followed by applying the SIC mechanism to remove the effect of interference caused by other users. Moreover, multiplication and division processes have been designed and implemented to multiplying the channels with the NOMA signal and for equalization purposes, respectively. The BER vs. SNR performance has been obtained for each user by using FPGA and Matlab simulations which reveal exact-close matching that validate the designed real-time system.

Nomenclatures

P_T	Total transmitted power
U_F	Furthest user from the transmitter
U_N	Nearest use from the transmitter

Greek Symbols

β_F	Power allocation factor for the far user
β_N	Power allocation factor for the near user
γ_i	Signal-to-interference-plus-noise ratio at the i^{th} user

Abbreviations

5G	5 th generation
ALU	Arithmetic logic unit
AWGN	Additive white Gaussian noise
BER	Bit-error-rate
BS	Base station
FPGA	Field-programmable gate array
GSM	Global system of mobile communication
MA	Multiple accesses
MIMO	Multiple-input multiple-output
NOMA	Non-orthogonal multiple access
OFDM	Orthogonal frequency division multiplexing
QPSK	Quadrature phase-shift keying
SIC	Successive-interference cancellation
SNR	Signal-to-noise ratio
ZF	Zero-forcing

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Appendix A

Table 2. Signals abbreviations with their names and functions in Fig. 2.

index	Signal abbreviation used In the Paper	Signal Name	Purpose of Using the Signal
1	Data-Stream	Data Stream	Serial Data Stream Input
2	RST	Reset	Reset the operation of the System
3	Valid_i	Valid Input Signal	When the value of the signal is '0' it mean the data stream input are not readable and these data stream will be just ignored while when this signal is '1' it mean the data stream input are readable
4	CLK	Clock	System Clock Frequency (50MHz)
5	CLK- Div	Clock Divider	System Clock Frequency (50MHz,12.5MHz)
6	QPSK(1:0)	Quadrature Phase shift Keying bits	Two bits are used for QPSK signal for output symbol block
7	QPSK-o	QPSK output	QPSK output Clock Frequency used for Synchronization process
8	Valid-o	Valid Output	Valid output signal used to enable receiving data input stream
9	QPSK-NR	QPSK for the Near Used	Mapping of two bits QPSK Symbol for the Near user

10	QPSK-FA	QPSK for the FAR used	Mapping of two bits QPSK Symbol for the Far user
11	FA-Scale	FAR Scale	Far user Symbol Scaling using the power allocating technique mechanism
12	NE-Scale	Near Scale	Near user Symbol Scaling using the power allocating technique mechanism
13	FA-Scale(39:0)	Far Scale For 40 bits	Far Scale Indication technique
14	NE-Scale(39:0)	Near Scale For 40 bits	Near Scale Indication technique
15	NOMA-Channel	NOMA channel	Adding the FAR and the NEAR Symbols along with adding the AWGN which generated by BOX Muller method technique
16	BOX-Muller-GN	BOX Muller Generation	Block Diagram used for AWGN Symbol Generator
17	NOMA-RX-FA	Receiving the FAR NOMA user	The NOMA signal for the FAR user which Received
18	NOMA-RX-NE	Receiving the NEAR NOMA user	The NOMA signal for the NEAR user which Received
19	NOMA-bit	NOMA bit	The bits after symbol detection of the FAR or NEAR ,corresponding on the user's receiver
20	BER-FA	Bit error rate FAR	Bit error rate for FAR signal
21	BER-NE	Bit error rate NEAR	Bit error rate for NEAR signal
22	MUL- ch	Multiply channel	Multiply with channel
23	Add-noise	Add noise	Add noise to the signal MUL_ch
24	DIV-ch	Division channel	Division channel with signal add noise
25	m/d	Multiplication /Division	For testing without noise