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IMPROVEMENT OF NON-LINEAR POWER AMPLIFIER PERFORMANCE USING DOHERTY TECHNIQUE

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Abstract

This paper presents a new method for improving the performances of the non-linear power amplifier using the Doherty concept. The proposed Doherty topology employs class F as basic building block in both the main and the auxiliary amplifiers of the Doherty power amplifier (DPA). The power is distributed between the main and auxiliary amplifiers according to the conditions of Doherty in the manner of uneven power division while keeping the operating point of the class F according to its basic design. The proposed design provides a good flexibility in proper selection of the transmission line characteristics to achieve the specified design goals. The design performance characteristics of the proposed power amplifier are significantly improved. A two-tone signal test showed a clear improvement in the linearity performance compared with the basic amplifier, where two-tone signal at 2.45 GHz with offset frequency of 20MHz is applied using Advance Design System (ADS) simulator environment. The dynamic range obtained is 11dBm and the output power is increased to 32dBm, thereby increasing the efficiency of the PAE in back off power region to 36 %.

Keywords: Doherty power amplifier (DPA), Dynamic range, Power added efficiency (PAE), Uneven power division.

1. Introduction

Most modern wireless communication systems with high data rates require wideband modulated signals with high peak to average power ratio (PAPR) [1]. Wireless systems such as long-term evolution (LTE), Code-Division Multiple Access (CDMA) and other systems with significant time-varying envelope behaviour need power amplifiers (PAs) that have wide frequency range, and to instantaneously achieve efficiency and linearity terms [2-4]. Therefore, this operating condition results in low average efficiency of the power stage. However, non-linear power amplifier which has high efficiency needs complicated architectures to account for the required driving time-varying envelope signals [5-8]. In order to achieve high efficiency, switching mode PAs, such as class-E, class-F, and inverse class-F have been developed [9, 10].

Switching mode power amplifiers achieve high efficiency at the saturation region and low efficiency at power back-off (PBO). This behaviour determines the peak to average power ratio (PAPR) of the transmitted signal. Therefore, the digital pre-distortion (DPD) and many other techniques are employed to overcome this problem [11-13]. High efficiency Doherty power amplifiers are supposed to be employed exceedingly in base stations. Doherty power amplifier (DPA) with its simplified configuration provides output performance in the stipulation of output power, efficiency, and gain as compared to the other structures [5, 11, 14]. However, the capacitance at the output of the transistor constrains the bandwidth of the Doherty power amplifier and this is one of its drawbacks [15, 16]. In addition to the existence of the capacitance issue, DPA suffers from bandwidth limitations due to the quarter wave impedance transformer. Therefore, the efforts have been made to find a new technique to overcome these drawbacks and thereby to improve the performance of the DPA [16, 17]. Harmonic control circuit (HCC) located in front of the matching circuit is used; this can control the impedance for the appropriate saturated operation [9].

Moreover, Doherty amplifiers with a combination of class-F and inverse class-F amplifiers have been developed and can provide higher efficiency at broad power levels. A design for a low power with high linearity DPA for wireless networks has been explored in [8] to provide high efficiency at a wide range of output power. Many other researchers have been improved the DPA performance by improving and developing a new technique and most of these techniques have concentrated in selecting proper biasing condition of the Main and Auxiliary amplifiers. These techniques include asymmetrical Doherty, uneven power division and adaptive gate biasing [3, 5, 11, 14].

This paper presents a design and development of a Doherty power amplifier with uneven power division technique that employs identical class F amplifiers in both Main and Auxiliary stages. The aim is to increase the bandwidth of proposed power amplifier as well as to improve the the linearty, and to reduce the sensitivity of the biasing conditions. Class F PA with a fifth harmonic wave-shaping network is designed to act as a filter to suppress down the third harmonic power and pass maximum output power to the load.

2. Design and Implementation of a New Doherty Amplifier

2.1. Theory

The Doherty power amplifier (DPA) is used in many areas where high efficiency RF power amplifiers are needed for high peak to average power ratio uses [18].

Generally, the Doherty Power Amplifier consists of two amplifiers and impedance-inverting network which convert the current source to voltage source. This converted amplifier is called a Main (carrier) amplifier, while the latter acts as the load modulating device and is called the Auxiliary or (peaking) amplifier [11].

In the traditional Doherty Power Amplifier (DPA), the Main and Auxiliary amplifiers are naturally biased in Class AB and C modes, respectively. The gate bias voltage of the auxiliary amplifier is selected to be below that of the Main amplifier in order to turn on the auxiliary amplifier at back off power (BOP) [11, 19]. The proposed realization of the DPA is achieved using class F power amplifier as basic building block, class F power amplifier is designed to meet CDMA system specification [1]. The key requirement specifications of a CDMA base station amplifier may involve the bandwidth, transmitted power, gain, and gain flatness [4, 18]. Figure 1 shows the schematic diagram of the proposed class-F Doherty amplifier [11, 20].

Z_{01}, Z_{02} and Z_{03} are the characteristic impedances of the transmission lines *TL1*, *TL2*, and *TL3*, respectively. Since the Main and Auxiliary amplifiers are in class F mode then they are sensitive to biasing condition [1, 11]. The key point is to find a proper power division between Main and Auxiliary amplifiers. The operating point of class F is sustained according to its basic design and accomplished in three working levels that include low, medium, and high-power levels by the distribution power between the Main and Auxiliary amplifiers depend on variation of the input impedance of the auxiliary stage. In general, and according to the characteristics of the $\lambda/4$ line, the characteristic impedance of $\lambda/4$ line (Z_0) is equal to $\sqrt{Z_{in} \times Z_{out}}$, where Z_{in} and Z_{out} are the input and output impedance of the $\lambda/4$ transmission line respectively.

Figure 1(b) shows the equivalent circuit of the proposed Doherty amplifier circuit. The output load of the Doherty amplifier is connected to the Main amplifier through the impedance inverter (a quarter-wave loss-less transmission line *(TL1)*) and directly to the auxiliary amplifier. The derivation of the design relationships starts from understanding the operation of the $\lambda/4$ line transformer. The transformation in the loss-less $\lambda/4$ line can be written in terms of node current as well as the input and output impedance as the follows [11, 20]:

$$I_M^2 Z_M = I_{MT}^2 Z_{MT} \tag{1}$$

where I_M and I_{MT} represent the input and output currents of the *TL1*. While Z_M and Z_{MT} represent the input and output impedances of *TL1*, respectively.

Equation (1) can be written in terms of it is terminal voltage. The current of the main amplifier (I_M) is calculated and can be written as:

$$I_M = \frac{V_M}{Z_M} \tag{2}$$

where V_M, Z_M are the output voltage and impedance of main amplifier, respectively.

Then, the transformation of the lossless $\lambda/4$ line in terms of terminal voltage can be obtained by combining Eqs. (1) and (2) gives:

$$V_{MT}^2 Z_M = V_M^2 Z_{MT} \tag{3}$$

where V_{MT} is the output voltage of *TL1* and is equal to V_L that represents the output voltage of the Doherty power amplifier.

The voltage transformation ratio "*m*" may define as:

$$m = \frac{V_M}{V_{MT}} \tag{4}$$

Based on the equation of characteristic of $\lambda/4$ line ($Z_{01} = \sqrt{Z_{MT} \times Z_M}$), then Eq. (3) can be expressed as:

$$m^2 = \frac{\mathrm{V_M^2}}{\mathrm{V_{MT}^2}} = \frac{Z_M}{Z_{MT}} = \frac{Z_{01}^2}{Z_{MT}^2} \tag{5}$$

The current delivered to the load (Z_L) by the main amplifier can be obtained by dividing the output voltage by the characteristic impedance of *TL1* and is given as in Eq. (6).

$$I_{MT} = \frac{V_M}{Z_{01}} \tag{6}$$

The auxiliary input power determines the output current I_a of the auxiliary amplifier according to the current gain. Hence, the load current (I_L) is the sum of the output current of the main and auxiliary amplifier and is given by:

$$I_L = I_{MT} + I_a \tag{7}$$

Also, the output impedance of the main amplifier can be expressed as:

$$Z_{MT} = \frac{\mathrm{V_{MT}}}{\mathrm{I_{MT}}} = \frac{\mathrm{V_L}}{\mathrm{I_{MT}}} \tag{8}$$

Therefore, a significant relationship for the output impedance of the main amplifier is obtained in Eq. (9) below:

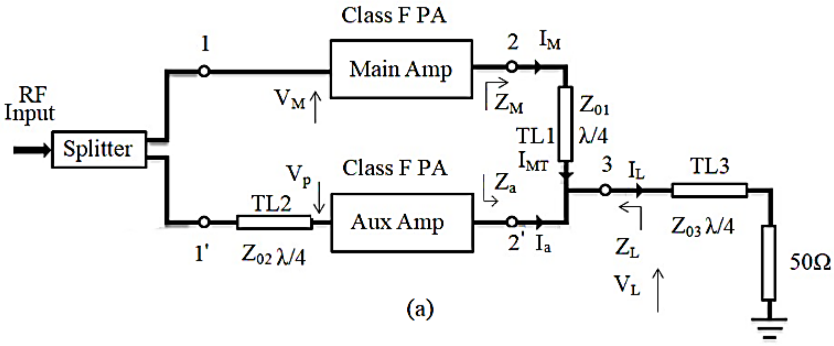
$$Z_{MT} = \frac{V_L}{I_L - I_a} \tag{9}$$

Based on the above equation, it is clear that the output impedance of the main amplifier (Z_{MT}) is controlled by the output current (I_a) of the auxiliary amplifier, and the specified output current (I_a) can be designed and determined by characteristic impedance of $\lambda/4$ line (Z_{02}). Therefore, the output impedance of main amplifier (Z_{MT}) will be depended on Z_{01} and Z_{02}. The main function of the characteristic impedance Z_{03} of *TL3* shown in Fig. 1 is to provide suitable matching between the output impedance of the Doherty power amplifier and the load impedance (50 Ω). Then, it is obvious that the optimum power distribution and maximum efficiency can be obtained by controlling the characteristic impedance of transmission lines *TL1, TL2* and *TL3*.

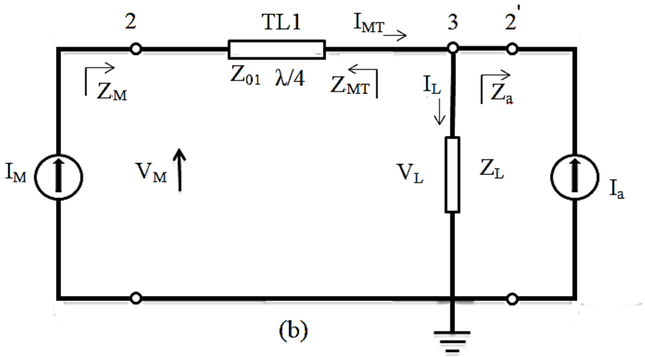
3. Realization of The Proposed Doherty Power Amplifier

The proposed DPA is realized to improve the performance of class-F non-linear power amplifier by making use of the concept of the Doherty technique. The realization of the proposed Doherty power amplifier is started by the design of class-F amplifier by selecting specific transistor that operates properly in the CDMA applications at 2.45 GHz [1]. The transistor type is selected from the available ADS library that has the specifications of Statz_Model (Statz Raytheon GaAs FET Model). The dc biasing conditions are determined using ADS to find the optimum operating point. The performance of class-F amplifier is obtained by wave-shaping network and the biasing of the class-F power amplifier circuit [1].

To satisfy the class-F operation of CDMA systems with high peak to average power ratio, the Doherty amplifier is used [6, 12].



(a) Proposed power amplifier.



(b) Equivalent circuit.

Fig. 1. The Doherty power amplifier.

The symmetric amplifier method with uneven power division is used for both the main and auxiliary amplifiers of the proposed DPA. A class F mode is applied as shown in Fig. 2(a) to avoid the sensitivity limitation of the amplifier, the uneven power division method and the bias point are used as fixed in both main and auxiliary stages in order to give the proper and ideal power distribution between main and auxiliary amplifiers [5, 11], and also to obtain maximum output power and efficiency for both amplifiers. The tuning facilities available in Advanced Design System (ADS) simulator environment provide an ability to change the variables of the characteristic impedance of the transmission lines 1, 2, and 3 presented in Fig. 2(b) of the DPA in order to obtain the convenient performance that satisfies the following three main goals:

- Suitable power division between the Main and Secondary amplifier (Auxiliary).
- The output impedance of the DPA amplifier Z_L must be determined and optimized.
- Obtain a proper and ideal matching between output impedance Z_L and the standard 50 Ω load.

To meet the specified parameters listed in Table 1, an appropriate selection is performed by tuning for design variables Z_{01}, Z_{02} and Z_{03} that determine the power distribution between the main and auxiliary amplifiers.

Table 1. The required specifications values of the proposed design.

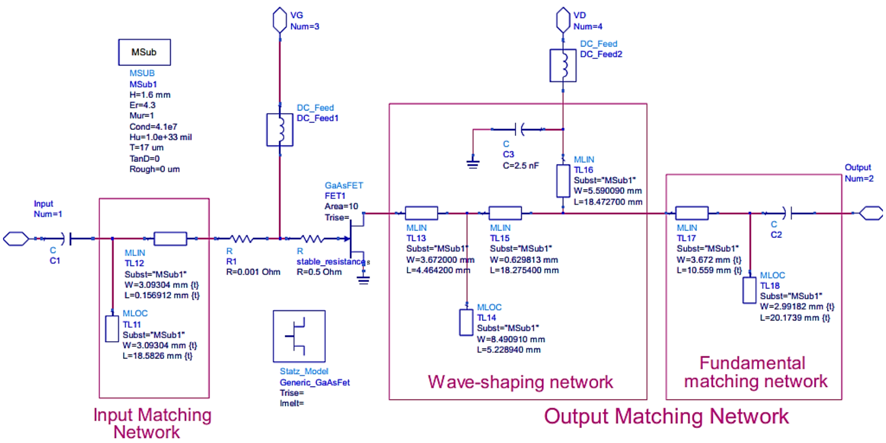
Specifications	Required values	Obtained values
Input Power(dBm)	≤20	19
PAE at Max Power	>50%	61.8%
Gain (dB)	≥ 13	13
PAE at (PBO)	> 20%	36%
BW(MHz)	> 5	20

The resultant optimum values that satisfy the required specification are listed in Table 2.

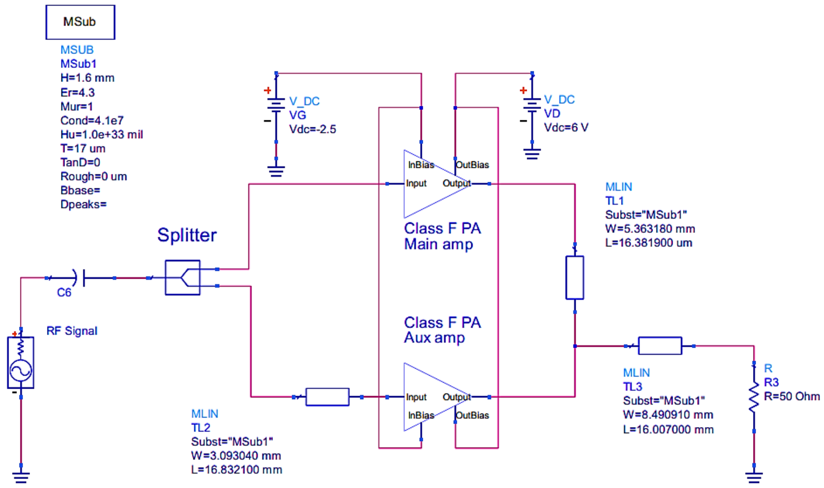
Table 2. Optimum values of characteristic impedances.

Impedance	Optimum value
$Z_{01}(\Omega)$	35
$Z_{02}(\Omega)$	50
$Z_{03}(\Omega)$	25

The schematic diagram of the proposed Doherty power amplifier that is shown in Fig. 1(a) is illustrated in Fig. 2(b) with the associated class-F power amplifier stage in Fig. 2(a).



(a) The Class-F PA amplifier realization.



(b) The proposed Doherty power amplifier realization.

Fig. 2. The schematic diagram realization of the class-F and proposed Doherty power amplifier.

4. Simulation Results

The proposed DPA is designed, tuned, and simulated using ADS simulator software for the application in base-station requests such as CDMA and 3G system. The signal with instantaneous bandwidth test has been implemented to determine the effects of the harmonics created as the proposed power amplifier is operating in the saturation (maximum power) region. The test signal has been fixed at frequency 2.45GHz with 20 MHz bandwidth. The results are considered and studied up to the 5th harmonic. Figure 3 shows the simulated DC component of the drain current versus the input power for both that main and peaking amplifier.

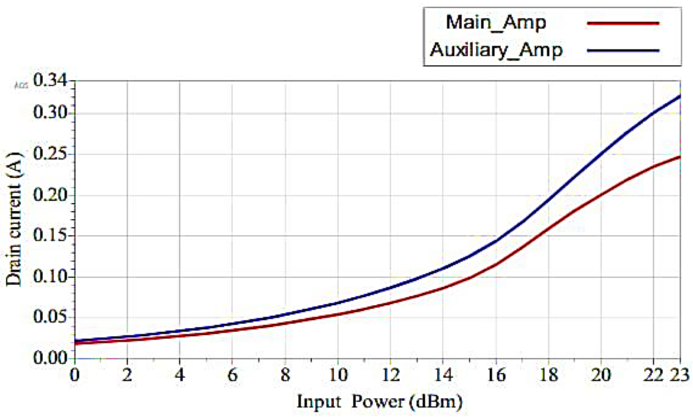


Fig. 3. Drain current versus the input power of the main and auxiliary amplifier.

The sizes of the two devices of the main and the auxiliary amplifier are designed to be equal dimension, thus a trade-off between the load modulation and drain currents is achieved to optimize the Doherty performance using tuning option that available in the ADS simulator. Hence an uneven power divider mandatory is used to assure the peaking amplifier reaches its maximum output current [11]. The output power and drain efficiency characteristics versus input power swept from 0 dBm to 24 dBm at 2.45 GHz for the designed DPA is depicted in Fig. 4.

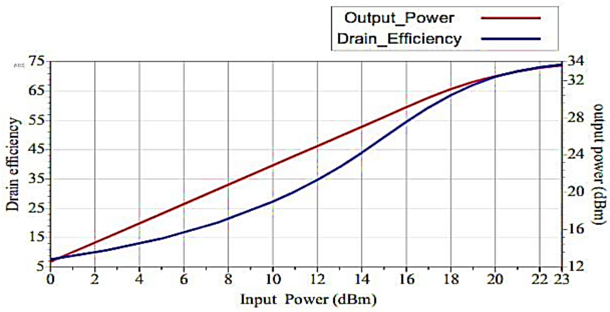


Fig. 4. Drain efficiency and output power versus input drive power for the overall DPA at *Vgs*= -2.5 V, *Vds*= 6 V and *F* = 2.45 GHz.

It can be seen from Fig. 4 that saturated DPA provides a drain efficiency of 70% at maximum output power of 32 dBm.

The deviations of the power gain and PAE compared to the load power is illustrated in Fig. 5. It is clear from Fig. 5 that the transducer power gain is constant between 12.5 and 13 for a wide range of input power which leads to make dynamic range (DR) wider for output power range extending from 19 dBm to 30 dBm.

It is obvious from single tone test that the 3rd harmonic relation shown in Fig. 6 is increased with increasing input signal. The overall variance between the 1st harmonic and the 3rd counterpart is around 60 dBm or more which provides properly a suitable output spectrum [21].

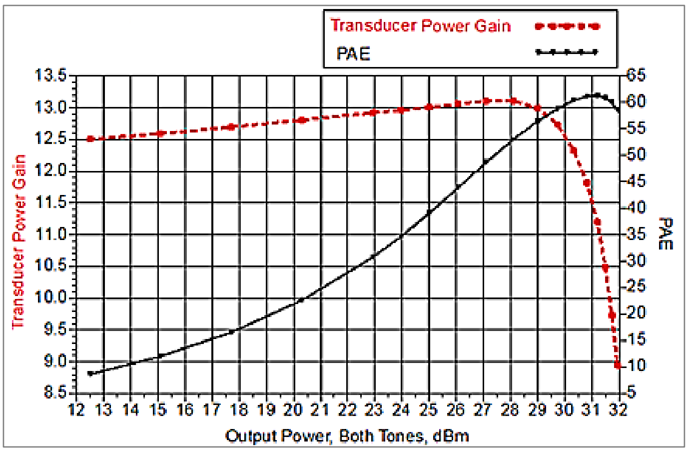


Fig. 5. PAE and gain as a function of output power.

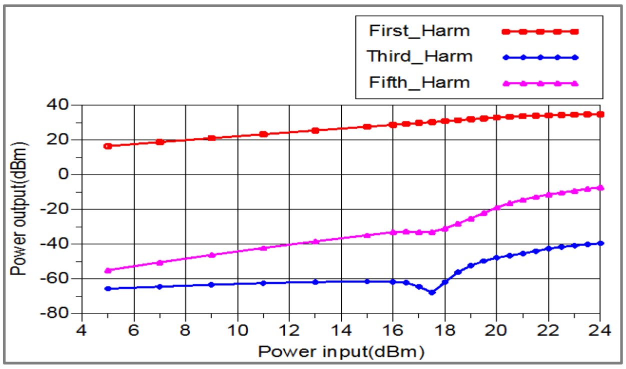


Fig. 6. Power harmonic with input power.

A two-tone signal is used to simulate the Inter-Modulation Distortion (IMD) and the output spectrum in order to analyse and validate the linearity obtained from the proposed power amplifier as depicted in Figs. 7 and 8. The intermodulation distortion of 3rd order (IMD3) and the intermodulation distortion of 5th order (IMD5) are illustrated in Fig. 7. It can be seen from this figure that the power ratio of the third order (IMD3) with respect to carrier signal at different values of the input power has reached to -16 dBc, while the value of the fifth order (IMD5) is less than -30 dBc at the maximum output power. Moreover, the simulation of the output signal spectrum of the designed DPA is shown in Fig. 8. It is clear from this figure that the nearest harmonic component is declined to a value less than 35 dBm from the fundamental component. The resultant values of the intermodulation distortion and the value of the output spectrum are obtained to be with the required range of the modern communication systems such as CDMA system [22-24].

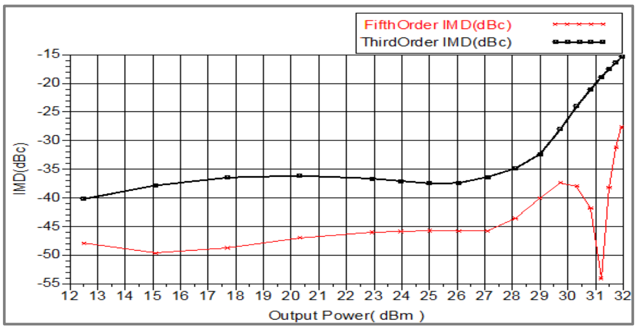


Fig. 7. Inter modulation distortion.

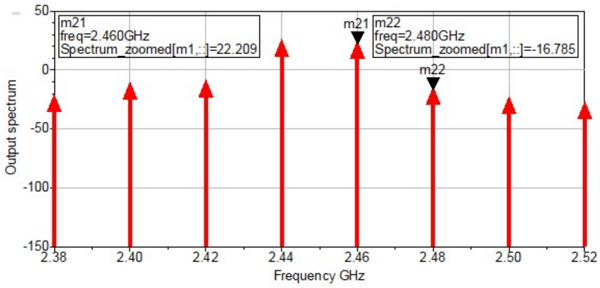


Fig. 8. Spectrum of the output signal.

The output response of the proposed amplifier with respect to the time-varying envelope behaviour signal is also measured to show the improvement of the linearity of this amplifier as shown in Fig. 9. This is performed by applying signal with peak to average power ratio (PAPR) equal to 6.4 dBc, and bandwidth of 20 MHz at 2.45 GHz. The measured value of the adjacent channel ratio (ACPR) is -35 dBc as shown in Fig. 9. Therefore, the Doherty power amplifier (DPA) shows a significant improvement in performance of the amplifier [21].

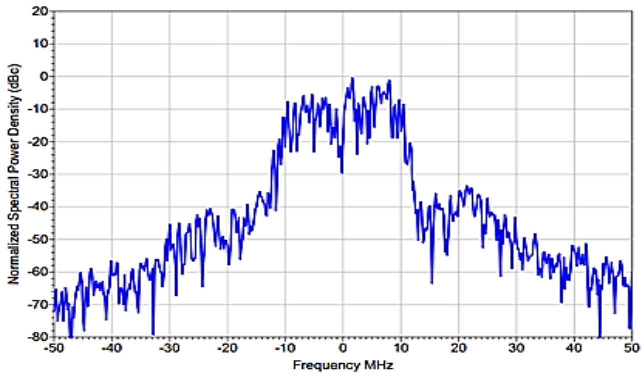


Fig. 9. Output response of the DPA.

The simulation results from the ADS simulator for proposed DPA are compared with that of the basic class-F power amplifier given in reference [1] and are listed in Table 3.

It can be seen from this table that a significant improvement in performance is obtained; these performances may include increase in efficiency, linearity, increased dynamic range, and increased transmitter bandwidth.

Table 3. Comparison between the results of the proposed amplifier and that of the class-F basic PA [1].

Specifications	[1]	Present work
***Pin* max (dBm)**	13	19
***Pout* max (dBm)**	26	32
Gain (dB)	13	13
PAE (%) at maximum output power (*Pout*)	62	61.8
PAE (%) at 6 dB back-off	33	36
IMD3 at maximum output power (dBc)	-21	-16
IMD5 at 6 dB back-off (dBc)	-38	-35
Offset frequency between two tones (MHz)	0.5	20
Dynamic range(dBm)	8	11

In addition, another comparison is done between previous research [12, 14, 24] that are based on asymmetrical DPA with selecting biasing condition and this work for uneven power division. Table 4 presents comparison between these methods for different performance parameters. It can be found that the DPA with uneven power division can operate in CDMA base stations or 3G mobile systems like long-term evolution (LTE)-advanced system at output power level more than 19 dBm and up to 32 dBm.

Table 4. Comparison between this work and other techniques [12, 14, 24].

Specifications	[24]	[14]	[12]	Present work
PA Mode	Class EF	Class F	Class F^{-1}	Class F
***Pout* (dBm)**	39.2	40	42	32
Gain (dB)	12	10	12	13
PAE (%) at maximum output power	68.5	56	63	61.8
PAE (%) at 6 dB back-off	30	35	49	36
Offset frequency between two tones	-	40 MHz	10MHz	20MHz
Dynamic range(dBm)	12	7	8.6	11
Frequency (GHz)	2.4	3.5	2.4	2.45
Techniques	Adaptive gate biasing	Adaptive gate biasing	supply modulator	Uneven power division

5. Conclusions

A new Doherty power amplifier has been designed, realized, and simulated. A proper uneven power distribution with an identical amplifier in both main and auxiliary has been employed by using the tuning facility available in ADS environment. The proper uneven power distribution has provided clear flexibility in power distribution between main and auxiliary blocks. The identical amplifier characteristic overcomes the problem associated with a class F power amplifier that is the sensitivity problem resulted from different bias point conditions. This new proposed combination has made use of the class-F and Doherty concept by manipulating the power distribution between main and auxiliary stages, and also the proper selection of bias conditions. This realization combined the advantages of both class-F and Doherty structures. A significant improvement has been obtained in the nonlinear power amplifier performances. These improvements include increasing of about 23% of the maximum output power and 9% increase of the power added efficiency (PAE) at 6 dB power back-off. The bandwidth of the proposed power amplifier has been expanded to be almost 19.5 MHz as well as increasing in the dynamic range (37%). A good linearity of the proposed Doherty amplifier has been also recorded to be -35 dBc based on the measuring ACPR.

Nomenclatures

P_{in}	Power input
P_{out}	Power output
T_L	Transmission lines
Z_0	The characteristic impedance
Z_{in}, Z_{out}	The input and output impedance
λ	Wavelength

Abbreviations

ADS	Advance Design System
ACPR	Adjacent Channel Ratio
BW	Band Width
BOP	Back Off Power

CDMA	Code-Division Multiple Access
DR	Dynamic Range
DPA	Doherty Power Amplifier
DPD	Digital-predistortion
IMD	Inter Modulation Distortion
LTE	Long-Term Evolution
PA	Power Amplifier
PAE	Power Added Efficiency
PBO	Power Back-Off
PAPR	Peak to Average Power Ratio
3G	Third Generation

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