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DESIGN A PROTOTYPE FPGA MODEL FOR TARGET DETECTION BY RADARS PASSIVE BASED ON SYNTHETIC-APERTURE RADAR ALGORITHM

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Abstract

There are many challenges that make it difficult to distinguish the targets along with the harsh environments that increase these difficulties and complexity of detection by the radar system. Several methods used in this field to overcome these difficulties, Synthetic-Aperture Radar (SAR) has been used in bi-static passive radar detection because it is ability to eliminate the effect of uncooperative transmitter and clutter so that it is making target detection easy even in harsh environments. This paper focuses on design system of passive radar based on matching and optimal matching filter applied in FPGA (Field Programmable Gates Array) with implementation of SAR algorithm. The RF radio using by radar as opportunity of transmitter and a specific of nine-channels radar arranged in shape of circular array to collect that affected signals. Actually experimental radar data used for testing system, MATLAB using for simulated data processing of SAR algorithm and model hardware using Xilinx FPGA Spartan-3 XC3S200 for implementation of proposed system in order to take advantage of the FPGA technique in terms of data processing speed and improve system performance by reducing processing time and minimizing the size of the desired circuit. Matching and optimal matching filter used in the circuit design of the system, the results show that clutter of zero Doppler better filtered out by using optimal matching filter, which is register value of (1×10^{-4}) bit error rate at 10 db. Power and timing analysis of hardware execution vindicate that FPGA provides dependable and fast processing program for real time SAR algorithm. Optimal matching filter registered more reduction in most utilization resources items compared with matching filter also the optimal filter recorded maximum frequency for data processing about 253.036 MHz by using FPGA and less power consumed about 3.682 W.

Keywords: FPGA; Matching and optimal matching filter; MATLAB; SAR algorithm; X- power analyser and timing analysis.

1. Introduction

Passive radars have conventional operative relate during the ancient few years among various action entities for surveillance and protection applications. These radars utilize signals of possibility from a spreading variety of communicating or show emissions similar Satellite, WLAN/Wi-Fi, WiMAX , DVB _ T , DAB , TV, FM, GSM, etc. [1, 2]. They offering a symbol of advantages over customary active radar scheme such as low operative cost, decrease power requirements, anti-stealth and covertness. The system of radar contains from two antennas along with two channels. Colone et al. [3] explained that the first antenna named as reference antenna thrilling the reference (direct) signal, which sending from transmitter while the second one received the signal, which is reflected from target.

These above two signals both processing to detect the target using matching filter such as processing of cross opacity. More complexity multi-frequency and digital multi-channel receiver system improved using a range of antennas. According to Le et al. [4] and Wong et al. [5], this one of advanced system provides additional potentiality such as digital beam shaping and progress filtering adaptive to detect the target and reject the clutter. Nominee of adaptive algorithm for this type of processing radar is Synthetic-aperture radar (SAR), it is especially salutary for slow and weak motion of terrestrial targets detecting, which is in environments clutter airborne. Most research has been done on SAR for energetic radars using circular array and uniform linear array while part of the research occur on the clutter inhibition of radar airborne.

In same manner, several algorithms of adaptive filter used for PBR cancellation of clutter, performance detection of SAR radar be maximize by find out a method for suitable code design [6, 7]. Colone et al. [3] and Le et al. [4] mentioned that one such algorithm and system uses a system receiver from two antenna to captivate solicitude signals. There is no research noteworthy obtainable focuses on implementation of FPGA with SAR algorithm regarding case of Passive radar compared with array circular uniform using for track and detect efficacious target.

This paper represents design and implementation FPGA model as per SAR algorithm for detection target in case of passive radar using a array in circular uniform to captivate the interest signals. The array antenna be composed of nine elements with regular spacing in radial uniform. The geometry of array in circular uniform spread because its capability to guide the beam in azimuth direction around 360° without any mechanical motion [8-10].

The practical experiment was carried out where the target represents by a vehicle movement. SAR algorithm in passive radar implementation is the main purpose assert on this paper, Section 2 explained steps pre-processing and scenario reception data containing model system. Section 3 described processing FPGA-GPU with data transfer results, the design and implementation model of FPGA based on SAR algorithm explained in Section 4, Section 5 explained the results and discussion while Section 6 dealing with remarks conclusion.

2. Scenario Reception Data

The setup experimental be composed of array antenna nine elements in circular uniform ,FM transmitter and the target represents by a mobile vehicle as shown in Fig. 1. This is applied to register nine signals in real time processing that are

separately clash on each element antenna in circular uniform. The explanation of the setup system shown in Fig. 2 represent block diagram of processing signal. The data FM real time of nine channels errors amplitude and phase standardization all prepare in a stage of pre-processing. It can be avoided rebounding echo from a target by forming beam digital adaptive and estimation in arrival of direction subjected data array, which are calibrated to get reference pure signal from the transmitter. The reference pure signal and the data nine-channel consist of targets echoes is then utilized for processing of SAR algorithm [11].

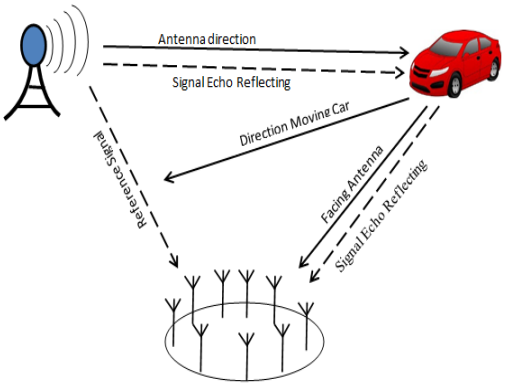


Fig. 1. Scenario of reception data.

SAR processing

The inputs of SAR processing contain from data nine channels signals and reference pure signal, the algorithm applied has main improvement represented by geometry array circular uniform that fixed by multi-elements in order to obtain more coverage and flexibility. Reference pure signal of version delayed time combine with signal data come from nine channels by using model mixing that is explained in Fig. 2. Equations (1) and (2) explain vector steering temporal $z(u_x)$ and vector steering spatial $y(u_w)$ respectively for specific array circular uniform [8, 12].

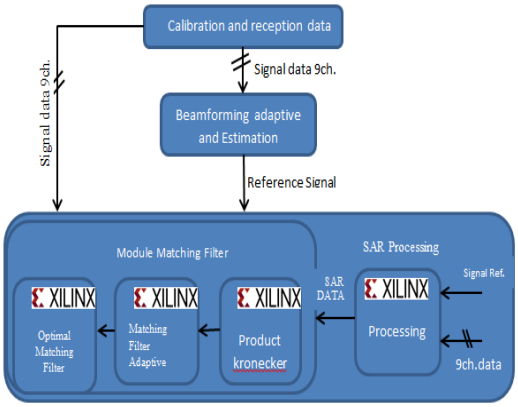


Fig. 2. Block diagram processing signal for a passive radar based on array circular uniform.

$$z(u_x)=[e^{(j\propto kcos(\emptyset_1-\emptyset))},\ldots\ldots,e^{(j\propto kcos(\emptyset_R-\emptyset))}]^N \quad (1)$$

$$y(u_w)=[1,e^{j2\pi u_w},\ldots\ldots,e^{j2\pi u_w(P-1)}]^N \quad (2)$$

where $\propto=\frac{2\pi}{\gamma}$ and γ is the length of the wave, k the array radius, each element positioned on array in angular form is $\emptyset_r=\frac{2\pi r}{R}$ where R is the elements antenna number and $\emptyset$ is the angle scanning or angle incidence. The frequency spatial is $u_x=\propto k\cos(\emptyset_r-\emptyset)$ and $u_w=\frac{h_w X}{h_x}$, which is decrease Doppler frequency, where h_w is target Doppler frequency, X and h_x means factor sub-sampling and frequency sampling respectively [3, 5]. Vector steering mutual temporal-spatial $U(u_x,u_w)$ can be expressed by the following equation:

$$U(u_x,u_w)=z(u_x)\otimes y(u_w) \quad (3)$$

where $\otimes$ sign is the correlation sign , the vector steering mutual temporal- spatio size relies on samples temporal *P* and elements antenna number *R* that are utilized in array circular uniform. Vector steering temporal- spatial or vector scanning $U(u_x,u_w)$ used to scan data of nine channels mentioned by s(*f*). For r range specific sometimes, the reference signal of version-delayed time is mixed with data that received from all channels [5, 13]. The product mixed $S_p(f;r)$ can be represented by:

$$S_P(f;r)=s(f)\circ(1\otimes X_{ref}(f-r))^* \quad (4)$$

where $X_{ref}(f-r)$ is purely reference signal with version delayed time and $\circ$ sign is product sign, sub-sampled result of product mixing using to get signal sub-sampled ordered $S_x(r)$ is given by:

$$S_x(r)=[S_P^N(0;r),S_P^N(S;r),\ldots\ldots,S_P^N\big((P-1)S;r\big)]^N \quad (5)$$

where *N* superscript matrix of transpose and r is block length depending on number of subcarrier. Targets Doppler angel details and major clutter of transmitter can be obtained from data collection device while signal sub-sampled in Eqs. (3) and (5) for vector steering temporal-spatial using to calculate $bp(u_x,u_w,r)$ output of matched filtered [7].

$$bp(u_x,u_w,r)=U^{\dagger}(u_x,u_w)S_X(r) \quad (6)$$

where $\dagger$ is operation transpose hermitian, the processing SAR final step is optimal matching filter, which is using to obtain signature of the target by contributions clutter filter out that containing signature of transmitter at frequency of zero Doppler.

Matrix of covariance noise (*K*) and interference calculation required for this processing. Matrix covariance model using for simulation beside that is find a lot exist approaches methods for determination matrix covariance with more accuracy, the calculation output of optimal matching filter as below:

$$b(u_x,u_w;r)=d^{\dagger}(u_x,u_w)S_x(r) \quad (7)$$

where $S_x(r)$ is the signal sub-sampled recorded and *d* is the vector weight optimal filter represent by:

$$d(u_x,u_w)=K^{-1}U(u_x,u_w) \quad (8)$$

where *K* is the matrix covariance interference estimation, practically it needed huge number samples of data training for K estimation and also current data is difficult

estimation for passive radar case so that in this scenario used matrix covariance interference model.

Detection target by reception data of SAR processing bounded by main steps as follows [14]:

- Foremost, pre-processing the signal data of nine channels that is obtained from array antenna so that correction amplitude and phase applied and effects coupling mutual removed.
- Beam forming adaptive technique using for the received data array antenna in order to extract perspicuous reference signal.
- Equation (4) used for mixing product, which is used mixed perspicuous reference signal with signal data of nine channels.
- Equation (3) represent vector scanning is known also vector steering temporal-spatial determined by using both Eqs. (1) and (2), which are represent vectors steering temporal $z(u_x)$ and vectors steering spatial $y(u_w)$ respectively.
- Equations (3) and (5) of matched filter is achieved to get interferences and targets information Doppler angle by utilize Eq. (6).
- Equation (8) represent weight vector of optimal matching filter, which quell the interferer direct track of zero-Doppler and can be obtained by calculating interference matrix covariance.
- Eventually, optimal matched Filter using the applied weight vector to obtain signature target perspicuous as represent in Eq. (7).

3. FPGA-GPU Processing

The components RF for the receiver do not react to linear amplitude and phase response on the operating bandwidth, which cause synthetic corruption in the profile of the field so that using an extra channel (nine instead of eight channel) to solve these problem by using architecture time-interleaved employing. Actually memory CPU have extra one buffer because sometimes happen that the data rate be doubles so that using one extra buffer in CPU that allows data access quickly on the row physical common of RAM memory beside each device buffer memory allocate requires flow standard between GPU (Graphics Processing Unit) and FPGA data exchange. Outside working FPGA framework slightly reduced rate transferred data per second because the extra interruption and memory operations lead to increase the time necessary to complete transferred data.

In fact find two ways for accomplished data transfer from GPU to FPGA, the first one transfer combination AMD (Access Memory Direct) for FPGA used to transfer memory host from FPGA and then GPU received from host by function CUDA employing cpu memory per lane R to F. various sizes of data transfer are registered in two cases of data rates measured ,important notice that GPU has multi lane ,this is clear for achievable cpu memory per lane F to R. Global throughput is limiting because each AMD transfer requires extra packet in achievable performance difference reading and writing.

The transfer GPU or AMD system utilizing instead of memory approach because the both targets (memory host or GPU) received data from one of the

above. Figures 3 and 4 explain rate transfer data of CPU and FPGA, it can be observed that CPU memory per lane R to F has a maximum data rate registered 264 M bytes/second at size transfer 1M byte while the others AMD of FPGA reach maximum value 215 M bytes/second at same size transfer, the reason for that is back to the response time reading request by GPU. All values sweep and points test are specified by using optimal matching filter, which contains object results in simulation rate error for error symbol test point registered as shown in Fig. 5.

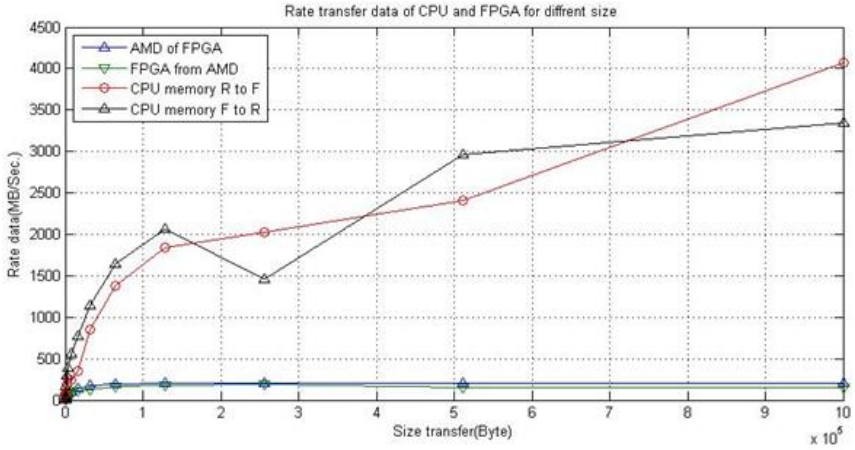


Fig. 3. Rates transfer data CPU and FPGA for different size.

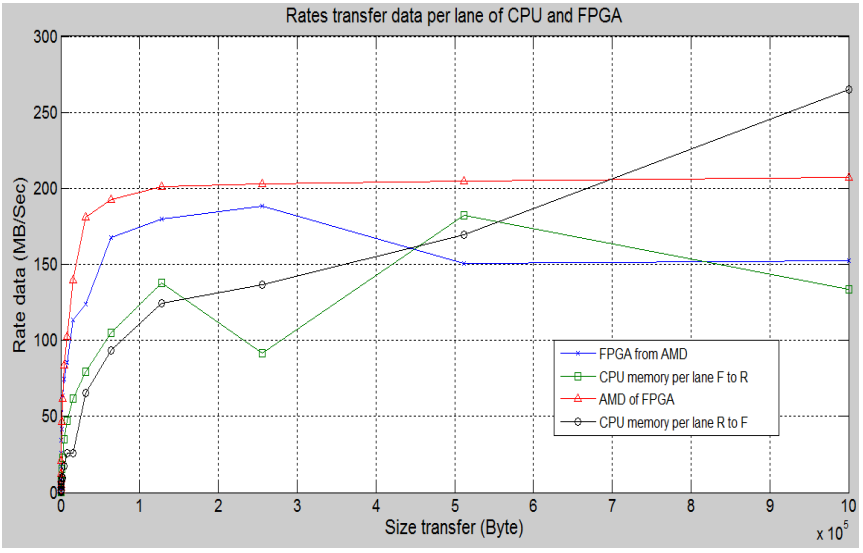


Fig. 4. Rates transfer data per lane of CPU and FPGA.

Based on studies by Lin and Ling [15], actually 802.11b object (is a solid objects that affected by RF coverageas per IEEE 802.11 Standards), which using semi logy methods or get data plot to obtain plots point test and data results. After tested object 802.11b, the results included zero Doppler, which represented by parameter1 test (plot curves parametric number and matrix data columns for control

parameter) while 'EsNo' represent parameter2 test (plot x-axis and matrix data rows of control parameter), that is explained clearly in Fig. 5 where the range frequency (0-200) Hz for Doppler values are shifted in order to plot bit error rate against 'EsNo'. Zero Doppler registered minimum value at 10 dB is ($1x10^{-4}$) bit error rate, which is less than another type Doppler ($3e^{+002}$) by 10^{-2} bit error rate by means that the target signature filtered out, these results taken when applied optimal matching filter in proposed system.

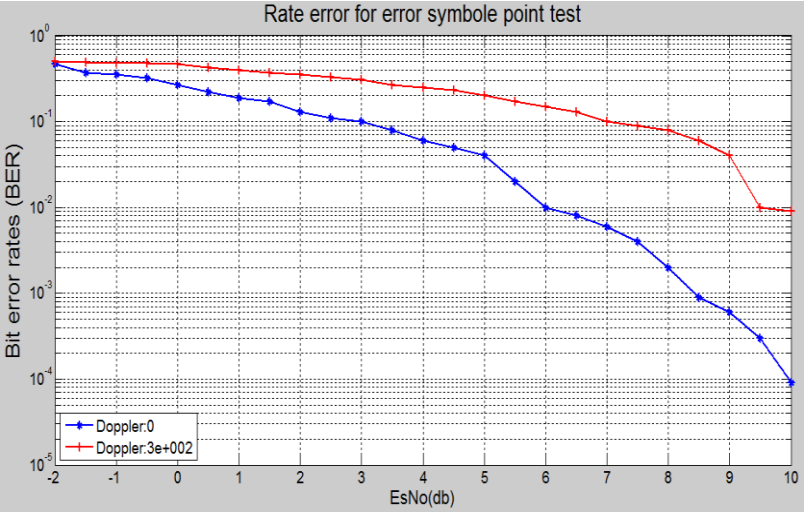


Fig. 5. Bit error rates comparison between two Doppler types.

Stages processing data

The scenario reception data include non-cooperative transmitter FM setup at 893 MHz and away from circular array antenna by 570 meter. The target vehicle moving to the direction of array by about 90° and speed of 130 km/h. After the signal of nine channels received, MATLAB with FPGA used to perform data post-processing and that is results perspicuous reference signal breaking up from the signal data of nine channels obtained. Then SAR processor fed by data of nine channels and reference signals. The output of matched filter using Eq. (6) for transmitter confirms at -35° with zero- Doppler frequency and signature target moving so slowly at 90° with Doppler 45 Hz. The optimal matching filter used Eq. (7) in order to remove zero-Doppler frequency constituents and split vigorous target signature.

4. FPGA implementation

The research section challenging achieved in the implementation of FPGA with SAR algorithm on passive radar using array circular uniform in order to improve the system of radar in terms of high speed and heavy weight so that a valid SAR algorithm can be performed. FPGA Spartan-3 Xilinx XC3S200 used for the design SAR steps data processing as shown in Fig. 6.

The model designed to contain buffers bin-Doppler and phase angle utilized for scan-collected data in order to find Doppler and angle target posture. Several control blocks were utilized to manage input data in order to execute specific SAR

processor tasks. Block generator address was used to designate input data addresses when reach at the input blocks of RAM dual-port. All operations of multiplication required matrix of complex multipliers because of the data collected is complex. In addition, block adder used for operations of multiplication in order to add all data rows and the result value store at assign addressable RAM.

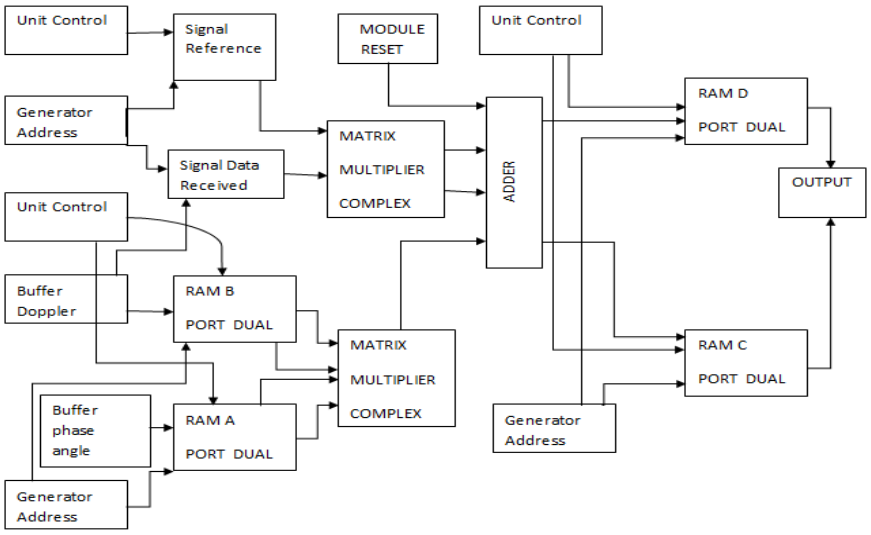


Fig. 6. FPGA designed for block set SAR processing.

The block set shown in Fig. 7 explain FPGA performed model designed based on SAR processing algorithm. The block set of scanning matrix produce scanning temporal and spatial vectors to recognize predestined target location. The block set signal of real data produces the signal of target blend processing module while the weights required by optimal matching filter loads directly from block set matrix weight. Basic block set processing matched filter designed, which is explained in Fig. 8, both block sets optimal matching filter and matched filter were used the same model. The block sets matched filter reused for prototype of optimal matching when FPGA clock and inputs changing.

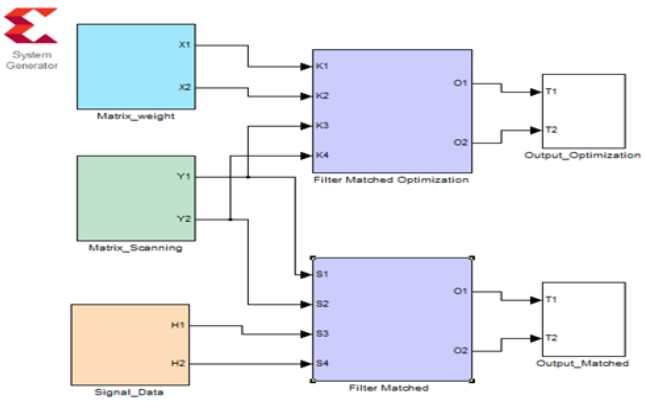


Fig. 7. Implementation of FPGA with SAR processing.

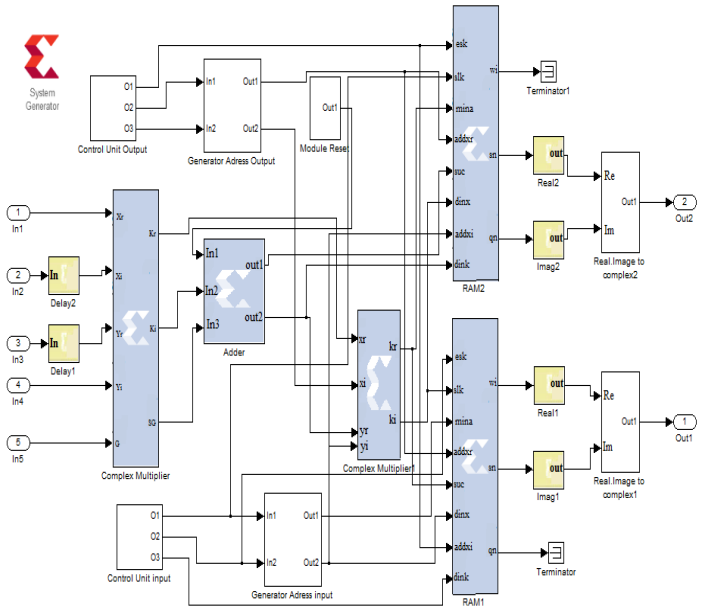


Fig. 8. Processing matched filter by using FPGA.

Figure 9 shows a model co-simulation hardware, System Xilinx Generator that using by FPGA directly processing of SAR. The target plot by the Doppler angle that display in computer by back transfers results, filter matched and optimal matching filter used for separate and manipulates data of the target, which are the computer, received, the processing results of MATLAB agreement with results obtained by Xilinx FPGA.

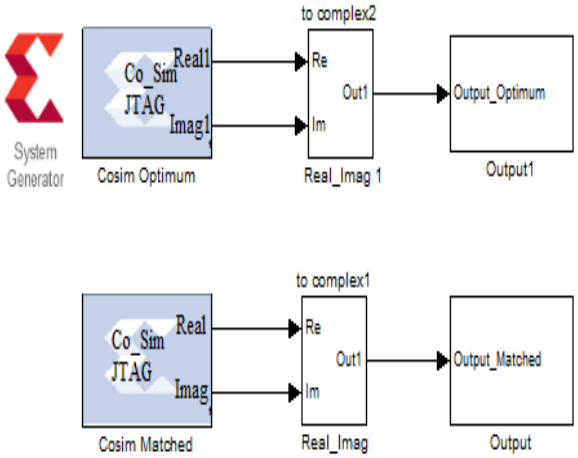


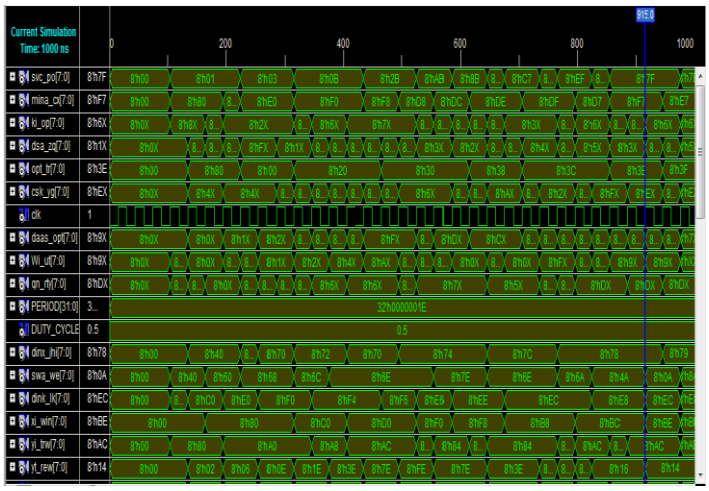
Fig. 9. Model co-simulation hardware implementation on FPGA.

5. Results and discussion

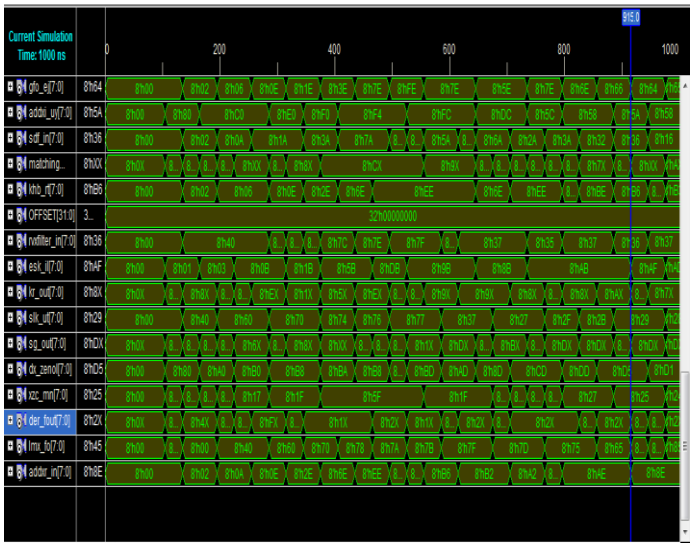
The results of all the circuits that including processing of matched filter in FPGA, FPGA design, simulation and implementation with SAR processing are describe below:

Analysis power and timing hardware

The implementation of FPGA represent the next stage to find out requirements of Power and arithmetical operations, Tables 1 and 2 represent the results of summary utilization resources for both filters matching and optimal matching respectively, Figure 10 explains the simulation waveform of proposed system model that shown in Fig. 8 when applied as optimal matching filter using Xilinx ISE 9.2i program.



(a) Simulation waveform part 1.



(b) Simulation waveform part 2.

Fig. 10. Simulation waveform for the proposed system.

Table 1. Matched filter summary utilization resources results that implementation in FPGA.

Logic utilization	Used	Available	Utilization (%)
Number of slice flip flops	2,031	309,467	0.65
Number of slice LUTs	1,617	151,310	1.07
Number of occupied slices	110	6,211	1.77
Number of slices only related logic	5,970	7,110	84
Number of slices unrelated logic	17	7,110	0.24
Total number memory RAM's	79	427	18.5
DSP48E1's	37	873	4.24
Number used as logic	4,612	31,700	14.54
Number of LUT flip flop used	121	410	29.5
Number with unused flip flop	1,715	19,765	8.7
IO's ports	197	710	27.7
Average fan out of non-clock nets	6.3	365	1.7

Table 2. Optimal matching filter summary utilization resources results that implementation in FPGA.

Logic utilization	Used	Available	Utilization(%)
Number of slice flip flops	1,374	309,467	0.44
Number of slice LUTs	2,954	151,310	1.9
Number of occupied slices	94	6,211	1.5
Number of slices only related logic	3,724	7,110	52.3
Number of slices unrelated logic	11	7,110	0.15
Total number memory RAM's	67	427	15.7
DSP48E1's	19	873	2.17
Number used as logic	3,573	31,700	11.27
Number of LUT flip flop used	139	410	33.9
Number with unused flip flop	1,367	19,765	6.9
IO's ports	172	710	24.2
Average fan out of non-clock nets	9.7	365	2.7

It can be observed from both Tables 1 and 2 that most items resources quantities, which are using by the prototype model of matching filter are more than that using by optimal matching filter as shown in Fig. 11.

Table 3 shows the comparison of chip component's power consumed between two filters these results obtained by using X-power analyser. The results show that the power consumed in the chip resources of a matched filter processing is higher than the power consumed by the optimal matching filter because it used less sources than matching one as shown in Fig. 12.

Table 4 shows analysis frequency and timing processing, which is, shows the very high difference in timing processing between FPGA and MATLAB. It can be observed also that the period clock of FPGA has less time required for processing of optimal matching filter because most of the resources parameters quantities that using in optimal one are less than that using in matching filter.

Table 5 shows and represent the comparison between this work and other related work, the comparison included quantities of components that using in hardware system. Also Table 5 explains that the FPGA parameters such as the number of slice registers, LUTs, RAM's blocks and DSP48El's blocks components of this work are less than that using in other work [16]. This is due to the efficient algorithm technique that used in this research.

Table 3. Comparison of power obtained by x-power analyser.

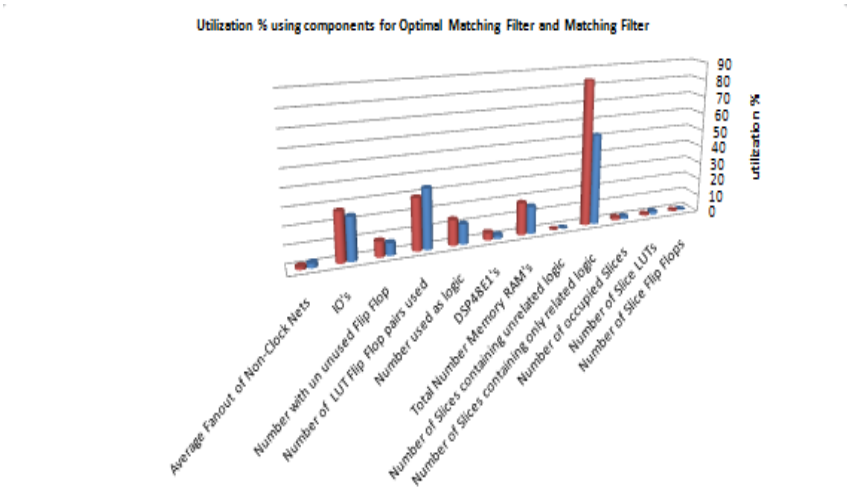
Components on chip	Power consumed by matching filter (Watt)	Power consumed by optimal matching filter (Watt)
Slice flip flops	0.070	0.043
Slice LUTs	0.015	0.009
RAM's BLOCKS	0.113	0.062
IO's pads	0.451	0.374
DSP48E1's BLOCKS	0.026	0.0085
Leakage power	3.412	3.1855
Total power	4.087	3.682

Table 4. Analysis results of frequency and time duty.

Item	Maximum frequency of FPGA (MHz)	Processing of FPGA (nanosecond)	Processing of MATLAB (second)
Optimal matching filter	253.036	3.952	7.4
Matched filter	112.701	8.873	9.1

Table 5. Comparison of FPGA parameters with other work.

Parameters		Orduyilmaz et al. [16]	This work
Number of slice register	Used	31,580	3,724
	Available	44,800	7,110
	Utilization (%)	70	52.3
Number of slice LUTs	Used	29,120	27,954
	Available	44,800	151,310
	Utilization (%)	65	18.5
Number of RAM/FIFO BLOCKS	Used	48	67
	Available	148	427
	Utilization (%)	32	15.7
Number of DSP48E1's BLOCKS	Used	108	19
	Available	128	873
	Utilization (%)	84	2.18
FPGA frequency		70 MHz	253.036 MHz
FPGA processing time		14.3 nanoseconds	3.952 nanoseconds



	Average Fanout of Non-Clock Nets	IO's	Number with un unused Flip Flop	Number of LUT Flip Flop pairs used	Number used as logic	DSP48E1's	Total Number Memory RAM's	Number of Slices containing unrelated logic	Number of Slices containing only related logic	Number of occupied Slices	Number of Slice LUTs	Number of Slice Flip Flops
Optimal Matching Filter	2.7	24.2	6.9	33.9	11.27	2.17	15.7	0.15	52.3	1.5	1.9	0.44
Matching Filter	1.7	27.7	8.7	29.5	14.54	4.24	18.5	0.24	84	1.77	1.07	0.65

Fig. 11. Diagram utilizing resources for both filters.

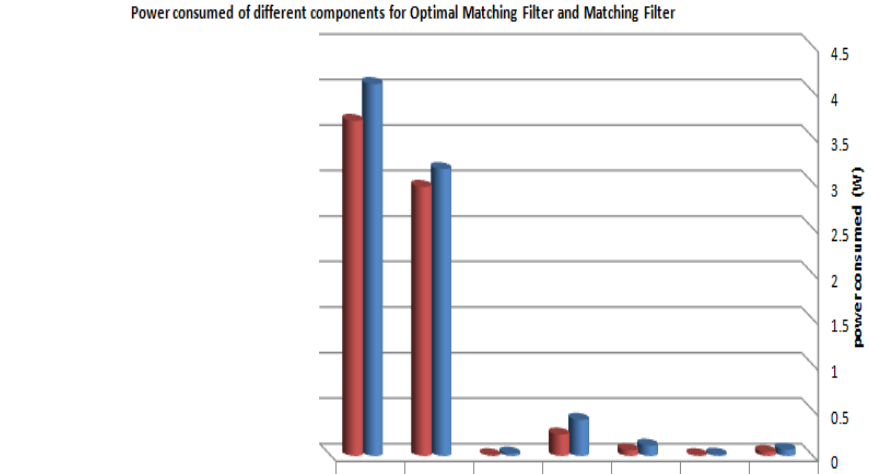


Fig. 12. Comparison of power consumed by resources for both filters.

6. Conclusions

Array circular uniform used by passive radar with SAR algorithm implemented hardware and simulated in MATLAB along with FPGA device Xilinx FPGA Spartan-3 XC3S200. This execution was substantiated with the genuine field empirical data and utilizing FM as transmitter. The results processing of MATLAB along with the output FPGA explain that the clutter of zero-Doppler can be forcefully filtered out by applied optimal matching filter in proposed system where the zero-Doppler registered the best value 10^{-4} bit error rates at 10db comparison with Doppler 3e+002, which reached about 10^{-2} bit at same db. It can be observed also that most resources items utilizing by the prototype model of matching filter are more than that utilized by optimal matching filter, this is greatly apparent when measure power by using X-power analyser where the power consumed by matching filter about 4.087 watt while less power registered by using optimal filter about 3.682 W. When making analysis for duty timing and frequency it recorded huge difference between FPGA and MATLAB in time and frequency processing, the better working frequency is for optimal matching filter registered 253.036 MHz about 3.952 nanoseconds by using FPGA processing while when processing in MATLAB registered very big difference about 7.4 seconds. In the future work the system will develop to cope with challenges at different levels by modifing algorithm to perform a devoted radar system for modern advance technique.

Nomenclatures

d	Vector weight optimal filter
h_w	Target Doppler frequency, Hz
h_x	Frequency of sampling, Hz
k	Array radius, m
K	Matrix covariance interference estimation
N	Superscript matrix of transpose
R	Elements antenna number
r	Block length depending on number of subcarrier
$S(f)$	Scan data of nine channels
$S_p(f\,;\,r\,)$	Mixed product
X	Sub-sampling factor
$X_{ref}(f\text{-}r)$	Purely reference signal with version delayed time
$y(u_w)$	Vector steering spatial
$z(u_x)$	Vector steering temporal

Greek Symbols

α	Attenuation factor ($2\pi/\gamma$)
γ	Length of the wave, Å
Φ_r	Angle of array positioned ($2\pi r/R$), deg.
ϕ	The angle scanning or angle incidence, deg.
$\otimes$, $\circ$	Correlation and product sign respectively
$\dagger$	Operation transpose hermitian factor

Abbreviations

AMD	Access Memory Direct
BER	Bit Error Rate

CPU	Central Processing Unit
CUDA	Compute Unified Device Architecture
F, R	Multi directional CPU memory per lane
FM	Frequency modulation
FPGA	Field Programmable Gates Array
GPU	Graphics Processing Unit
PBR	Passive Bistatic Radar
SAR	Synthetic-Aperture Radar

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