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PRE-CHARGE FREE SOFT ERROR HARDENED CAM CELL DESIGN FOR LOW POWER AND HIGH PERFORMANCE

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Abstract

The Content Addressable Memory (CAM) is a high throughput large capacity hardware device. It searches stored lookup data in parallel but consumes a large amount of power. NOR CAM cell offers high speed but suffers from high power consumption due to a short circuit current path in the precharge phase during mismatch. The Self-Controlled Precharge Free (SCPF) CAM cell, which removes the precharge phase offers low power consumption. As technology scales down, the reliability of memory nodes are sensitive to Soft Errors Single Event Upsets (SEUs). In this paper, a NOR CAM cell with different types of SRAM cells has been studied by inserting Double Exponential Current Pulse (DECP) at sensitive nodes of a memory cell for soft error hardened design. In addition, radiation hardened precharge-free CAM cell has been proposed for low power and high-performance design. The proposed CAM cell design and soft error hardened NOR CAM cell designs had been simulated and verified using Virtuoso tool at 45 nm Complementary Metal Oxide Semiconductor (CMOS) technology. Process corner simulations for search delay and power are performed on proposed and existing CAM cells. Simulation results show that proposed CAM cell exhibits 76.95% lesser energy than NOR-type CAM and 37.27% lesser energy than SCPF CAM cell design.

Keywords: High-speed search, Low-power, Match/miss, Pre-charge free, Radiation hardened, Single event upset (SEU).

1. Introduction

CAM is a hardware-based search system, which surmounts the software-based search systems for high throughput. CAM compares the array of stored binary words against the given search input binary word parallel within a single clock cycle [1, 2]. CAMs are useful in many high-speed search applications, which include IP routing [3], gray coding [4], image processing [5], parameter curve extraction [6], Huffman coding/decoding [7] and others. Unwanted parallel comparisons [8], a short circuit current path [9], leakage power [10] are responsible for high power consumption in a CAM. Thus, the main thread of CAM design for the research is to reduce power by novel circuit approaches without sacrificing the performance.

A CAM cell structure is designed with two basic units; storage and comparison [11]. Each CAM cell stores one bit of information through SRAM and compares that binary data through a comparison circuitry for match/miss condition at ML. All the CAM designs possess the same storage unit but differ in comparison circuitry. CAM memory is formed by an array of CAM cells arranged in rows and columns. Each row is considered as one word with separate ML and a precharge circuitry as shown in Fig. 1. CAM operation begins with writing the data in the memory cell. Once the data is written in a CAM cell, precharge is followed by an evaluation phase. Practically an array of CAM words stores unique lookup data in its rows. Thus, only one CAM word match is possible with an array of unique words. In this architecture when the data in the array of the stored word is matched with the given search input word, it returns the address of that word to the encoder through MLSA otherwise return nothing.

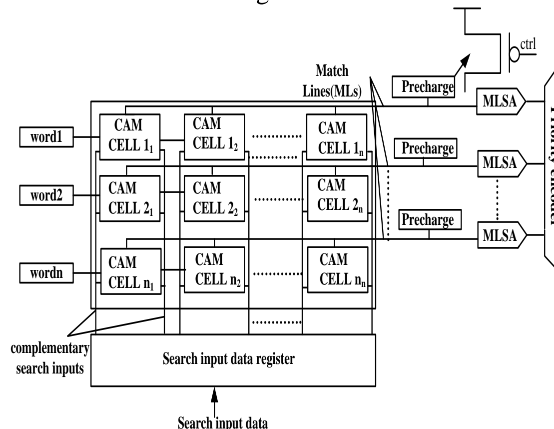


Fig. 1. Block diagram of CAM.

The reliability of memory cell designs at lower technology nodes is limited by radiation particles like protons, α-particles, and neutrons, which are caused by SEUs [12-14]. The SEUs are soft errors, which affect memory storage state temporarily. As technology scaled to nanoscale, memory cells are more sensitive to different types of radiation particles because of small node capacitance and low supply voltage [15-17]. When radiation particles induce memory cells, they can change their state and cause malfunctioning of the memory system. In some critical biomedical memory applications, the soft error can be crucial and prejudicial. Thus, it is essential to protect memory cells over SEUs in different radiation environments.

Here, DECP is modelled as SEU based on the characterization of Critical Charge ($Q_{critical}$) [18]. The critical charge is defined as minimum charge collected by the circuit when DECP strikes on sensitive nodes of the memory cell to change the state of memory. In this paper, the DECP is injected into sensitive nodes to study the memory cell for radiation hardening. SEU is said to occur when charge induced by a current pulse on the sensitive nodes of the memory cell is greater than the $Q_{critical}$ stored at that sensitive node. In literature, several types of current pulse models have been presented. Roche et al. [19] commented the current pulse model is proposed by defining the $Q_{critical}$ with the following Eq. (1). In this model, $Q_{critical}$ is marginally calculated because of neglecting some additive term I_{dpmax}T.

$$Q_{critical}=C_M\ V_{DD}+\ I_{dp\max}T \tag{1}$$

where C_M is the node capacitance, V_{DD} is the supply voltage, I_{dpmax} is maximum drain current for conduction of PMOS, and T is the flipping time of memory cell. According to Freeman [20], the current pulse model is proposed to compute $Q_{critical}$ for bipolar memories. Here, the current pulse is defined in terms of timing parameter τ_p and the total amount of charge deposited Q_t is given by the following Eq. (2).

$$I(t)=\frac{2}{\sqrt{\pi}}\frac{Q_t}{\tau_p}\sqrt{\frac{t}{\tau_p}}e^{\frac{-t}{\tau_p}} \tag{2}$$

Merelle et al. [21] and Heijman et al. [22] reported that a diffusion collection current pulse is modelled, which is more suitable for neutron strikes given by the following Eq. (3).

$$I(t)=I_m(e^{\frac{t_m}{t}})^{\frac{3}{2}}e^{\frac{-3t_m}{2t}} \tag{3}$$

where t_m represents maximum value current I_m. Finally, most widely [23] used current pulse model has doubled exponential, which is given by the following Eq. (4), where τ_f and τ_r represent falling and rising time constants respectively, Q_{de} is a positive or negative charge. In the present work, a double exponential current pulse with rising time start = 6 ns, rise time constant = 0.5 ns, fall time start = 7 ns and fall time constant = 0.5 ns is inserted at sensitive nodes of CAM cell as shown in Fig. 2.

$$I_{de}=\frac{Q_{de}}{\tau_f-\tau_r}(e^{\frac{t}{\tau_f}-\frac{t}{\tau_r}}-e^{\frac{t}{\tau_f}-\frac{t}{\tau_r}}) \tag{4}$$

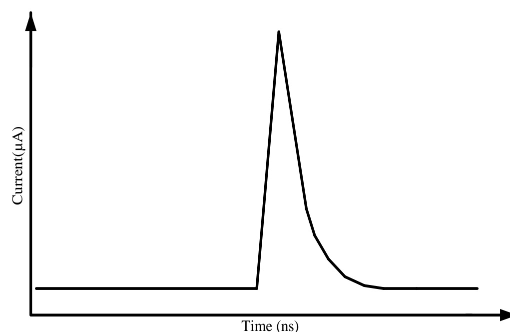


Fig. 2. Double exponential current pulse.

In this paper, DECP is induced on different types of NOR CAM memory core cells for radiation hardening memory design. In basic 6T SRAM, the cells flip its memory logic state easily if any radiation particles induced on the sensitive nodes of memory core cell. There is no circuitry to recover the memory state to come back its initial state. Thus, the NOR CAM with 6T SRAM as memory cell changes its ML output from its original state when it is flipping from 0 to 1 SEU and 1 to 0 SEU. To avoid the flipping of memory state from its initial state due to radiation [24], NMOS stack-based memory cell was represented but this design work only for recovering the memory cell when it is flipping from state 0 to 1 SEU. Calin et al. [25] presented in Dual Interlocked Storage Cell (DICE), which is controlled by dual node feedback, the memory cell is free of radiation effects against a single node upset but fails at multiple node upsets. Lin et al. [26] presented a 13 transistor memory cell in which, to protect the memory cell from multi-node upset. However, this memory cell design requires a large layout area and power consumption. According to Guo et al. [27], Radiation Hardened Memory (RHM) cell is proposed, which is immune to single and multiple-node upset. Here, NOR CAM cell with RHM cell is designed, which works for recovering the stored data when it is flipped from state 0 to 1 SEU and 1 to 0 SEU. In this paper, we designed a Radiation Hardened Precharge Free (RHPF) CAM memory cell design in order to reduce the total average power and search delay. The proposed CAM design is compared with basic NOR CAM cell [11] and SCPF CAM cell [28]. Simulation results show that the proposed design significantly reduces both power and search delay.

The rest of the paper is organized as follows: Section 2 discusses the effect of radiation particles when DECP strike on different NOR CAM memory cells. Section 3 explains proposed CAM cell design. Section 4 explains the simulation results obtained from the Cadence Virtuoso tool. Section 5 concludes the brief.

2. Radiation hardened CAM memory cell

2.1. NOR CAM cell with basic 6T SRAM cell

In NOR CAM cell, the binary data 0 or 1 is stored in memory by 6T SRAM cell. Each NOR CAM cell stores one bit of data through complementary bit lines BL and BL_{bar}. Four transistors are required to compare the complementary binary data *P* and *Q* through complementary search lines SL and SL_{bar} as shown in Fig. 3. These comparison transistors form two separate pull-down paths from the ML. CAM operation begins with writing the data in SRAM cell. Data in SRAM is stored when WL is high. CAM search operation starts when WL is low. In the precharge phase, ML output is high irrespective of stored data and search input. Search operation always starts by pre-charging the ML. In the evaluation phase, if there is a mismatch, one of the pull-down paths is connected to ground, which discharges ML to ground. If there is a match, no pull-down path is connected to ground. Hence ML retains the precharge stage.

In this structure, sensitive node *P* or *Q* is injected by DECP to know the effect of radiation particle on memory state. Here, memory core cell is easily affected by SEU and flip its state from 0 to 1 or 1 to 0. It fails to recover the memory from its initial state from both the states. Assume that the initial state of *P* is 0 and *Q* is 1. If DECP strikes on node *P*, then this node is flipped to 1. Transistor P_2 and N_4 will turn off and on respectively and, thereby node *Q* changes its state to 0. Similarly, if DECP strikes on node *Q*, then this node is flipped to 0. Transistors P_1 and N_3 turn

on and off respectively and node *Q* changes its state to 1. In this CAM cell, there is no recovery circuitry to flip its state to the initial value, and hence it results in both 0 to 1 SEU and 1 to 0 SEU to occur. Thus, NOR ML output with 6T SRAM cell shows incorrect output for match/miss if radiation particle strikes on sensitive nodes of a memory cell.

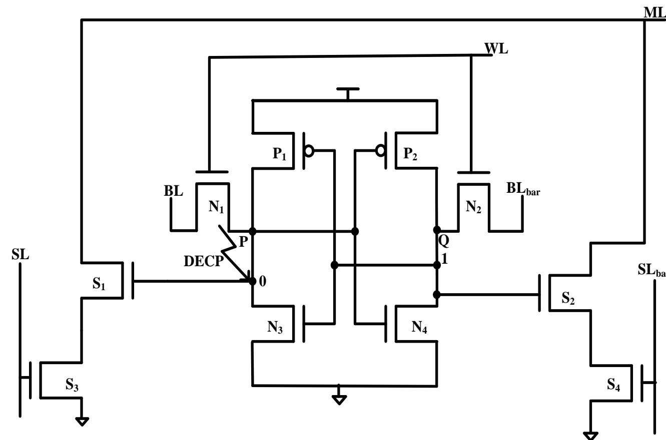


Fig. 3. NOR CAM cell with 6T SRAM cell.

2.2. NOR CAM cell with NS radiation hardened SRAM cell

NOR CAM cell with NMOS stacked (NCNS) memory cell as a storage circuit is as shown in Fig. 4. It uses NMOS as a stacked structure and two surrounding PMOS transistors additionally when compared with conventional 6T SRAM cell. Here, memory core cell is capable of recovering the memory states of SEU only when it is flipped from 0 to 1 state. It fails to retrieve the memory state when it is flipped from 1 to 0. Assume that the sensitive nodes in memory cells are *P*, *Q*, *R*, and *S*. The sensitive nodes are initially set to (P = 1, Q = 0, R = 1, S = 0). If DECP is injected at node Q, then it flips from state 0 to 1. The transistors N_3 and P_2 are turned on, and off respectively. Nodes *R* and *S* are unaffected by the current pulse.

Thus, these nodes maintain the memory to be an initial state. As N_1, and N_2 transistors are still on, the initial state is recovered from the flipped state, even though the cell is struck by a radiation particle. If DECP is injected at node *P*, then it flips from state 1 to 0. Then the transistors N_1, N_2, P_2, and P_3 are turned off and transistors N_3, N_4, P_4, and P_1 are turned on. Here, the nodes *R* and *S* change their initial states. The outputs *P* and *Q* do not recover from their flipped state, which results in SEU to occur. Thus, when the radiation particle strikes the sensitive node of the memory cell, the NCNS memory cell shows correct ML output for miss/match case only when it is flipping from 0 to 1 state and shows incorrect ML output when flipping from 1 to 0 state.

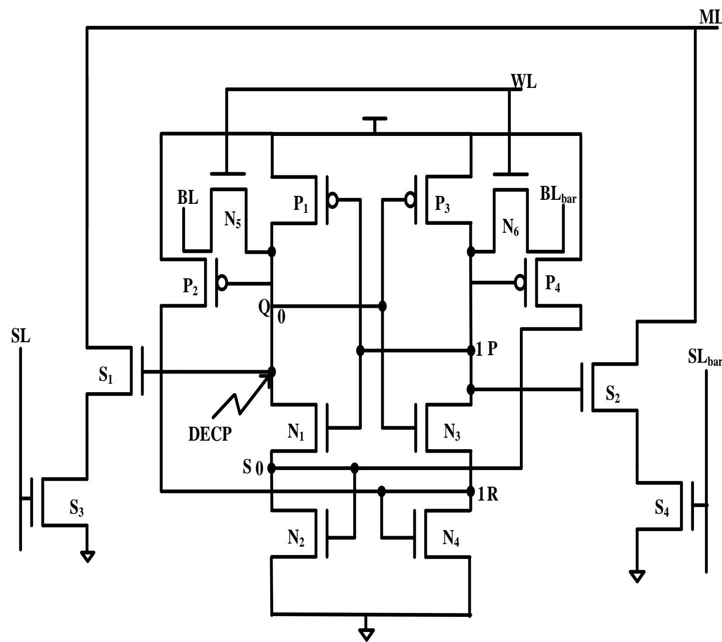


Fig. 4. NOR CAM cell with NS SRAM cell.

2.3. NOR CAM cell with RHM radiation hardened SRAM cell

NOR CAM cell with radiation hardened memory (NCRHM) cell is designed by adding two PMOS stacked transistors to NCNS cell. The NMOS access transistor is replaced by PMOS access transistor as shown in Fig. 5. According to the physics of SEU, when SEUs strike an NMOS transistor, a negative transient pulse is generated and when SEUs strike a PMOS transistor, a positive transient pulse is produced [27]. Assume that the nodes are initially set to (P = 1, Q = 0, R = 1, S = 0). The nodes Q, R, and S are sensitive nodes and P is not a sensitive node.

If node P is induced by DECP, then the node P is unaffected because SEU induces positive transient pulse, which does not change the memory state as it is surrounded by PMOS transistor. Similarly, for the initial set (P = 0, Q = 1, R = 0, S = 1), the nodes P, R and S are sensitive nodes and Q is an insensitive node.

In this state, if the node P is injected by DECP, then it changes its state to 1. This flip turns off P_3, P_5 transistors and turns on N_3 transistor temporarily. Then node Q stays at initial state 1 as it enters into high impedance state and node S stays at initial state 1 because of capacitance effect. This allows N_2 transistor to be on which, in turn, flips node R back to its initial state. As a result, the node Q is recovered to its initial state. Hence, this NCRHM cell design is free from 0 to 1 SEU and 1 to 0 SEU. Thus, the ML output of NCRHM cell shows the correct functionality for match/ mismatch even though DECP strikes on sensitive nodes of memory cell states.

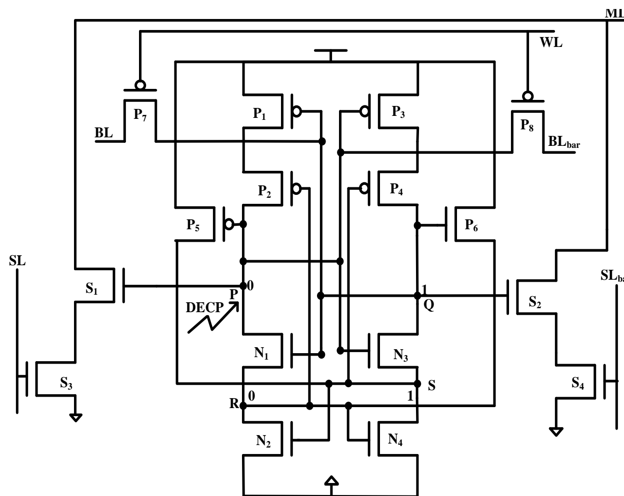


Fig. 5. NOR CAM cell with RHM SRAM cell.

3. Proposed CAM cell design

Based on studies by Mohammed and Kittur [9], all CAM designs at the circuit and architectural level discussed are based on precharge applied to ML. The power consumption and search delay of these CAM cell ML outputs depend on circuit behaviour at write phases, the precharge phase, and evaluation phase. In this type of CAM cell design, the power and search delay of ML output reduction is based on novel design approaches at the circuit and architecture level. Mohammed and Kittur [9] identified for the first time a short circuit current path in precharge phase consume more power and to avoid that, they propose a novel CAM cell without a precharge phase, which reduces search delay and power consumption when compared with any other precharge based architectures. Another precharge-free CAM named as SCPF-CAM cell is proposed, which overcomes the disadvantage of precharge-free CAM cell design but with a small increment in power consumption [28]. In the present work, we developed a low power self-controlled precharge free CAM cell, which is radiation hardened.

3.1. SCPF CAM cell

Precharge-free CAM structure has been developed to reduce power. Mohammed and Kittur [9] explained that a CAM structure without a precharge phase is proposed. Here, the control of ML output is based on the control bits. This structure eliminates the problem of short- circuit current path and charge sharing problem. Further, according to Mahendra et al. [28], the authors identified that due to a cascade chain of the charge control circuit, the search delay is high, which may be reduced. To overcome this problem, SCPF CAM cell is developed as shown in Fig. 6. The data is stored in this CAM memory by 6T SRAM cell. Once the data is written, the evaluation phase starts to compare the search input data and stored data. This structure consists of two comparison transistors to compare with the stored data. In this structure, ML output for match/miss control is based on the charge at the node S. If search input misses with the pre-stored data, then it passes low value through transistor M_9 else it passes high value through transistor M_8. The power

and delay are the two important performance parameters of the CAM memory design, which are given by Eqs. (5) and (6).

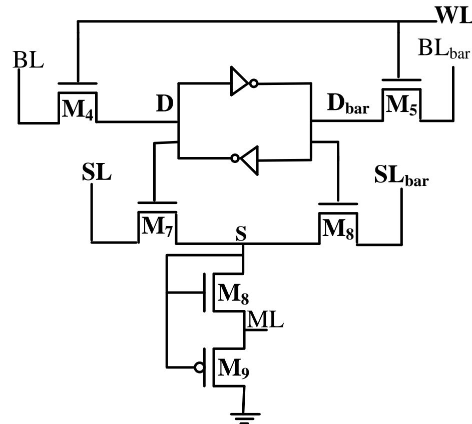


Fig. 6. SCPF CAM cell.

Power consumption of CAM cell for a search cycle is given by:

$$Power = (\alpha - 1)\ C_{ML}\ \ V^2{}_{DD} \tag{5}$$

where α = switching activity, C_{ML}= matchline capacitance, V_{DD}= supply voltage.

Delay of CAM cell for a search cycle is given by

$$Delay = T_D + T_{RC} \tag{6}$$

where T_D = transistor delay, T_{RC} = match line time constant.

Elimination of the precharge phase provides the precharge-free CAM to perform search operation with high speed and low power consumption. Equations (7) and (8) represent the time required to complete the search clock cycle for precharge and precharge free CAM designs respectively [28].

Total time required to complete one search operation for a precharge base CAM cell design is as follows:

$$T_p = T_{wr} + T_{pre} + T_{SL} \tag{7}$$

Total time required to complete one search operation for a precharge-free CAM cell design is:

$$T_{pf} = T_{wr} + T_{SL} \tag{8}$$

where T_P is the total precharge time, T_{pf} is the total precharge free time, T_{wr} is the write time, T_{pre} is the precharge time and T_{SL} is the evaluation time.

3.2. Radiation hardened precharge free CAM

Mohammed and Kittur [9] commented that SCPF CAM cell structure offers high search speed but consumes large power when being compared. In precharge-free CAM designs, the binary data storing and comparing of that stored data are performed

in a write phase followed by evaluation phase. Thus, in this type of designs, the power and search delay depends on circuit behaviour at write phase and evaluation phase and moreover leakage power play an important role in power consumption as technology scaled to nano. In this concise, to reduce power further without degrading the performance, a novel CAM cell structure is proposed and is shown in Fig. 7.

The operation begins with storing the data in the memory core cell. The storage cell of SCPF CAM is replaced by RHM cell. In this proposed RHPF CAM cell, the access transistors are implemented with transmission gates T_1 and T_2 and a diode-connected transistor N_5 is added for low power consumption.

The T_3 and T_4 are the two transmission gates used for comparing the stored data. Write phase begins with switching on transmission gates T_1 and T_2 through word lines WL_1 and WL_2, and then the data stored in the memory cell is bypassing complementary bit information through BL and BL_{bar}.

Evaluation phase starts by switching off transmission gates T_1 and T_2 through word lines WL_1 and WL_2, and then the data stored is compared with the search input through complementary search lines SL and SL_{bar}. The ML output match/miss depends on the charge developed at node *N*.

If there is a match between given search input and stored data, ML is high through transistor P_7 else ML is low through transistor N_6. To reduce leakage power, the proposed RHPF circuit is constructed with gated V_{dd} with LP_1 transistor and gated ground with LN_1 transistor [10]. The transmission gate access transistors help to reduce the write power [29].

Further, the comparison transistors of the transmission gate help to improve the voltage swing on the node *N* and also help to reduce the power and search delay. Thus, the proposed RHPF cell structure improves total average power in both the write phase and evaluation phase. Hence this design is suitable for constructing an array of longer word lengths with high-speed search applications with reduced energy and most importantly immune to radiation effect.

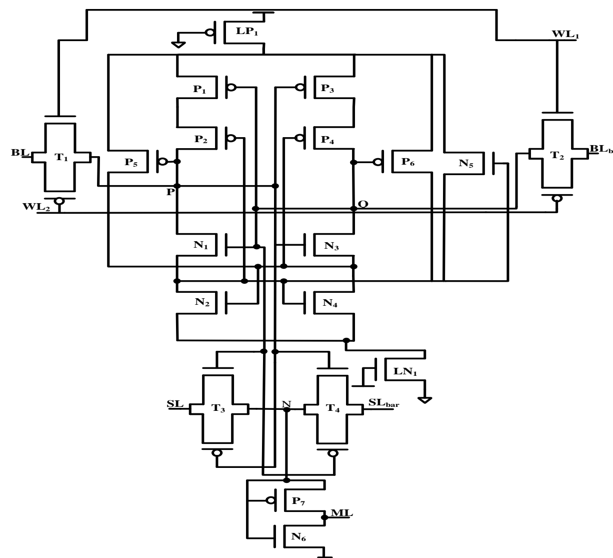


Fig. 7. RHPF CAM cell.

4. Simulation Results

NOR CAM cell with different storage SRAM cells has been simulated by inserting DECP at sensitive nodes of the memory cell. Simulation is performed in two clock cycles. The first clock cycle includes writing followed by precharge and evaluation phase. Here, at first clock cycle, the DECP is inserted at sensitive nodes of memory storage states for radiation effect. The second clock cycle also includes writing followed by precharge and evaluation phase, which is free of radiation particle.

Simulation results show that NOR CAM cell with RHM as SRAM memory cell has the capability to recover back its initial states even though the DECP strikes at sensitive nodes of the memory cell. Figures 8 and 9 show the radiation effect on NOR CAM with 6T SRAM cell with a current pulse value of 50 μA. The waveform shows that radiation pulse struck on NOR CAM cell with 6T SRAM cell deviate the ML output from its actual ML output in both the storage states 0 and 1. Figures 10 and 11 show the radiation effect on NOR CAM with NS SRAM cell with a current pulse value of 50 μA. The waveform shows that the NOR CAM ML output deviates from its actual output only for SEU 1 to 0. Figures 12 and 13 show the radiation effect on NOR CAM with RHM SRAM cell with a current pulse value of 50 μA. The waveforms clearly indicate that the NOR CAM ML output will not deviate from its actual value even with occurrence of SEU 0 to 1 and 1 to 0. In addition to this, we also simulated the proposed RHPF CAM along with the exciting CAM cell design in 45 nm CMOS technology. Total time required to complete one single clock cycle for precharge based NOR CAM cell is T+0.66 ns and for precharge free design is T ns, where T represents the time period equivalent to 1.33 ns. Simulation results showed that the proposed design has 76.95% less energy than NOR-type CAM cell and 37.27% less energy than SCPF-CAM cell.

Table 1 shows the performance comparisons of proposed and existing CAM cell designs. Delay and power are the important performance parameters for CAM design. An Exhaustive analysis on delay and power are performed on proposed CAM design by varying the temperature and supply voltage. It is observed that when the temperature goes on increasing, ML delay increases and there is a slight decrement in average power. It is also noted that ML delay decreases with increment in supply voltage. The related plots are depicted in Figs. 14 to 16.

Process corner simulations for existing and proposed CAM cell designs are also simulated for power and delay comparisons. The proposed design work fines at all the process corners like typical, fast and slow corners. Depending on the design and condition of operation the worst case and best case simulation can be a corner case simulation. From the simulation results, it is observed that the worst case and best case search delays have occurred at SS (slow nMOS slow pMOS) and FF (fast nMOS fast pMOS) process corners respectively. The search delay is high at SS process corners because the threshold voltage is high at SS, i.e., (0.6 mV to 0.7 mV) whereas it is low at FF, i.e., (0.48 mV to 0.52 mV). It is evident that high threshold voltages will increase the search delay. In the similar grounds, we can understand that higher threshold voltage at FF results in high power consumption. It is observed that the least power is 0.132 (μW) and worst power is 0.174 (μW), best search delay is 3.9 (pS) and worst search delay is 8.14 (pS). The process corner simulation results for average power and ML delay are depicted in Figs 17(a) and (b).

Table 1. Performance comparisons with prior works.

Type of CAM	NOR CAM [11]	SCPF CAM [28]	Proposed CAM
Supply voltage	1 V	1 V	1 V
technology (nm)	45	45	45
Cell type	NOR	Precharge free	Precharge free
Average power (µW)	0.460	0.2544	0.1593
ML delay (pS)	18.4	22.7	5.66
Energy (fJ)	0.92	0.338	0.212

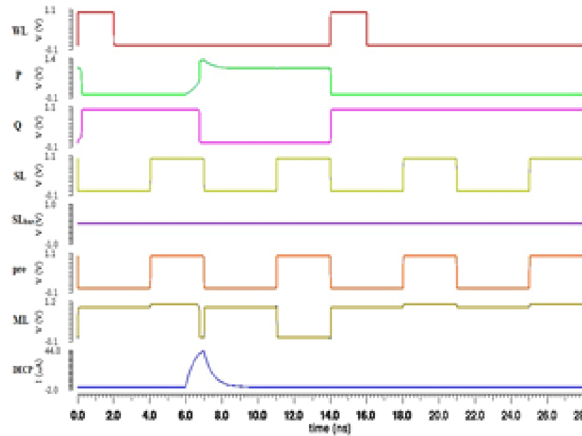


Fig. 8. Simulation results of NOR CAM cell with 6T SRAM cell, which shows the ML output changed to miss due to DECP strike on sensitive node.

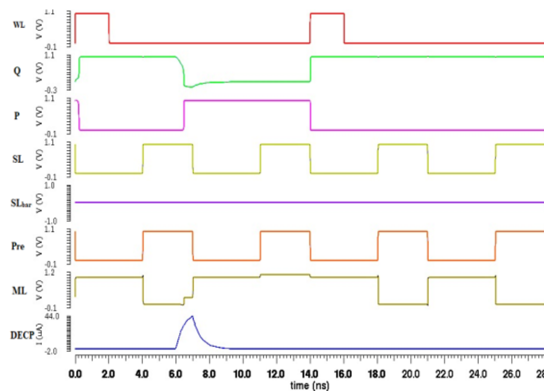


Fig. 9. Simulation results of NOR CAM cell with 6T SRAM cell, which shows that ML output changed to to match due to DECP strike on sensitive node.

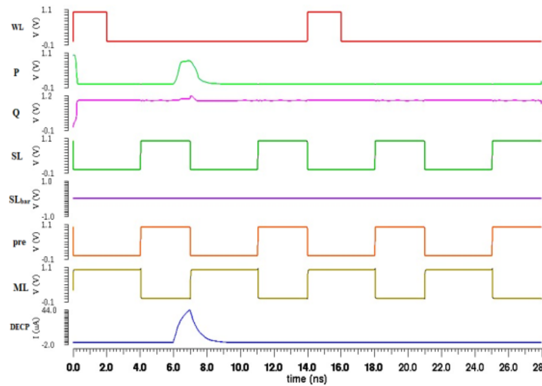


Fig. 10. Simulation results of NOR CAM cell with NS SRAM cell. Which shows that ML output does not change even though DECP strike sensitive node.

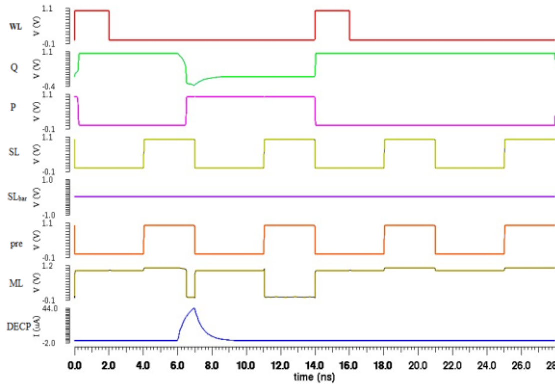


Fig. 11. Simulation results of NOR CAM cell with NS SRAM cell, which show that ML output change to miss due to DECP strike on sensitive node.

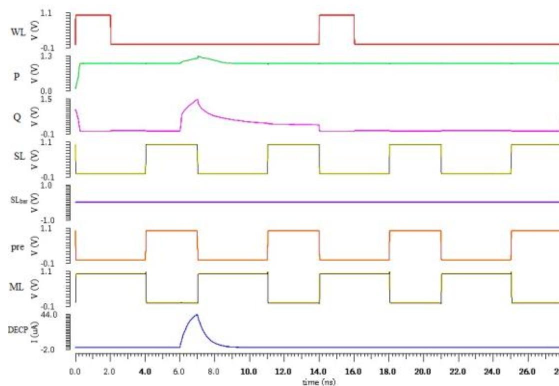


Fig. 12. Simulation results of NOR CAM cell with RHM SRAM cell, which show that ML output does not change even though DECP strike on sensitive node.

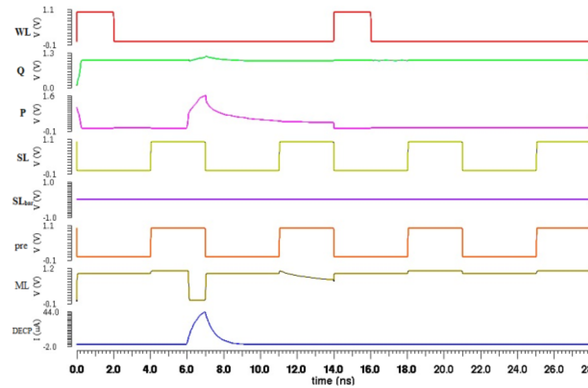


Fig. 13. Simulation results of NOR CAM cell with RHM SRAM cell, which show that ML output does not change even though DECP strike on sensitive node.

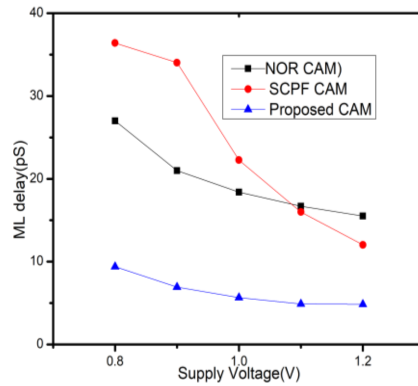
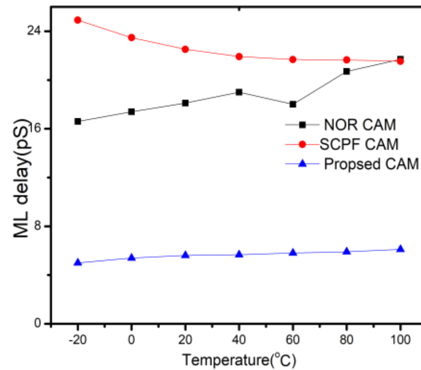


Fig. 14. ML delay comparisons at various supply voltage.



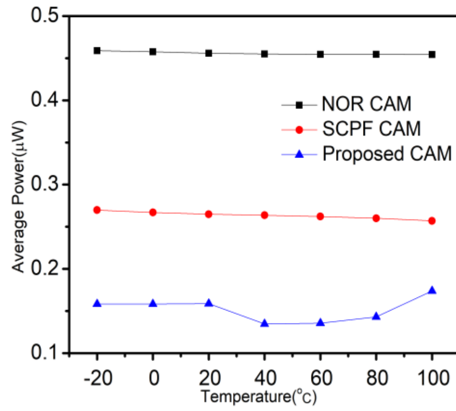
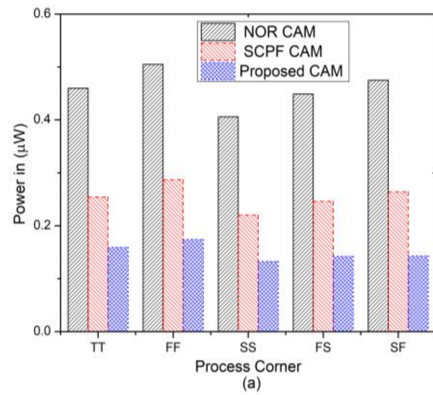


Fig. 16. Average power comparisons at different temperatures.



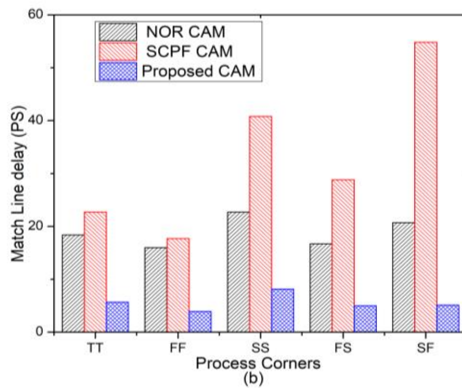


Fig. 17. (a) Process corner versus average power.
(b) Process corner versus ML delay.

5. Conclusions

NOR CAM cell with 6T SRAM cell and NS SRAM cell suffer from recovering back to its initial state when DECP is hit on sensitive nodes. This paper presented radiation hardened memory SRAM cell, which has the capability to recover the memory states even the DECP strike on sensitive nodes of memory. In addition to this, precharge-free radiation hardened CAM cell for low power and high performance has been proposed. The proposed CAM cell has power and search delay comparable to NOR CAM cell and SCPF CAM cell. Simulation results showed that the energy of proposed CAM cell is 76.95% and 37.27% lesser than NOR-type CAM cell and SCPF CAM cell. Thus, the proposed design is suited for low power, high search delay and radiation hardened CAM design for various applications.

Nomenclatures

C_M	Node capacitance, C
I_{dpmax}	Maximum drain current, ampere
I_m	Maximum current, ampere
$Q_{critical}$	Critical charge, C
Q_t	Total charge deposit, C
t	Flipping time
t_m	Maximum value of current, I_m
V_{DD}	Supply voltage, V

Greek Symbols

τ_f	Falling time constant
τ_p	Timing parameter
τ_r	Rising time constant

Abbreviations

CAM	Content Addressable Memory
CMOS	Complementary Metal Oxide Semiconductor
DECP	Double Exponential Current Pulse
DICE	Dual Interlocked Storage Cell
ML	Match Line
MLSA	Match Line Sensing Amplifier
NCNS	NOR CAM Cell with NMOS Stacked
NCRHM	NOR CAM Cell with Radiation Hardened Memory
RHM	Radiation Hardened Memory
RHPF	Radiation Hardened Precharge Free
SCPF	Self Controlled Precharge Free
SEU	Single Event Upset
SRAM	Static Random Access Memory

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