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ULTRA-LOW VOLTAGE OPERABLE BULK-DRIVEN SECOND GENERATION CURRENT CONVEYOR BASED FILTERS WITH SINGLE-INPUT AND SINGLE-OUTPUT

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Abstract

Nowadays, Bulk-driven principal is being hugely incorporated in designing of analogue signal processing modules so as to meet the rising demand for highly compact and portable CMOS integrated circuits, which essentially require ultra-low voltage supply (< 1 V) for their operation. In this paper, we present five different Single-Input-Single-Output (SISO) filter configurations using a single Bulk-driven Second Generation Current Conveyor (BD-CCII). These include first-order Current-Mode (CM) Low-Pass (LP), High-Pass (HP) configuration and second-order Voltage-Mode (VM) Low-Pass (LP), Band-Pass (BP) and High-Pass (HP) sections. A BD-CCII structure operating at ±0.5 V with large bandwidth and decent power consumption in a minimal transistor structure has been utilized for realization of these filters. To evaluate and verify the performance of implemented circuits PSPICE simulations have been carried out using CMOS 0.18 µm standard TSMC technology.

Keywords: Bulk-driven, Current-mode, First-order, High-pass, Low-pass, Low voltage, Second-order, Voltage-mode.

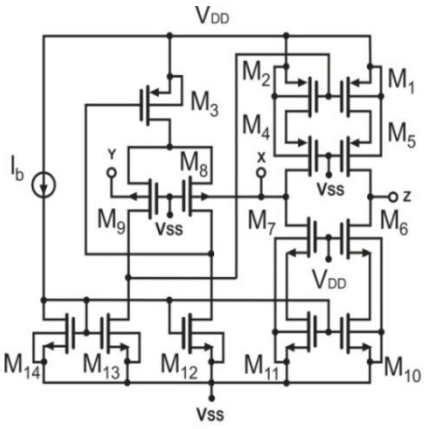
1. Introduction

In recent times, low voltage (< 5 V) and ultra-low voltage (< 1 V) circuit design strategies have drawn tremendous attention of the analogue designers [1-3]. Razavi [4] reported that it is because while down-sizing the device dimensions and supply voltage requirements, there is always a constraint on reducing the Threshold Voltage (V_T) value, needed to completely turn-on a MOSFET device. To overcome such limitations of scaling and fulfil the ever-rising demand for portable electronics, various low-voltage low-power design techniques have come around. According to Ferri and Guerrini [5] and Senani et al. [6], consequently, the emphasis is being laid on building low-voltage operable analogue signal processing applications like filters, oscillators, amplifiers, multipliers, dividers, etc. Bulk-Driven (BD) technique is one such promising solution to LV designing today. In BD technique, the gate-source is set to a sufficient DC value to form an inversion layer under the gate oxide and input is applied to the bulk terminal of the transistor. Bulk voltage can control the thickness of the conduction channel, through the body effect of a MOS transistor. Thus, drain current can be modulated by varying the input applied at bulk and V_T can either be reduced or removed from the signal path. Circuits employing BD transistors have design simplicity along with reduced voltage and power consumption.

Most signals exist in the analogue form in nature. In signal processing, filters are frequently used for allowing particular frequency components to pass while rejecting others. Analogue filters do not have to convert the signal into digital form; hence, there is no requirement for an Analog to Digital Converter or Digital to Analog Converter. Second generation current conveyor [7-10] is the most attractive and versatile current-mode analogue building block, especially for realizing active filters. It is an abstraction for a three terminal device intended to implement different types of analogue signal-processing functions. CCII offers a number of advantages such as inherent wider bandwidth, simpler circuitry, low power consumption, better dynamic range, electronic tuning, etc., which makes it a good alternative to operational amplifiers (Op-amps). Bulk-driven analogue signal processing circuits [11-15] with current conveyors have not been explored much before. T, the major intention of this brief is to study the bulk-driven current conveyor based simple filter designs.

A few bulk-driven second-generation current conveyors are available in open literature [16-20]. Among these, Tonk and Afzal [20] provide the best performance in terms of high current and voltage bandwidth along-with decent power consumption in a minimal transistor structure. This BD-CCII structure refers to Fig. 1, comprises of only 14 transistors and operates at an ultra-low supply voltage of ±0.5 V. Aspect ratios of all transistors are given in Table 1. BD-CCII is represented with the same characteristic matrix, see Fig. 1(a), as the traditional second generation current conveyor. ±100 µA is its linear current range and ±250 mV is the rail-to-rail voltage operation range. For the BD-CCII [20], 72 MHz and 114 MHz are the 3-dB current (Iz/Ix) and voltage (Vx/V_Y) bandwidths respectively. In the next section, two first-order current-mode filters: LP, HP; have been proposed using a single BD-CCII. Subsequently, three second-order voltage mode filters based on single BD-CCII: LP, BP and HP sections; have also been implemented. PSPICE simulations have been performed using TSMC 0.18 µm standard CMOS technology. Further, all the results obtained have been discussed.

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ I_Z \\ V_Y \end{bmatrix}$$



(a) Characteristic matrix. **(b) Schematic diagram.**

Fig. 1. Bulk-driven second generation current conveyor.

Table 1. MOS transistor sizing.

MOS transistors	W/L (μm/μm)
M1, M2	100/0.3
M3	18/0.3
M4, M5	100/2
M6, M7	50/2
M8, M9	10/0.3
M10, M11	40/0.3
M12, M13, M14	4/0.3

2. First-Order Current-Mode Filters

The proposed CM filters make use of only one BD-CCII along-with three grounded passive components, for obtaining the HP and LP response. Figures 2 and 3 depict block diagrams of the first-order low-pass and high-pass configuration respectively. The routine analysis yields the following current transfer function, cut-off frequency and gain for the first-order low-pass filter configuration.

$$\frac{Io}{Ii} = \frac{\frac{1}{R_2C_1}}{s+\frac{1}{R_1C_1}} \; ; \; \omega_o = 1/R_1C_1 \; ; \; H_{lp} = R_1/R_2 \tag{1}$$

For the high-pass filter, the current transfer function, cut-off frequency and gain are given below:

$$\frac{Io}{Ii} = \frac{s\frac{R_2}{R_1}}{s+\frac{1}{R_1C_1}} \; ; \; \omega_o = 1/R_1C_1; \; H_{hp} = R_2/R_1 \tag{2}$$

From Eqs. (1) and (2), it can be seen that the gain for low-pass and a high-pass filter can be independently tuned through R_2 without disturbing pole-ωo.

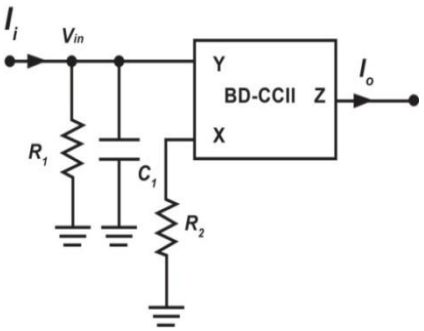


Fig. 2. First-order LP filter.

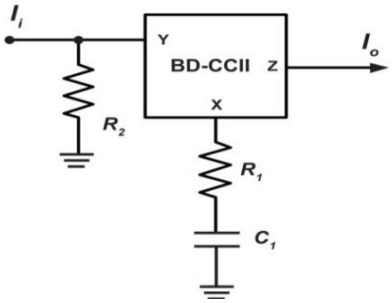


Fig. 3. First-order HP filter.

3. Second-Order Voltage-Mode Filters

The circuit of second-order voltage-mode low-pass, band-pass and high-pass filter sections consist of one BD-CCII along-with five grounded passive components. Figure 4 to 6 represent block diagrams of the low-pass, band-pass and high-pass configurations respectively.

Routine analysis yields following voltage transfer function, cut-off frequency and gain for the second-order filters. It can be seen from Eq. (3) that the gain of LP filter can be independently tuned through R_2 without disturbing pole-ωo and pole-Q.

$$\frac{Vo}{Vi} = \frac{\frac{1}{R_2R_1C_1C_2}}{s^2+s\left(\frac{1}{R_3C_2}+\frac{1}{R_1C_1}\right)+\frac{1}{R_3R_1C_1C_2}};\ \omega_o=1/\sqrt{(R_1R_3C_1C_2)};\ H_{lp}=R_3/R_2; \quad (3)$$

$$Q=\frac{1/\sqrt{(R_1R_3C_1C_2)}}{\left(\frac{1}{R_3C_2}+\frac{1}{R_1C_1}\right)}$$

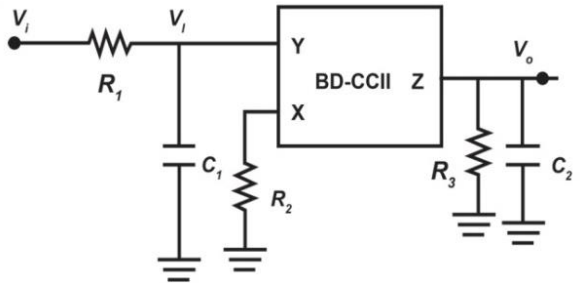


Fig. 4. Schematic of second-order LP filter.

In the configuration depicted by Fig. 4, if we interchange R_1 and C_1, we get a second-order band-pass response. For this BP filter the voltage transfer function, cut-off frequency and gain are:

$$\frac{Vo}{Vi} = \frac{s\frac{1}{R_2C_2}}{s^2+s\left(\frac{1}{R_1C_1}+\frac{1}{R_3C_2}\right)+\frac{1}{R_3R_1C_1C_2}};\quad \omega_o=1/\sqrt{(R_1R_3C_1C_2)};\quad Q=\frac{1/\sqrt{(R_1R_3C_1C_2)}}{\left(\frac{1}{R_3C_1}+\frac{1}{R_1C_2}\right)}\quad H_{bp} = R_1R_3C_1/R_2\,(R_1C_2+R_3C_1) \quad (4)$$

Again, the gain can be tuned independently through R_2 without disturbing pole-ωo and pole-Q. There is one limitation of these designs. In the pole-Q expressions for above filters, the denominator is greater than the numerator. Hence, the circuit can realize only low Q values.

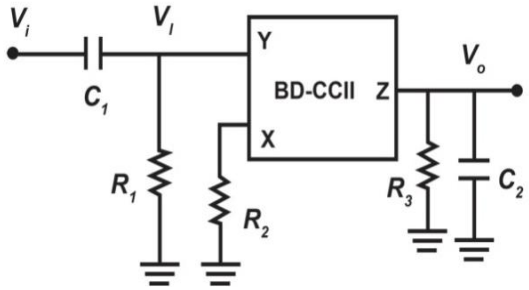


Fig. 5. Schematic of second-order BP filter.

For HP filter the voltage transfer function, cut-off frequency and gain are:

$$\frac{Vo}{Vi} = \frac{s^2\frac{R_3}{R_2}}{s^2+s\left(\frac{1}{R_1 C_2}+\frac{1}{R_2 C_1}\right)+\frac{1}{R_2 R_1 C_1 C_2}} \; ;\omega_o = 1/\sqrt{(R_1 R_2 C_1 C_2)};\; H_{hp} = R_3/R_2; \quad (5)$$

$$Q=\frac{1/\sqrt{(R_1 R_2 C_1 C_2)}}{\left(\frac{1}{R_1 C_2}+\frac{1}{R_2 C_1}\right)}$$

It can be seen from Eq. (5) that the gain of HP filter can be independently tuned through R_3 without disturbing pole-ωo.

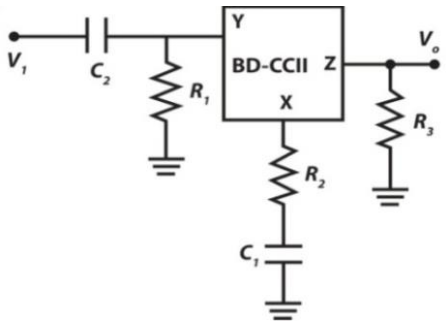


Fig. 6. Schematic of second-order HP filter.

Sensitivity study

The sensitivities of filter parameters are evaluated with respect to active and passive components is given below.

Sensitivity value of CM filters (Figs. 2 and 3):

$$S^{\omega o}_{R1,C1} = S^{Hlp}_{R2} = -S^{Hlp}_{R1} = -1, S^{Hlp}_{\alpha,\beta} = 1; S^{\omega o}_{R1,C1} = S^{Hhp}_{R1} = -1, S^{Hhp}_{R2} = S^{Hlp}_{\alpha,\beta} = 1 \quad (6)$$

It can be inferred from above and the calculations given in Table 2 that the current-mode and voltage-mode filters designed exhibit low and attractive sensitivity of pole-ωo and pole-Q with respect to the various circuit elements.

Table 2. Sensitivity figures of VMF of Figs. 4 to 6.

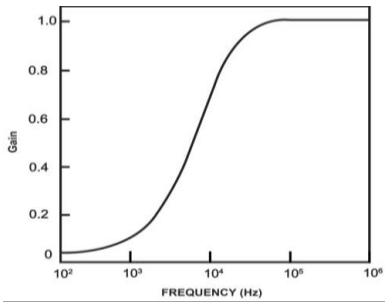
Sensitivity	VM-LPF		VM-HPF		VM-BPF	
To/of	ωo	Q	ωo	Q	ωo	Q
R_1	-1/2	$\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$	-1/2	$-\frac{(R_1C_2 - R_2C_1)}{2(R_1C_2 + R_2C_1)}$	-1/2	$\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$
R_2	-	-	-1/2	$\frac{(R_1C_2 - R_2C_1)}{2(R_1C_2 + R_2C_1)}$	-	-
R_3	-1/2	-	-	-	-1/2	$-\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$
R_4	-	-	-	-	-	-
C_1	-1/2	$\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$	-1/2	$\frac{(R_1C_2 - R_2C_1)}{2(R_1C_2 + R_2C_1)}$	-1/2	$\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$
C_2	-1/2	$-\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$	-1/2	$-\frac{(R_1C_2 - R_2C_1)}{2(R_1C_2 + R_2C_1)}$	-1/2	$-\frac{(R_3C_2 - R_1C_1)}{2(R_3C_2 + R_1C_1)}$

4. Simulation and Results

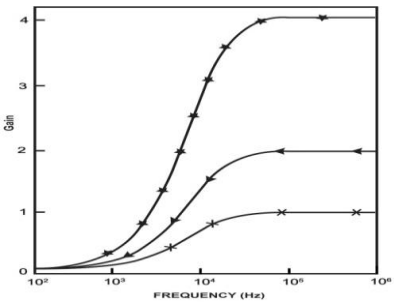
The filter configurations given in Figs. 2 to 6 have been simulated using level 7 PSPICE parameters of 0.18 µm CMOS technology with supply voltage of ±0.5 V. Wilson [8] commented that from the few BD-CCII based filter configurations published in the literature till date, the majority have been designed for cut-off and central frequencies limited to few kHz only. This is because these circuits typically find usage in the processing of biological signals, which have limited amplitude (in µA) and frequency (few kHz).

4.1. Current-mode filter

An input of 10 µA, 1 kHz is provided to the CM filters to verify their characteristic response. Figure 7(a) represents first-order high-pass response. The filter has been designed for a cut-off frequency (f_o) of 11 kHz and the observed frequency is equal to 9.54 kHz. Values chosen for the passive components are R_2 = 1 kΩ, R_1 = 0.91 kΩ and C_1 = 15.9 nF. R_2 is used to control the filter's gain, as shown by figure 7(b). First-order CM LPF, as seen in Fig. 8(a), has been designed for a slightly higher cut-off frequency of 523 kHz. In this case, observed f_o is 524.80 kHz. For this design, values of the passive component chosen are R_1 =4 kΩ, R_2 = 4 kΩ and C_1 = 76 pF. Again R_2 can be seen to control the filter's gain independently, as depicted by Fig. 8(b).

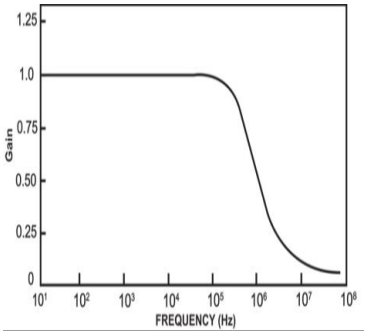


(a) Frequency response of CM first-order HPF.

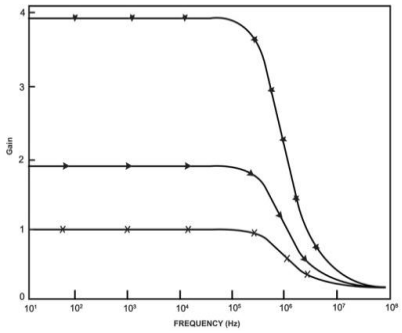


(b) Tuning of HPF gain through R_2: x = 1 k, ^ = 2 k ;*= 4 k.

Fig. 7. Simulation results of CM first-order LPF.



(a) Frequency response of CM first-order LPF.



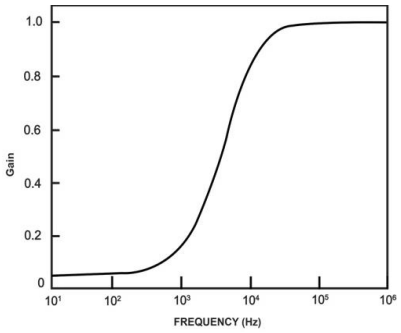
(b) Tuning of LPF gain through R_2: x = 4 k; ^ = 2 k;* = 1 k.

Fig. 8. Simulation results of CM first-order LPF.

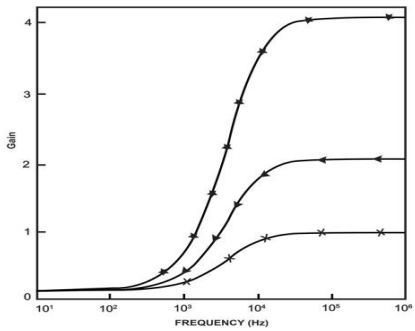
4.2. Voltage-mode filter

An input of 100 mV, 1 kHz is applied to the VM filters For second-order VM HPF, values of the passive component chosen are R_1 = 1.5 kΩ, R_2 =1.5 kΩ, R_3= 1.6 kΩ, and $C_1 = C_2$ = 15.9 nF. HPF, refer to Fig. 9(a), has been designed for a cut-off frequency of 6.676 kHz. In this case, the observed f_o = 6.165 kHz. Figure 9(b) presents the independent gain tuning feature of the HPF using R_3. The frequency response of VM low-pass filter is presented by Figs. 10(a) and (b) depicts the independent gain variation of the filter response, which has been designed for a cut-off frequency of 200 kHz.

For HPF, values of the passive components are $R_1 = R_2 = R_3$=17.68 kΩ and $C_1 = C_2$ = 45 pF. The observed f_o is 148 kHz. Figure 11(a) shows the VM band-pass filter frequency response and Fig. 11(b) presents the independent gain control using R_2. The filter has been designed for a cut-off frequency of 200 kHz. Values chosen for passive components are $R_1 = R_3$ = 17.68 kΩ, R_2 = 8.84 k and $C_1 = C_2$ = 45 pF. The observed f_o is 204.17 kHz. The calculated Q value is 0.5 and the observed Q is 0.51. Hence, the obtained results verify the theory. The DC gain values taken by CM and VM filter responses when R_2 or R_3 is varied, for independent gain control, can be verified from the corresponding calculated values of DC gain, given in Table 3 to 5.

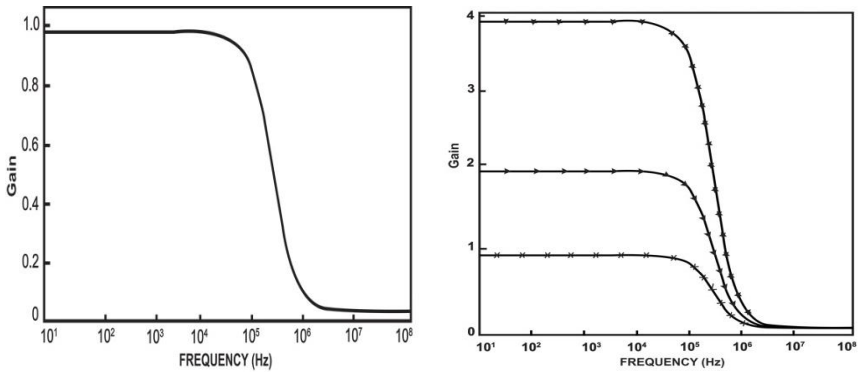


(a) Frequency response of VM second-order HPF.



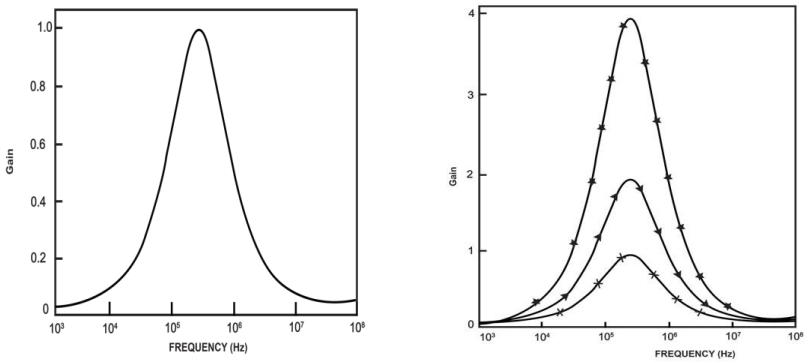
(b) Tuning HPF gain through R_3: x = 1.6 k; ^ = 3.2 k;* = 6.4 k.

Fig. 9. Simulation results of VM second-order HPF.



(a) Frequency response of VM second-order LPF. **(b) Tuning of LPF gain through R_2: x = 17.68 k; ^=8.84 k;* = 42 k.**

Fig. 10. Simulation results of VM second-order LPF.



(a) Frequency response of VM second-order BPF (Q = 0.5). **(b) BPF gain tuning through R_2: x = 8.84 k; ^ = 4.42 k;*=2.21 k.**

Fig. 11. Simulation results of VM second-order BPF (Q = 0.5).

Table 3. Current-mode HPF and LPF gain variation.

Value of R_2 (in Ω)	H_{hp} calculated	H_{lp} calculated
1 k	1.09	4
2 k	2.19	2
4 k	4.39	1

Table 4. Voltage-mode LPF and HPF gain variation.

Value of R_2 (in Ω)	H_{lp} calculated	Value of R_3 (in Ω)	H_{hp} calculated
17.68 k	1	**1.6 k**	1.07
8.84 k	2	**3.2 k**	2.13
4.42 k	4	**6.4 k**	4.26

Table 5. Voltage-mode BPF gain variation with R_2.

Value of R_2 (in Ω)	H_{bp} calculated
8.84 k	1
4.42 k	2
2.21 k	4

5. Conclusions

With the advent of the LV design techniques, there is a complete shift in the focus of analogue designers on building low voltage and ultra-low voltage operable current conveyor based analogue signal processing applications. Keeping the above in view, five different filter configurations have been designed to operate at supply as low as 0.5 V and 0.18 µm CMOS technology. Workability of the proposed filters has been established by PSPICE simulations.

- High-Pass and Low-Pass configurations: In this paper: (1) A first-order current mode HPF with f_o = 11 kHz (2) A voltage-mode second-order HPF filter with f_o = 6.676 Hz (3) A first-order current-mode LPF with f_o = 523 Hz (4) A voltage-mode second-order LPF filter with cut-off frequency of 200 kHz; have been designed and discussed.
- Band-pass configuration: A voltage-mode second-order BPF filter with f_o = 200 kHz and Q =0.5 has also been realized.
- The gain of all filters can be independently tuned without effecting f_o, by adjusting a single passive component value.
- Escalating demand for LV LP LF circuits in the fields like bio-signal processing and bio-electronics, where signals to be dealt is limited in the frequency range (up-to few kHz) and low in amplitude, can be fulfilled by such filters.
- This work is our sincere effort to present the realization of simple first and second-order filter configurations based on bulk-driven second generation Current Conveyor (CC).

Nomenclatures

C	Capacitor
f_o	Cut off, Hz
f_o/ ω_o	Cut off/Central frequency
I_b	Bias current, A
I_i and V_i	Input current or voltage, A and V
I_o and V_o	Output current or voltage, A and V
I_Z/I_X	Current at Z terminal/current at X terminal
Q	Quality factor
R	Resistor, Ω
S	Sensitivity
V_T	Threshold voltage, V
V_X/V_Y	Voltage at X terminal/voltage at Y terminal

Greek Symbols

ω_o	Central frequency, radians

Abbreviations

BPF	Band-Pass Filter
CM	Current Mode
FG-MOS	Floating Gate MOSFET
HPF	High-Pass Filter
LF	Low-Frequency
LP	Low-Power
LPF	Low-Pass Filter
LV/ULV	Low-Voltage/Ultra-Low Voltage
QFG	Quasi-Floating Gate
SISO	Single-Input Single-Output
TSMC	Taiwan Semiconductor Manufacturing Company
VM	Voltage Mode

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