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A SOFT SWITCHED INTERLEAVED HIGH GAIN DC-DC CONVERTER

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Abstract

In this paper, a novel soft-switched interleaved DC-DC converter which provides a high voltage gain of 12 is proposed. Voltage gain of the basic interleaved boost converter is extended by using diode-capacitor multiplier (DCM) cells. The switches are operated at a nominal duty ratio of 0.5. The voltage stress on the power switches and diodes is only a fraction of the output voltage. To enhance the operating power conversion efficiency, the switches are turned ON at zero voltage condition. Experimental results of 18-216V, 100W prototype converter validate the operating principle and the advantageous features of the presented converter.

Keywords: Gain extension, High gain, Interleaved converter, Soft-switching.

1. Introduction

Recently, electrical energy conversion from renewable energy sources (RES) like solar, wind and fuel cells are gaining greater importance. This is mainly due to the stringent pollution norms imposed on coal and oil based power plants and the ease with which RES are connected to the main grid [1- 4]. However, the output voltage levels of these sources are very low. An intermediate level boosting stage is essential to utilise these sources to their maximum extent. Conventional boost converter has its own limitations in providing higher gains due to the reverse recovery problem of output diode at higher duty ratios. To alleviate this difficulty, some boost derived topologies have been developed and presented in [5 - 8].

In order to employ a DC-DC converter for renewable energy application, factors such as efficiency, input and output current ripple, weight, system dynamics, losses, and power handling capability should be considered. Different topologies have been

Nomenclatures

D	Duty ratio
f	Switching frequency, Hz
f_r	Resonant frequency, Hz
N	Number of voltage multiplier cells
V_{C1}	Voltage across capacitor C1 (Fig. 1), volts
V_{C2}	Voltage across capacitor C2 (Fig. 1), volts
V_{C3}	Voltage across capacitor C3 (Fig. 1), volts
V_{C4}	Voltage across capacitor C4 (Fig. 1), volts
V_{C5}	Voltage across capacitor C5 (Fig. 1), volts
V_{D0}	Voltage across output diode D0 (Fig. 1), volts
V_{D1}	Voltage across diode D1 (Fig. 1), volts
V_{D2}	Voltage across diode D2 (Fig. 1), volts
V_{D3}	Voltage across diode D3 (Fig. 1), volts
V_{D4}	Voltage across diode D4 (Fig. 1), volts
V_{D5}	Voltage across diode D5 (Fig. 1), volts
V_{in}	Input voltage, volts
V_o	Output voltage, volts
V_{S_1}	Voltage across switch S_1 (Fig. 1), volts
V_{S_2}	Voltage across switch S_2 (Fig. 1), volts

Abbreviations

DCM	Diode Capacitor Multiplier
PV	Photovoltaic
VMC	Voltage Multiplier Cell
ZVS	Zero Voltage Switching

developed based on coupled inductors, interleaved techniques and other gain extension methods [9 - 19]. These techniques improve the voltage gain and power handling capability of the converters. However, these topologies operate under discontinuous input current condition. This degrades the system performance. At higher switching frequencies, transformer based topologies possess some limitations like cause incremental losses and saturation. In addition, the overall weight and cost of the converter also increases.

Pan et al. [9], presented a transformerless step up converter with limited voltage conversion ratio. Prudente et al. [10] developed a high gain converter based on voltage multiplier cells (VMCs). Though the gain can be increased by increasing the number of such gain extension cells, the component count increases drastically. Rossa et al. [11] and Zhang et al. [12] proposed multilevel DC-DC converters. However, high input current ripple make these converters less attractive, especially for photovoltaic (PV) application. Girish et al. [13], Do et al. [14], Li et al. [15], Hu et al. [16], Sanghyuk.L. et al. [17] and Nouri et al. [18] proposed several interleaved topologies to mitigate input current ripple.

Interleaved converters using VMCs have been proposed by Girish et al. [13], Li et al. [15], Sanghyuk.L. et al. [17] and Nouri et al. [18]. Zhou et al. [19] presented interleaved converter with diode capacitor multiplier (DCM) cells to reduce the component count. Such converters achieve the same gain with half the number of

components used in VMC based topologies. In this converter, the switch voltage stress remains the same as that of conventional interleaved converter. Nevertheless, the hard switching mechanism of the DCM based converter reduces the overall efficiency. Hence, Li et al. [20], Hsiesh et al. [21] and Chuang et al. [22] proposed soft switched high gain topologies.

A soft switched high gain DC-DC converter with reduced input current ripple and switch voltage stress is proposed in this paper. The paper is outlined as follows: in section 2, the operating principle and the characteristic waveforms of the proposed converter is described. Section 3 is used to analyse the converter under steady-state condition and expressions for voltage gain, passive elements, device stresses and resonant elements are derived and presented. The experimental results and discussion is presented in section 4 while conclusion is described in section 5.

2. Circuit Description

The proposed converter has two stages; (i) the interleaved boost stage which is formed by the switches S_1, S_2 along with the inductors L_1 and L_2 and (ii) the diode-capacitor multiplier (DCM) stage. For PV application, the input current ripple must be less. In order to reduce the input current ripple, the two switches operate at a duty ratio of D=0.5 and are phase shifted by 180°. The interleaved boost stage helps in reducing input current ripple and DCM stages is useful in extending the voltage gain of the converter. Diodes D_{s1} and D_{s2} are the intrinsic body diodes of the switches S_1 and S_2 respectively. C_{s1} and C_{s2} are the resonating capacitors added across the switches to achieve zero-voltage switching (ZVS) of the switches. A prototype converter consisting of an interleaved boost stage and 5 DCM cells formed by diode-capacitor pairs D1-C1 to D5-C5 is shown in Fig.1.

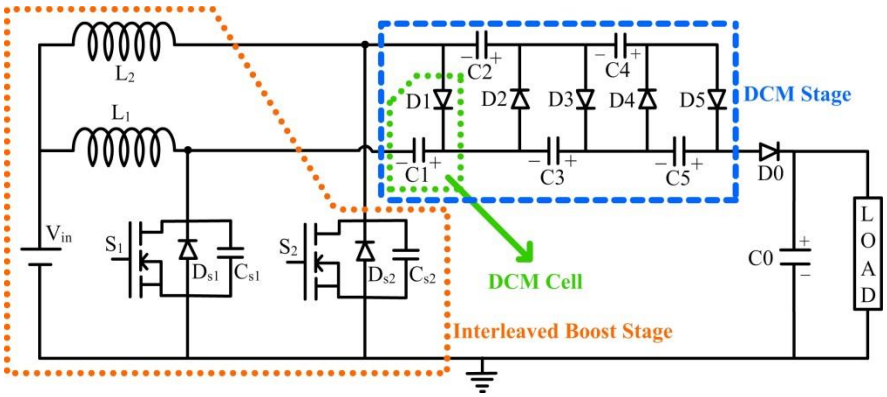


Fig. 1. Power circuit diagram of the proposed converter.

The operating principle of the presented converter can be explained in six operating modes in one switching cycle T_s starting from time t_0 to t_6. Till t_0 switch S_2 remains in ON state. Assuming ideal passive components and diodes, the operating modes can be explained as follows.

Mode 1(t_0-t_1): At time $t=t_0$, gate pulse to switch S_2 is removed and S_2 turns OFF. S_1 remains in OFF state. Capacitor C_{s1} discharges through the inductor L_1. Stored energy in L_2 charges the resonant capacitors C_{s2} Consequently, voltage across C_{s2} increases gradually towards supply voltage V_{in} while C_{s1} gradually discharges to zero.

Mode 2(t_1-t_2): At time $t=t_1$, capacitor C_{s1} is completely discharged. Voltage across C_{s1} is zero and the voltage across S_1 is also zero. Now, the antiparallel diode D_{s1} starts to conduct. This results in a small leakage current through the diode D_{s1}. Since D_{s1} conducts, current through the switch S_1 is slightly negative in this mode. The voltage across S_1 is zero. Gate pulse is applied to S_1 at the end of this mode. By using ZVS technique, switch S_1 is turned ON under zero voltage condition.

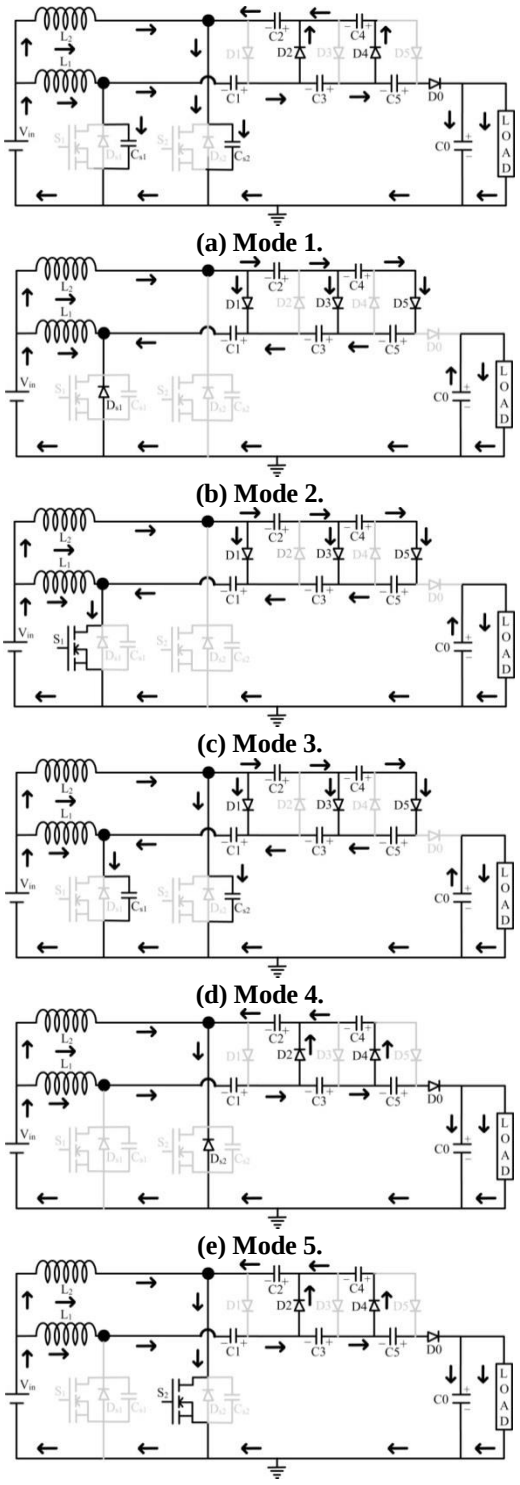
Mode 3(t_2-t_3): Switch S_2 is still in OFF state. Current through inductor L_1 raises linearly towards the maximum value $I_{L_{1,max}}$ whereas decreases linearly towards $I_{L_{1,min}}$. Diodes D1, D3 and D5 are forward biased while D2, D4 and D0 remain reverse biased. A small part of current flows through capacitors C2, C3, C4 and C5. Consequently, C2 and C4 discharges through S_1 and capacitors C3 and C5 charge through diodes D3 and D5 respectively. C1 continues to charge towards a voltage equal to a conventional boost converter due to the remaining part of I_{L1}. The output capacitor C0 discharges through the load.

Mode 4(t_3-t_4): In this mode, S_1 is turned OFF at time $t=t_3$. The resonant capacitor C_{s1} charges towards the supply through L_1. The voltage across C_{s2} decreases towards zero. Other circuit parameters are similar to Mode 3.

Mode 5(t_4-t_5): At time $t=t_4$, C_{s2} is completely discharged. Voltage across C_{s2} and S_2 becomes zero. The antiparallel diode D_{s2} starts to become forward biased. This results in small leakage current through the switch. As D_{s2} is conducting, voltage across S_2 is zero. Switch S_2 is turned ON under zero voltage condition. Thus, ZVS turn-ON is achieved.

Mode 6(t_5-t_6): As S_2 is turned ON, inductor current I_{L_2} raises linearly while I_{L_1} decreases linearly towards their respective maximum and minimum values. A part of I_{L_1} is contributed by the discharging capacitors C1, C3, C5. The remaining part of I_{L_1} flows through diodes D3 and D5, thus charging the capacitors C2, C4 respectively. Output diode D0 conducts and recharges capacitor C0. This mode ends at time $t=t_6$. The next operating cycle commences when gate pulse to S_2 is removed.

The equivalent circuit for all the operating modes and characteristic waveforms are shown in Figs. 2 and 3 respectively.



(a) Mode 1.

(b) Mode 2.

(c) Mode 3.

(d) Mode 4.

(e) Mode 5.

(f) Mode 6.

Fig. 2. Equivalent circuit of the converter during Mode 1 to Mode 6.

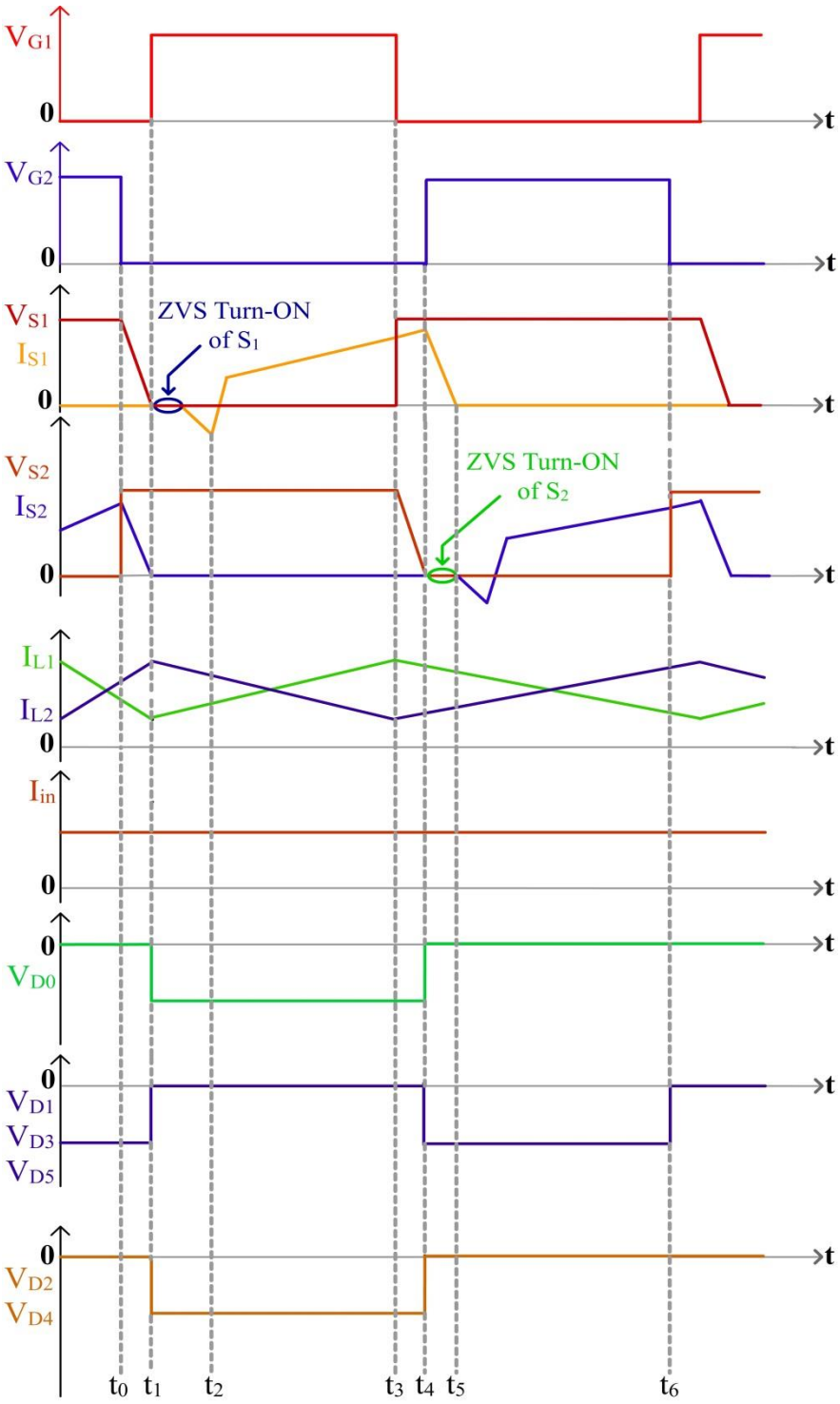


Fig. 3. Characteristic waveforms of the proposed converter.

3. Design Parameters and Characteristic Equations

The converter involves computation of voltage gain, device stresses and determining the value of passive elements. They are obtained as outlined below.

3.1. Voltage gain

Applying volt-second balance on the inductors L_1 and L_2, the governing equations are given by

$$V_{in}D=\left(V_{C1}-V_{C2}+V_{C3}-V_{C4}+V_{C5}-V_{in}\right)\left(1-D\right) \tag{1}$$

$$V_{in}D=\left(V_{C1}-V_{in}\right)\left(1-D\right) \tag{2}$$

$$V_{in}D=\left(V_{C2}+V_{C4}-V_{C1}-V_{C3}-V_{in}\right)\left(1-D\right) \tag{3}$$

$$V_{in}D=\left(V_{0}-V_{C1}-V_{C3}-V_{C5}-V_{in}\right)\left(1-D\right) \tag{4}$$

Solving Eq. (2), the voltage across capacitor C1 is derived as

$$V_{C1}=\frac{V_{in}}{1-D} \tag{5}$$

By rearranging and solving Eq .(1) and (3), the capacitor voltages are obtained as

$$V_{C2}=V_{C3}=V_{C4}=V_{C5}=\frac{2V_{in}}{1-D} \tag{6}$$

By substituting Eq. (5) and (6) in Eq. (4), the overall voltage gain is derived as

$$\text{Voltage gain G=}\frac{V_0}{V_{in}}=\frac{6}{1-D} \tag{7}$$

The voltage gain of the proposed converter depends on the duty ratio D and number of DCM cells that connected. Hence, a generalized expression for voltage gain with 'N' DCM cell can be obtained as,

$$\text{Generalized voltage gain G = }\frac{V_0}{V_{in}}=\frac{1+N}{1-D} \tag{8}$$

3.2. Passive energy storage elements

The interleaved topology is derived from a classical boost converter. Hence, the critical inductance and capacitance values are calculated similar to a conventional boost converter. The expressions for obtaining the values are expressed as

$$L_{critical}=\frac{V_{in}D}{f\Delta i_L}\ \text{and}\ C_{critical}=\frac{I_oD}{f\Delta v_C} \tag{9}$$

where f is switching frequency, Δi_L is the inductor current ripple and Δv_C is the voltage ripple across the capacitor. The input current ripple must be very low so

as to suit PV application. Hence, the inductor value is obtained by considering 10% input current ripple. The output capacitor value is designed such that the voltage ripple at the output must be less than 5% of the total voltage output.

3.3. Resonant capacitors C_{s1} and C_{s2}

Soft switching of S_1 and S_2 is achieved by allowing the inductors L_1 and L_2 to resonate with C_{s1} and C_{s2}. The resonant frequency f_r is expressed as

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{10}$$

By considering the switching frequency to be lesser that the resonant frequency ($f < f_r$), the values of L_r and C_r to obtain ZVS condition can be found out.

3.4. Voltage stress on the switches and diodes

The classical interleaved boost converter stage is formed by the switches S_1 and S_2. The gain extension happens through the DCM stage. Therefore, the voltage stress on S_1 and S_2 with 'N' DCM cells is expressed as

$$V_{S_1} = V_{S_2} = \frac{V_{in}}{1-D} = \frac{V_0}{1+N} \tag{11}$$

The diodes present in the DCM stage experience a voltage stress equivalent to the sum of the voltage from a classical boost converter and the input to the DCM network. Therefore, the voltage stress across D1 to D5 is expressed as

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = \frac{2V_{in}}{1-D} \tag{12}$$

The output diode D_0 in this converter will be subjected to a voltage stress given by

$$V_{D0} = V_0 - \frac{5V_{in}}{1-D} = \frac{V_{in}}{1-D} \tag{13}$$

4. Experimental results

To demonstrate the practical feasibility, a hardware prototype of the proposed converter was built and tested. The hardware specifications are given Table 1 and photograph of the laboratory prototype is shown in Fig. 4. Figure 5 shows the waveforms pertaining to gate pulses, input and output voltages obtained from the experimented converter. The gate pulses are properly phase shifted with a duty ratio of *D=0.5* and at 50 kHz frequency.

For an input voltage of 18V, an output voltage of 216V was obtained at a nominal duty ratio *D=0.5*. This proves the high gain capability of the power converter. Further, the output voltage ripple is less than the 5% voltage ripple norms which was considered during the design stage. Figure 6 shows the input voltage V_{in},

input current I_{in}, output voltage V_0 and output current I_0. The voltage conversion ratio and the power handling ability of the converter have been proved.

The gate pulses and current through the inductors are shown in Fig. 7. Since the proposed converter was designed to suit PV application, the input current ripple was chosen as 10%. The switches present in the interleaving stage operate at a duty ratio of 0.5 with 180° phase-shift between them. The inductor currents are equal in magnitude and out of phase with each other. Therefore, the current ripple at the input is as low as 8% of the total current.

Table 1. Specifications of the prototype converter.

Parameters	Value
Input voltage (V_{in})	18V
Output voltage (V_0)	216V
Output power (P_0)	100W
Switching frequency (f)	50kHz
Resonant frequency (f_r)	146kHz
Duty ratio (D)	0.5
Switches (S_1, S_2)	FDPF33N25T (250V, 33A, 94 mΩ)
Diodes (D0-D5)	MUR1660 (600V, 16A, 1.7V)
Inductors (L_1, L_2)	230μH, 5A
Capacitors (C1-C5)	10μF/250V, electrolytic
Output capacitor (C0)	47μF/500V, electrolytic
Resonant capacitors (C_{s1}, C_{s2})	47nF/600V, polyester

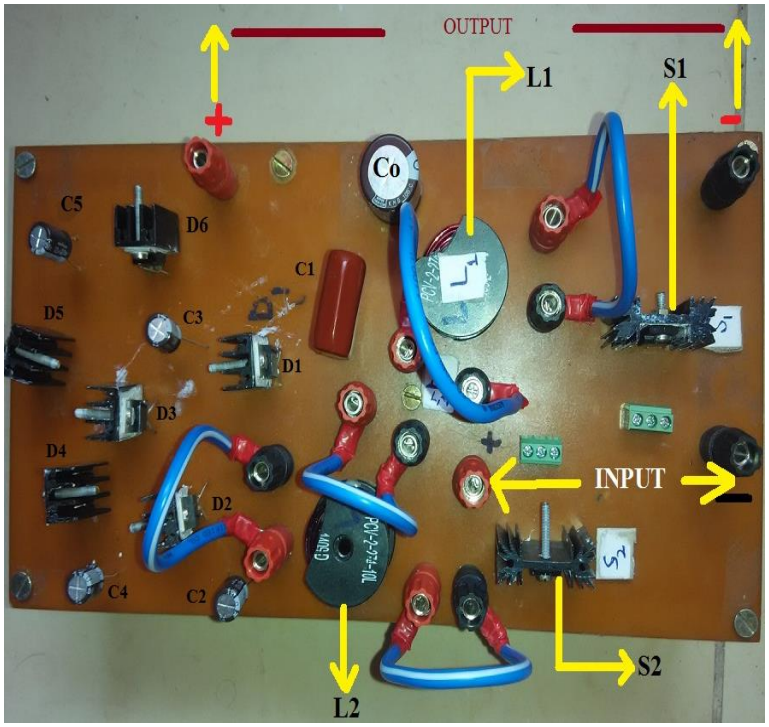


Fig. 4. Hardware prototype of the proposed converter with 3 DCM cells.

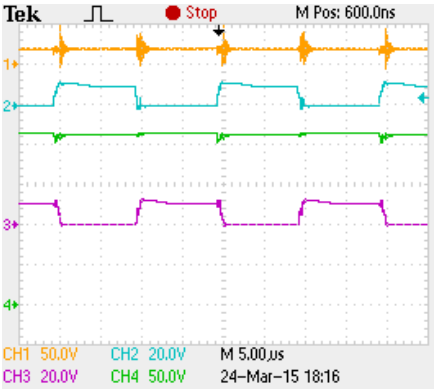


Fig. 5. Waveforms depicting input voltage, gate pulses of S_1, S_2 and output voltage. (CH1: V_{in}, CH2: V_{GS1}, CH3: V_{GS2}, CH4: V_o).

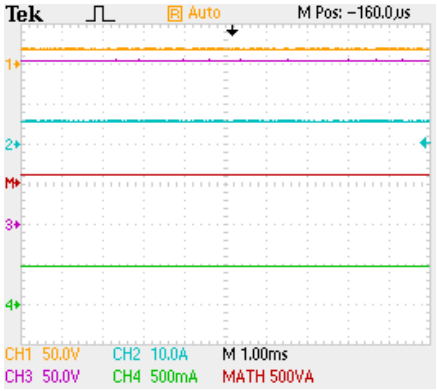


Fig. 6. Voltage and current waveforms obtained at the input and output sides. (CH1: V_{in}, CH2: I_{in}, CH3: V_o, CH4: I_o).

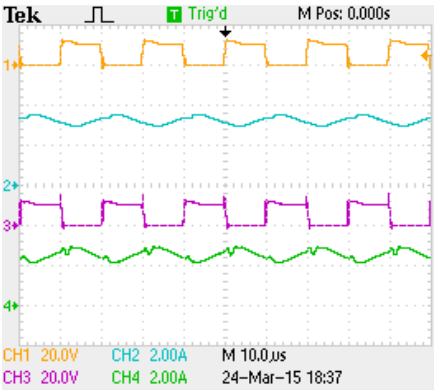


Fig. 7. Gate pulses and inductor current waveforms. (CH1: V_{GS1}, CH2: I_{L1}, CH3: V_{GS2}, CH4: I_{L2}).

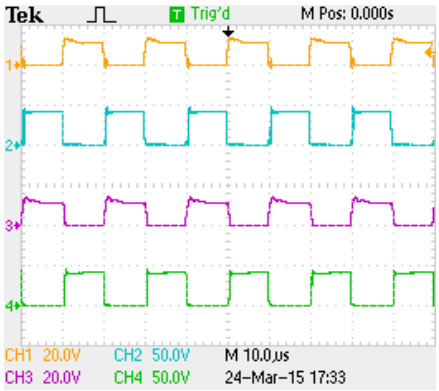


Fig. 8. Practical waveforms depicting the gate pulses and voltge stress on the switches. (CH1: V_{GS1}, CH2: V_{DS1}, CH3: V_{GS2}, CH4: V_{DS2}).

Figure 8 shows the gate pulses applied to S_1 and S_2 and the corresponding voltage stresses across the S_1 and S_2. The switches turn ON and turn OFF at the desired instants. Further, the voltage stress across the switches during the OFF period is close to $\frac{1}{6}V_0$ as predicted in Eq.(11). This reduced voltage stress across the switches is because of the gain extension occurring in the DCM stages. As the voltage stress on devices is very less compared to output voltage, switches with low voltage rating can be used to reduce the losses. The voltage across and current through the switches S_1 and S_2 are shown in Fig. 9. The complementary nature of voltage and current is observed. Further, due to interleaving, the total input current is equally shared by the switches. The slight deviation in current

sharing is due to the implicit mismatch in the inductors and the diodes present in DCM stages. The voltage across diodes D2-D5 is shown in Fig. 10. The diode pair D2, D4 operate complimentary to the other diode pair D3, D5 while charging and discharging the capacitors in the DCM network. Further, the voltage stresses across all the diodes D2-D5 is equal to the sum of voltage of a boost converter stage and one DCM cell. The diode voltage stress agrees with the expression derived in Eq. (12).

Figure 11 shows the voltage across capacitors C1-C4. Since capacitor C1 is present at the input of the DCM stage, the voltage across C1 is same as the output obtained from a conventional boost converter. Other capacitors (C2-C4) will charge to a voltage which will be the sum of the boost converter and the DCM cell. The practical values of capacitor voltages obtained from the prototype converter prove the design methodology adopted and the proper operating principle of the converter with the DCM stage.

Switches S_1 and S_2 are turned ON under ZVS condition. This is clearly depicted in Figure 12. Since resonant capacitors (C_{s1} and C_{s2}), resonate with the main inductors, the voltage across the switch falls to zero completely. After a small delay caused by the resonant tank elements, the current through that particular switch increases. During this switching transition, the power loss occurring across the switches is brought down to zero. As a result, the overall efficiency of the converter is improved. Figure 13 shows the waveforms pertaining to input and output parameters which are used to compute efficiency. The efficiency attained for the soft switched converter is about 96% under full load condition. To appreciate and quantify the efficiency enhancement obtained by employing soft-switching, the hard-switched converter was operated under full load condition. Figure 14 shows the waveforms obtained from the hard-switched prototype converter. The computed efficiency was about 93% at full load condition for the hard-switched converter. The 3% increment in efficiency is due to soft-switching technique. Figure 15 shows the efficiency curves of the hard and soft switched converter.

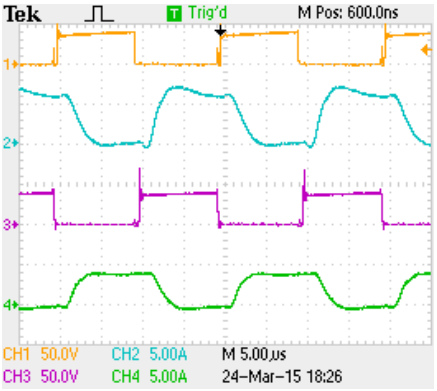


Fig. 9. Practical waveforms depicting the switch voltage and current. (CH1: V_{S1}, CH2: I_{S1}, CH3: V_{S2}, CH4: I_{S2}).

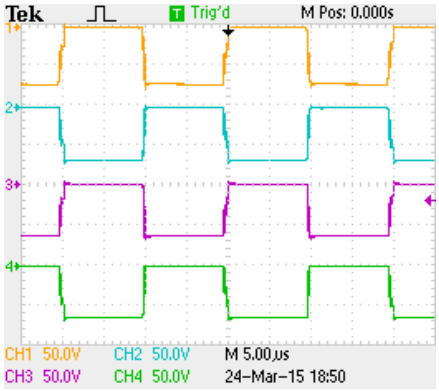


Fig. 10. Waveforms showing the voltage stress experienced by diodes D2-D5. (CH1: V_{D2}, CH2: V_{D3}, CH3: V_{D4}, CH4: V_{D5}).

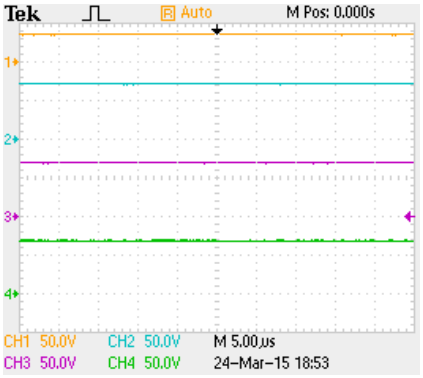


Fig. 11. Waveforms for voltage across capacitors C1-C4. (CH1: V_{C1}, CH2: V_{C2}, CH3: V_{C3}, CH4: V_{C4}).

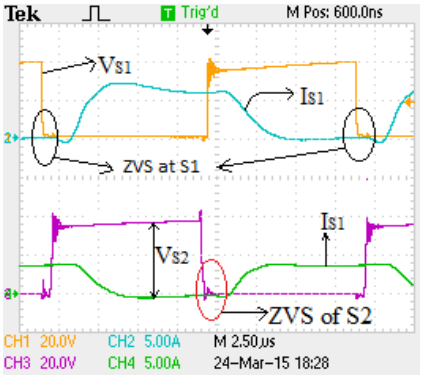


Fig. 12. Practical waveforms showing the soft-switching (ZVS turn-ON) of S_1 and S_2. (CH1: V_{S1}, CH2: I_{S1}, CH3: V_{S2}, CH4: I_{S2})

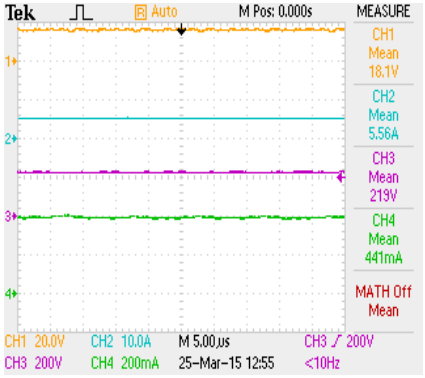


Fig. 13. Waveforms showing input and output parameters to compute efficiency under soft switching. (CH1: V_{in}, CH2: I_{in}, CH3: V_0, CH4: I_0)

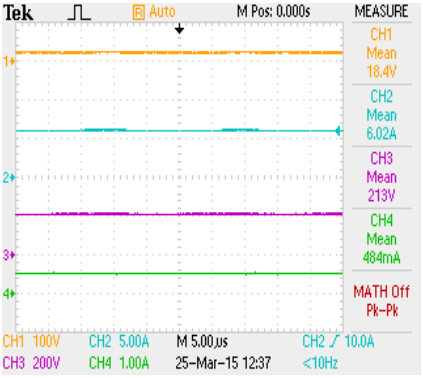


Fig. 14. Waveforms showing input and output parameters to compute efficiency under hard switching. (CH1: V_{in}, CH2: I_{in}, CH3: V_0, CH4: I_0)

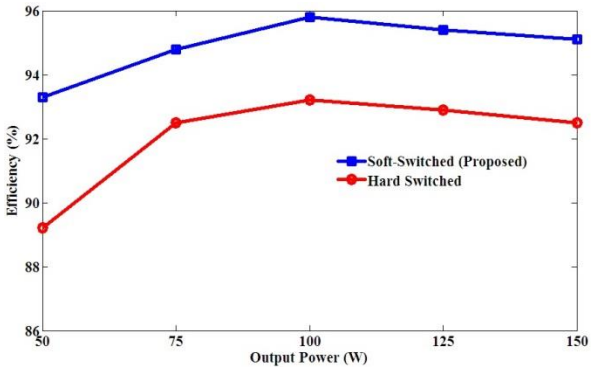


Fig. 15. Power versus efficiency curve of the proposed converter under hard and soft switched conditions.

5. Conclusion

A soft-switched high gain interleaved DC-DC converter was proposed and demonstrated practically. The converter used 5 diode capacitor multiplier cells and the switches were operated at a nominal duty ratio of 0.5. Under these conditions, a voltage conversion ratio of 12 was obtained from the 18V-216V, 100W prototype converter. The input current was continuous. The ripples at the input current were reduced by employing interleaving technique. Since gain extension was obtained through the DCM stages, the switches and diodes were subjected to a very low voltage stress which was only a fraction of output voltage. This permits the use of semiconductor devices with very low voltage rating and ON state voltage drop, thereby aiding to improve the operating efficiency. By employing ZVS turn-ON, the power conversion efficiency of the topology was about 96% under full load condition. The desirable features like high gain, higher efficiency, reduced input current ripple, reduced switch and diode voltage stresses and modularity make this converter an appropriate choice for PV applications.

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