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EXPERIMENTAL AND SIMULATION ANALYSIS OF BREAK-LOCK IN PHASE LOCKED LOOP SYNTHESIZER FOR FREQUENCY TRACKING APPLICATIONS

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Abstract

Modern missile seekers invariably employ monopulse radar with phase locked loop (PLL) as a frequency (angle) tracking subsystem in the receiver. The frequency locking and/or unlocking of these receivers can be achieved either by introducing imperfections in the monopulse design or using multiple repeater sources. In the present paper, the break-lock of PLL synthesizer in the monopulse radar receiver is presented. The linear frequency modulated (LFM) signal has been used as a repeater interference signal, which is injected into the PLL along with radar echo signal. The frequency deviation as a function of LFM signal power required to break-lock is presented for different values of modulation rate and echo signal power. The simulation results show that break-lock is achieved at frequency deviation of 0.36 MHz (0.35 MHz measured value) for a typical jammer power of -14 dBm and modulation rate of 200 kHz with radar echo signal power of -14 dBm at the PLL input. The measured results show that at a typical jammer power of -14 dBm, break-lock is achieved at frequency deviations of 0.35 and 0.9 MHz for modulation rates of 200 and 500 kHz respectively, revealing that at lower values of modulation rate, break-lock is achieved at lower values of frequency deviation. The computer simulation is carried out for performance prediction and experimental measurement results are presented in support of the simulated results. With fairly good and consistent agreement between the measured and simulated results, the PLL is well suited to be integrated within monopulse radar receivers for LFM jamming.

Keywords: Break-lock, Jamming, Linear frequency modulation, Phase locked loop, Tracking radar.

Nomenclatures

C_{tot}	Total capacitance, pF
f_0	Initial frequency, MHz
f_c	Loop bandwidth, kHz
f_{frac}	Fractional mode frequency, MHz
f_{int}	Integer mode frequency, MHz
f_{vco}	VCO frequency, GHz
f_{XTAL}	Reference oscillator frequency, MHz
k	Chirp rate, per sec
K_ϕ	Phase detector gain, mA
K_{vco}	VCO gain, MHz/Volt
N	Division ratio
N_{frac}	Fractional division ratio
N_{int}	Integer division ratio
ϕ	Phase margin, degree
R	Reference path division ratio
T_1	Time constant
T_2	Time constant
T_3	Time constant
T_{31}	Pole ratio

Abbreviations

AWR	Advancing wireless revolution
ESD	Electro static discharge
HMC	Hittite microwave corporation
MMIC	Monolithic microwave integrated circuit
PLL	Phase locked loop
VCO	Voltage controlled oscillator
VSS	Visual system simulator
XREF	Reference oscillator path

1. Introduction

Monopulse is a radar technique used to locate the angular direction of the target by receiving the echo signal using two or more antenna feeds. This monopulse technique has become the most successful tracking schemes in modern missile seeking applications. For effective jamming of these missile radars employing monopulse techniques, it is essential that the tracking of the radar should be broken either by introducing imperfections in the monopulse design or using multiple repeater sources in order to distort the angle of arrival of the echo signal at the monopulse antenna. As a result the monopulse tracker is caused to move away from the target and thus results in break-lock in the missile seeker [1].

The modern monopulse radar receivers invariably employ phase locked loop (PLL) as a frequency tracking subsystem [2]. When the reference input and repeater jamming signals are simultaneously applied into PLL, initially, the PLL locks onto the signal frequency whichever is stronger. When the strength of the weak signal is increased and it exceeds the strength of the stronger signal, the PLL loses the frequency lock from the initially locked signal [3], which depends

upon the amplitude ratio (J/S) and frequency separation between these two signals. This results in break-lock in the PLL. Several studies have been made earlier on break-lock of the PLL in monopulse receiver in the presence of interference signal [4 - 9]. The classical monopulse estimator is reviewed and the general monopulse formula based on maximum like hood estimation has been derived in [4]. The design of a prototype fractional-N PLL synthesizer that generates a linear FM signal for a 24 GHz FMCW radar system suitable for velocity and range measurement is presented in [5]. An X-band CMOS single chip transceiver [6] is implemented by meandered complementary conducting strip transmission lines for frequency modulation continuous wave (FMCW) radar application, while the design of a 77 GHz FMCW radar transceiver CMOS IC with a PLL synthesizer based FMCW generator is realized in [7].The possible architecture for real time angle estimation and statistical performance of a random-noise monopulse system is examined in [8]. The LFM signal has been considered [9] as a noise radar waveform for resolving the targets in range and Doppler domains in the presence of channel noise and radar side lobes.

In the present paper, PLL modeling and design, and simulations have been carried out using visual system simulator (VSS) AWR software for frequency deviation measurements through frequency spectrum analysis. The PLL has been realized using HMC703LP4E, an 8 GHz fractional-N PLL synthesizer, which is integrated with external loop filter and HMC508LP5 voltage control oscillator (VCO). Performance parameter, e.g., frequency deviation measurement has been carried out using Agilent Technologies (E8257D) signal generator in a laboratory environment. The frequency spectrum of the PLL is measured using Rhode and Schwarz signal source analyzer (20-50 GHz).

2. System Characterization and Modeling

2.1. Characteristics of PLL synthesizer

The PLL as a synthesizer multiplies a low frequency reference source up to a higher frequency. The phase detector (PD) and charge-pump (CP) drive the tuning signal of the VCO, such that the phase of the two signals at the phase detector input (reference and divider output) become equal. This results in equal frequency of the phase detector input. Since the divider output frequency is equal to the VCO frequency divided by the division ratio (N), this means the control loop forces the frequency of the VCO output to lock on to a frequency equal to N times the reference frequency [10].

Two different types of PLLs are in use for frequency synthesis such as integer and fractional PLL. Mainly, in integer synthesizers, N can only take on discrete values. The frequency steps achieved using an integer-N PLL is too large to make the output continuous and linearly varying function of time. It is therefore common to use a fractional - N PLL for frequency synthesis in which the divider value is changed rapidly between integers by means of delta-sigma modulator [11]. To overcome these limitations, the fractional frequency synthesizer has been integrated in the monopulse receiver. In fractional synthesizers, the division ratio can also take on fractional value. In addition, the fractional divider normally permits higher phase-detector frequencies for a given output frequency with associated improvements in signal quality (phase-noise). HMC703LP4E

frequency synthesizer operating in exact frequency mode with 24 bit fractional modulator and generating fractional frequencies with zero frequency error is modelled and measurements are performed for performance prediction.

2.2. HMC703LP4E fractional-N PLL synthesizer

The HMC703LP4E fractional synthesizer is built upon the high performance PLL platform. The key features include frequency sweep and modulation, external triggering, double buffering, exact frequency control and phase modulation. The functional block diagram of HMC703LP4E synthesizer is shown in Fig.1.

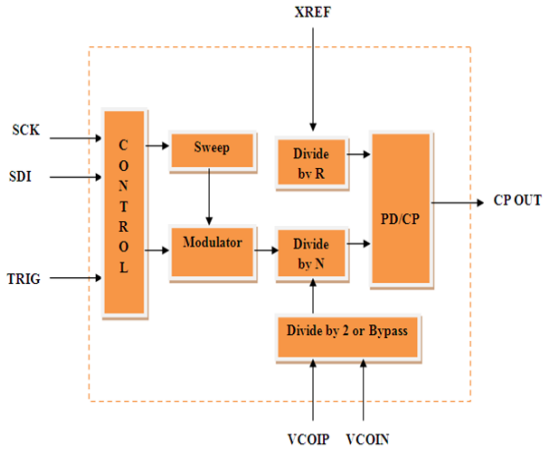

Fig. 1. Functional block diagram of HMC703LP4E.

With reference to Fig.1, the reference buffer provides the path from an external reference source (generally crystal based) to the *R* divider, and also to the phase detector. At high frequency (typically below 350 MHz), the buffer offers high gain and is internally DC biased with 100 Ω internal termination which is then given to the XREF input of the PLL. The reference path *R* divider is based on a 14 bit counter and can divide input signals up to 350 MHz by values from 1 to 16,383. The RF path features a low noise 8 GHz RF input buffer followed by an 8 GHz RF divide-by-2 with a selectable bypass. If the VCO input is below 4 GHz, the RF divide-by-2 is bypassed for improved performance in fractional mode. The RF divide-by-2 is followed by the *N* divider, a 16 bit divider that can operate in either integer or fractional mode up to 4 GHz inputs. Finally, the *N* divider is followed by the phase detector (PD), which has two inputs, the RF path from the VCO and the reference path from the crystal. The PD is recommended to operate at 100 MHz speed in fractional Mode B. The PD is realized using charge pump type rather than a classical voltage PD. The charge pump produces a current by comparing the reference input and the VCO output phase. The PD output current is proportional to the difference in phase between the two signals. The RF input stage provides the path from the external VCO to the phase detector via the RF or *N*-divider which is implemented using a differential common emitter stage with internal DC bias and is protected by ESD diodes. The input frequency at the RF input path is rated up to 8 GHz. The external signal is applied at either VCOIP or VCOIN inputs with the other input connected to ground

through a DC blocking capacitor. The preferred input level for best spectral performance is -10 dBm nominally. The main RF path *N*-divider is capable of divide ratios between 2^{16} - 1 (524,287) and 16. When operating in fractional mode, the *N* divider can change by up to +/- 4 from the average value. Hence, the selected divide ratio in fractional mode is restricted to values between 2^{16}-5 (65,531) and 20. The delta and sigma modulator provides the controlled voltage at the VCO input to tune its frequency equal to the reference input signal. In fractional mode, the frequency of a locked VCO (f_{vco}) controlled by the HMC703LP4E is given by:

$$f_{vco} = f_{\text{int}} + f_{frac} = \frac{f_{XTAL}}{R}(N_{\text{int}} + N_{frac}) \tag{1}$$

where, f_{int} and f_{frac} are the integer and fractional mode frequency, N_{int} is the integer division ratio, N_{frac} is the fractional part, R is the reference path division ratio, f_{XTAL} is the frequency of the reference oscillator. The performance characteristics of HMC703LP4E fractional-*N* PLL is given in Table 1.

Table 1. HMC704LP4E characteristics.

Parameters	Min - Max	Units
RF input frequency	DC - 8	GHz
Power range	-15 - -3	dBm
Reference input frequency	50 - 350	MHz
CP output current	0.02 - 3.5	mA
Phase noise	-112	dBc/Hz
Figure of merit	-228 - -225	dBc/Hz

2.3. Loop filter

The loop filter is a crucial element in the PLL, which determines the bandwidth and dynamic performance of the receiver. A third order passive loop filter is modelled and designed for the simulation because this filter is generally recommended for most of RF applications and it is rare that a PLL is constructed with a filter higher than third order. In addition, the passive loop filter has the advantage over active filter that there is no active device to add noise into the PLL. The loop filter is designed using exact method and this method of filter design involves with solving the time constants of the PLL and then determining the loop filter components from these time constants [12]. The different key parameters chosen in the design of the loop filter are phase margin (ϕ), loop bandwidth (f_c), phase detector gain (K_Φ in mA), voltage controlled oscillator gain (K_{vco} in MHz/volt) and pole ratio. The phase margin is typically chosen between 48 and 50 degrees, which is related to the loop stability. The loop bandwidth is determined at a frequency where the maximum rate of change of phase margin is zero. The selection of pole ratio has an impact on reference spur in the loop. The time constants of filter are determined from phase margins of the forward loop gain [G(s)] given as:

$$\phi = \pi + \tan^{-1}(\omega T_2) - \tan^{-1}(\omega T_1) - \tan^{-1}(\omega T_1 T_{31}) \tag{2}$$

where, T_1 and T_2 are the filter time constants and T_{31} is the pole ratio. The loop gain G(s) is given by:

$$G(s) = \frac{K\phi\, Kvco}{s} Z(s) \tag{3}$$

where, Z(s) is loop impedance, K_{Φ} is phase detector gain and K_{vco} is gain of VCO.

Since the value of phase margin and the pole ratio are known, so an equation containing T_1 and T_2 can be obtained from Eq. (2). So, another equation of T_1 and T_2 can be obtained by finding the maximum value of phase margin at loop bandwidth. It is seen that the loop maximizes the phase margin at a frequency equal to loop bandwidth. So, we can write

$$\left.\frac{d\phi}{d\omega}\right|_{\omega=\omega_C} = 0 \tag{4}$$

Solving Eq. (4), we can express

$$\frac{\omega_c T_2}{1+\left(\omega_c T_2\right)^2} = \frac{\omega_c T_1}{1+\left(\omega_c T_1\right)^2} + \frac{\omega_c T_3}{1+\left(\omega_c T_3\right)^2} \tag{5}$$

Now solving Eq. (2) and (5) sfor two unknowns, the time constants T_1 and T_2 can be determined. The time constant T_3 can be obtained by using the relation

$$T3 = T1T31 \tag{6}$$

To find the values of filter components from these time constants, let's define the constants K_1, K_2, K_3 and K_4 as:

$$K1 = C_{tot} \tag{7}$$

$$K2 = \left(T1 + T3\right)K1 \tag{8}$$

$$K3 = \frac{T1T3K1}{T2} \tag{9}$$

$$K4 = \frac{C3}{C1} \tag{10}$$

Since, C_{tot} is the total loop filter capacitance and equal to C_1+C_2+C_3, hence Eq. (7) can be written as

$$K1 = C1 + C2 + C3 \tag{11}$$

The time constants of the loop filter are defined as

$$T1 + T3 = \frac{C2C3R2 + C1C2R2 + C1C3R3 + C2C3R3}{C1 + C2 + C3} \tag{12}$$

and

$$\frac{T1T3}{T2} = \frac{C1C3R3}{C1 + C2 + C3} \tag{13}$$

Substituting the value of T_1+T_3 from Eq. (12) into Eq. (8), K_2 can be written as

$$K2 = C_2C_3R_2 + C_1C_2R_2 + C_1C_3R_3 + C_2C_3R_3 \quad (14)$$

Now, substituting the value of T_1T_3/T_2 from Eq. (13) into Eq. (9), K_3 can be written as

$$K3 = C_1C_3R_3 \quad (15)$$

Therefore, by solving K_1, K_2, K_3 and K_4, the value of filter components R_1, R_2, C_1, C_2 and C_3 are determined. The typical parameters chosen for the design of the loop filter are presented in Table 2. The loop filter is designed using Hittite Microwave PLL Design and Analysis software Tool and filter components obtained are shown in Fig. 2.

Table 2. Design parameters.

Parameters	Typical values	Units
Reference input frequency	50	MHz
VCO output frequency	4	GHz
Phase detector gain	2.5	mA
VCO gain	40	MHz/volt
Bandwidth	200	kHz
Phase margin	55	Degree

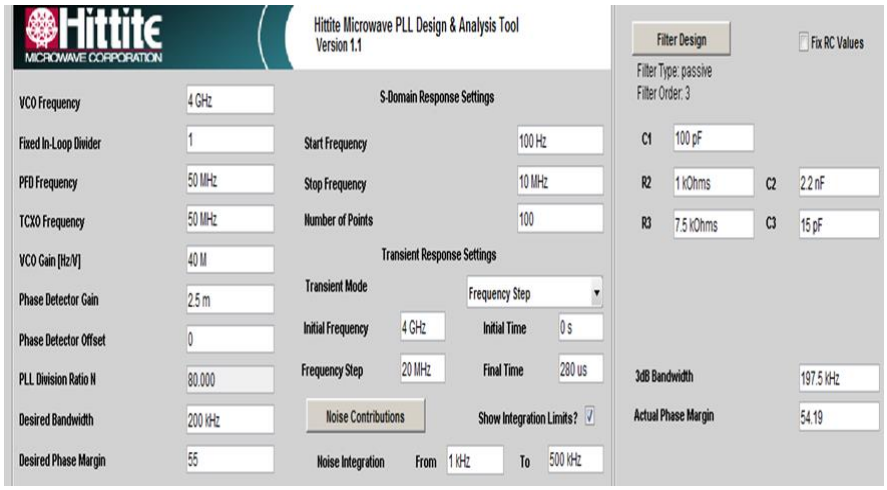

Fig. 2. Design window.

2.4. HMC508LP5 VCO

The HMC508LP5 is an MMIC VCO with integrated resonators, negative resistance devices, varactor diodes, and buffer amplifiers, which operates over the frequency range from 7.8 to 8.7 GHz in response to tuning voltage range of 1 to 11 volt. The VCO has excellent phase noise performance typically -103 dBc/Hz @ 100 kHz offset frequency. The Power output is typically +14 dBm from a single supply of +3.0 V @ 77 mA.

2.5. LFM signal generation

It is important to generate linear FM signals with high linearity ramp. There are several methods employed to synthesize linear FM signal. The simplest approach is to apply a linear ramp voltage to the tuning node of a VCO [13, 14]. It is, however, very difficult to design and fabricate that has a linear tuning curve, especially for wideband requirement. Here, we synthesize linear FM signal through an FM modulator scheme which translate a baseband signal to 4.5 - 8 MHz linear FM signal. The simplified signal generation scheme is shown in Fig. 3.

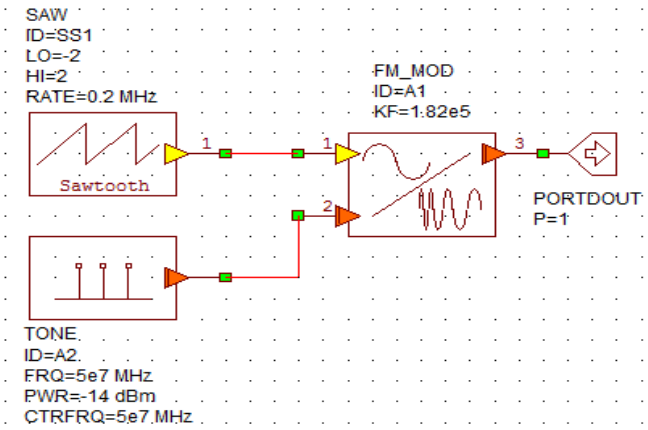

Fig. 3. LFM signal generation.

The linear FM signal can be obtained if the instantaneous frequency of a classical sinusoid signal varies linearly with time, which is achieved by making the phase of the signal quadratic. The instantaneous frequency of LFM signal is given by

$$f(t) = f_0 + \frac{k}{2\pi} t \tag{16}$$

The LFM signal whose frequency varies linearly with time is given by

$$x(t) = A\cos(2\pi f_0 t + \frac{k}{2\pi} t^2) \tag{17}$$

where, f_0 is initial frequency, k is chirp rate. As shown in Fig. 3, the LFM generator includes a CW carrier, a saw tooth wave generator, and an FM modulator. The linear FM jamming signal is generated by frequency modulating the sinusoidal CW carrier with a center frequency of 50 MHz by a baseband saw tooth modulating signal (2 V peak, 200 kHz) using an FM modulator. The FM modulator block frequency modulates the sinusoidal carrier signal by the modulating signal and produces a baseband FM signal. Table 3 summarizes the characteristics of LFM signal.

The frequency spectrum of the LFM shows that the bandwidth of the signal is about 6 MHz centered at 50 MHz. The bandwidth of the signal mainly depends on the modulating signal amplitude and frequency sensitivity of the FM modulator.

Table 3. LFM signal Parameters.

Parameters	Typical values	Units
Modulating signal	2	volt
Modulation frequency	200 - 500	kHz
Carrier center frequency	50	MHz
Carrier signal power	-14 - -2	dBm

The modulating signal and LFM signal spectrum are shown in Figs. 4(a) and (b).

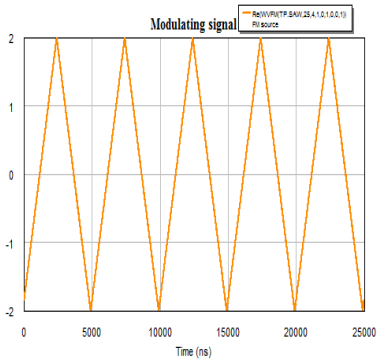

Fig. 4 (a) Modulating signal.

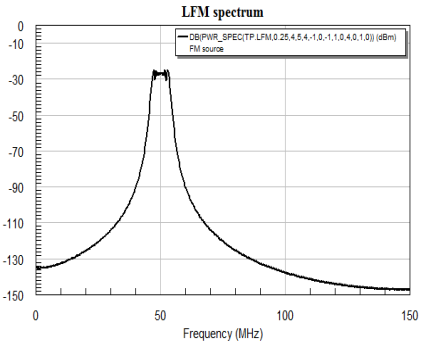

Fig. 4 (b) LFM signal spectrum.

3. Measurements

The photograph of hardware realized using a HMC703LP4E fractional PLL synthesizer is shown in Fig. 5 and complete measurement setup in the laboratory environment is shown in Fig. 6. The radar echo is generated using Agilent Technologies (E8257D) signal generator. Anristu RF/Microwave signal generator (MG3690C) is used to generate LFM signal. These two signals are combined using an L-band RF combiner and then applied into the PLL. The PLL output is connected to the Rhode and Schwarz signal source analyzer (20-50 GHz) and frequency spectrum is measured. Initially, it is observed that the PLL spectrum is centered at 5 GHz reference frequency (-2.43 dBm power) demonstrating that the PLL is locked onto the echo signal frequency (Fig. 7). When the frequency deviation is increased, the PLL spectrum is observed to be widened (Fig. 8) Revealing that the PLL is unlocked from the echo signal frequency. The PLL spectrum at break-lock is depicted in Fig. 9. The frequency deviation is measured as indicated by Anristu RF/Microwave LFM signal generator. The above measurement is performed for a typical modulation rate of 200 kHz with LFM signal and radar echo signal powers of -14 dBm each. The measurements are also performed for selected jammer power in the range from -14 and -2 dBm and different modulation rates of 300, 400, 500 kHz with the echo power of -10 dBm at the PLL input. These measurements are carried out at output frequency of 5 GHz and 0 dBm output power. The resolution and video bandwidth in locked condition and break-lock conditions are selected to be 2 MHz and 5 MHz, respectively.

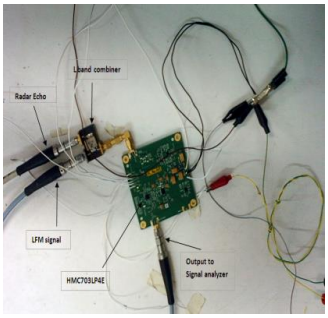

Fig. 5. HMC703LP4E PLL.

Fig. 6. Measurement setup.

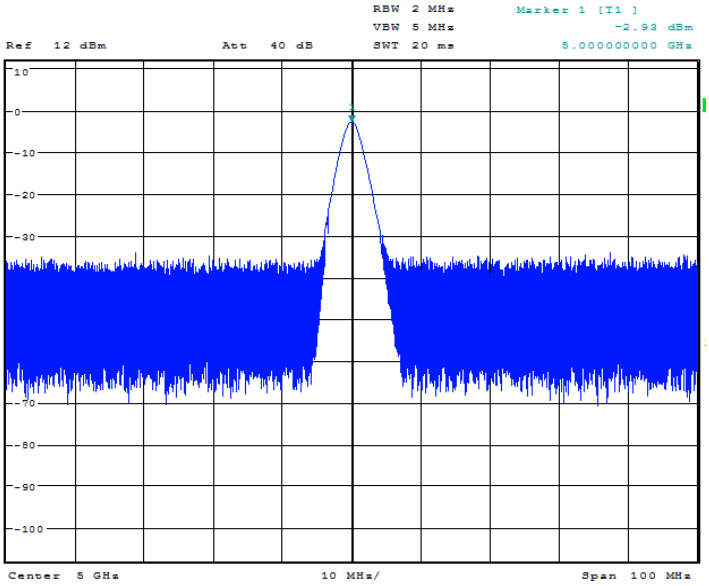

Fig. 7. PLL spectrum in locked condition.

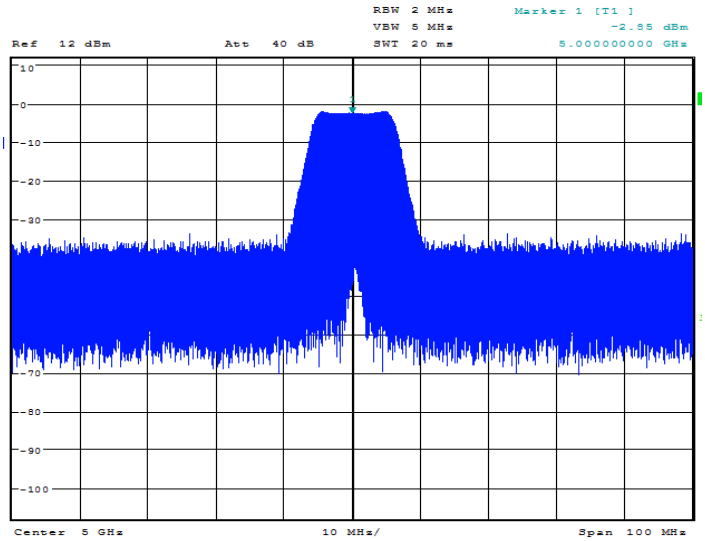

Fig. 8. PLL spectrum while unlocking.

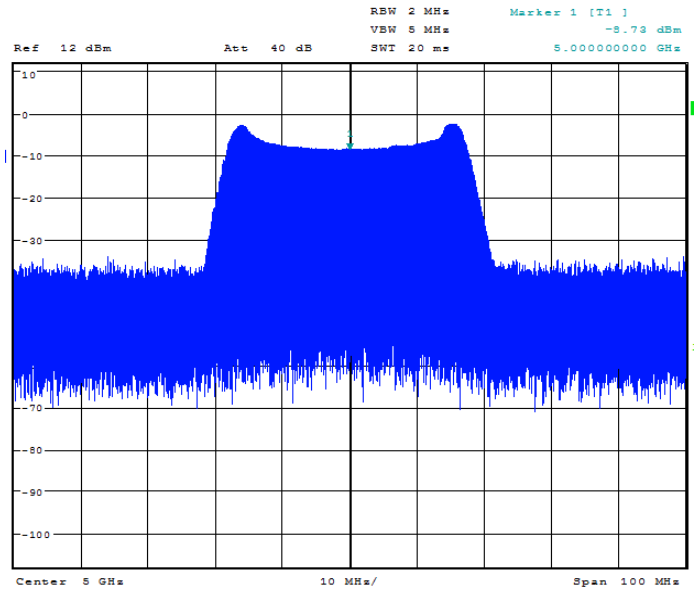

Fig. 9. PLL spectrum in break-lock.

4. Computer Simulation

The computer simulation is carried out to verify the measured results presented in section 3. The PLL is designed with the same specifications used for experimental measurements and is implemented using the VSS simulator as shown in Fig. 10.

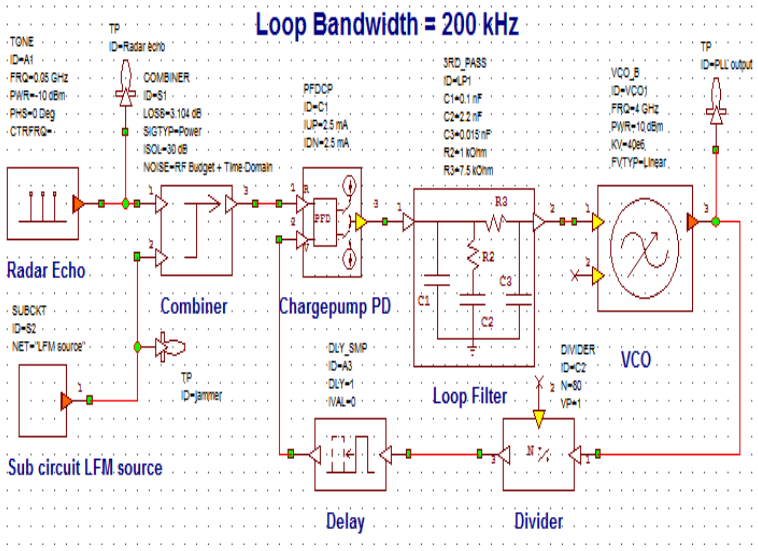

Fig. 10. Phase locked loop.

With reference to Fig.10, the radar echo signal typically operating at an IF frequency of 50 MHz with -14 dBm power and the LFM jamming signal centered at an IF frequency of 50 MHz with -14 dBm power are applied at the PLL input

simultaneously. The reason for selecting the center frequency of LFM signal same as the IF frequency of the radar echo signal is that the radar response to the jamming signal will be maximized if the jamming signal is closely replica of radar waveform. Further, any deviation either in the envelope or phase (frequency) of jamming signal with respect to radar echo signal causes mismatch loss, which must be compensated by additional jammer power. Initially, it is observed that the PLL is locked onto the radar echo signal frequency (4 GHz typical VCO output frequency). The frequency deviation is increased in steps of 0.001 MHz and break-lock is observed. The typical simulation results of the PLL at break-lock are shown in Figs. 11(a) and (b). The results are presented for the modulation rate of 200 kHz with the echo power of -14 and -10 dBm at the PLL input.

It is noted from Fig. 11(a) that the radar echo signal power is -14 dBm at 0.05 GHz and the PLL output power is 9.85 dBm at 4.08 GHz demonstrating that break-lock is achieved at 0.36 MHz frequency deviation. It is clear from Fig. 11 (b) that the frequency deviation required to break-lock is 0.51 MHz with the echo power of -10 dBm. From these above results, it is revealed that break-lock is achieved at higher value of frequency deviation with large echo power at the PLL input.

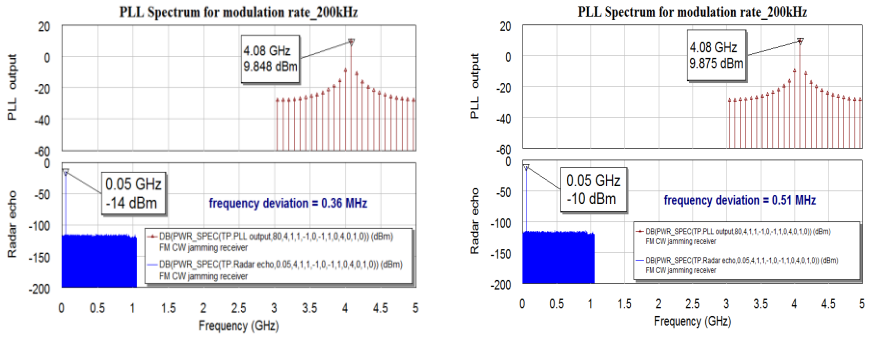

Fig. 11 (a) For echo power of -14 dBm (b) For echo power of -10 dBm.

5. Results and Discussion

The simulation and experimental results of frequency deviation required to break-lock as a function of jammer power and modulation rate are plotted and are shown in Figs. 12 and 13. The results are presented for modulation rates of 200, 300, and 400 kHz and the echo powers of -14 and -10 dBm.

From Fig. 12, it is seen that for a typical modulation rate of 200 kHz, break-lock is achieved at frequency deviations of 0.36 (simulation value) and 0.35 (measured value) MHz at -14 dBm jammer power. This shows good agreement between the simulation and measured results. It is also seen from Fig. 12 that for a typical modulation rate of 200 kHz, the frequency deviation required to break-lock is 0.36 MHz at jammer power of -14 dBm and its value is 0.19 MHz at -2 dBm of jammer power demonstrating break-lock is achieved at lower value of frequency deviation when the jammer power is high. From Fig. 12, it is noted that the break-lock is achieved at 0.36 and 0.91 MHz frequency deviations at jammer power of -14 dBm, for modulation rates of 200 and 500 kHz respectively, revealing that at lower values of modulation rate, break-lock is achieved at lower values of frequency deviation.

From the Fig. 12 and 13, it is estimated that for a modulation rate of 200 kHz and at a jammer power of -14 dBm, the break-lock is achieved at frequency deviations of 0.36 and 0.51 MHz for the echo signal powers of -14 and -10 dBm respectively.

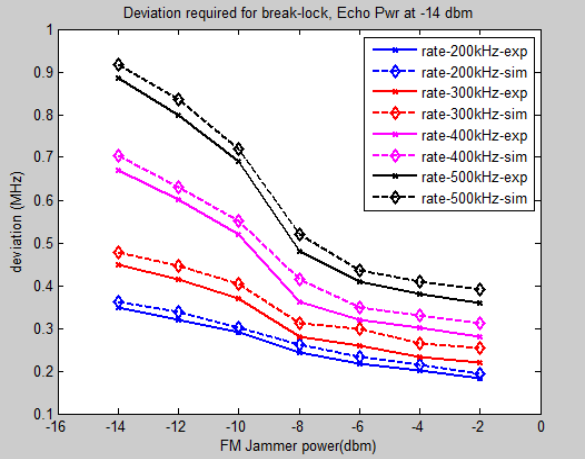

Fig. 12. Simulation and measured results of frequency deviation for -14 dBm echo power.

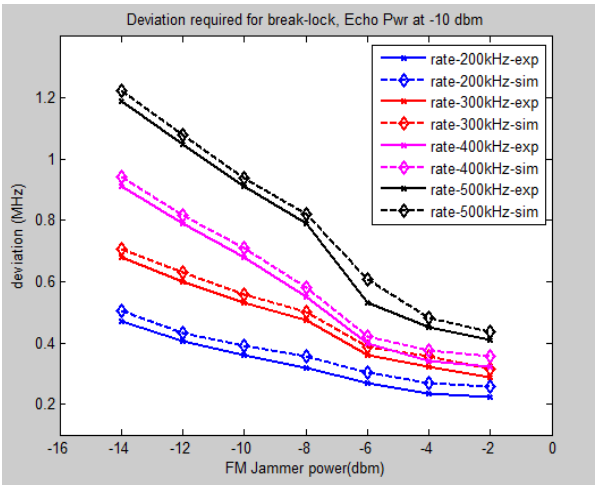

Fig. 13. Simulation and measured results of frequency deviation for -10 dBm echo power.

6. Conclusions

In the present work, the simulation and measured results of break-lock in PLL synthesizer in the presence of LFM jamming signal has been presented. The frequency deviation required to break-lock as a function of jamming signal power has been illustrated for different modulation rates and echo signal power.

Some concluding observations from the investigation are given below.

- Measured results show that the break-lock is achieved typically at 0.35 MHz (0.36 MHz simulation value) frequency deviation for a jammer power of -14 dBm and modulation rate of 200 kHz, with the echo power of -14 dBm at the PLL input. The measured values indicate good agreement with simulation results owing acceptable break-lock in the PLL.
- Furthermore, it is estimated that break-lock is achieved at frequency deviations of 0.36 and 0.91 MHz for the modulation rates of 200 and 500 kHz respectively, for a typical jammer power of -14 dBm.
- Therefore, it is demonstrated that the smaller the modulation rate, the lower the frequency deviation required to break-lock.
- Thus, the larger the echo signal power at the PLL input, the greater the frequency deviation required to break-lock.
- The results presented can be useful for successful modelling of PLL to be integrated within monopulse radar receivers for jamming using LFM interference signal.
- The results can be applied in the design of LFM jammers in the target platform for jamming tracking radar receivers employing PLLs.
- The work presented in this paper can be extended in estimating the break-lock with pulse modulated linear FM jamming signal. The linear FM jamming signal can be generated by VCO and voltage predistortion with delay-Line reference method.

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