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ASYMMETRICAL VOLTAGE SOURCE BASED THREE-PHASE NINE-LEVEL INVERTER WITH REDUCED POWER SWITCHES

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Abstract

A three-phase asymmetrical nine-level multi-level inverter is proposed in this paper. This inverter has less switching device and diode compare than other multi-level inverter topology. This inverter has asymmetrical voltage source 1:2:4 ratios. The fundamental frequency modulation method is used for control the inverter output voltage. Number of levels are increased by adding source section with few switches. The proposed circuit switching device is reduced further by replacing a diode in the source section, as a result, the control algorithm and driver circuit complexity are reduced further. The circuit cost and size is also reduced. The circuit is simulated using MATLAB. The proposed circuit prototype is implemented using PIC microcontroller. Both simulation and hardware results are verified.

Keywords: Bi-directional switch and asymmetrical source, Harmonic, Multi-level inverter.

1. Introduction

Due to industrial and commercial requirements are increases the research works in the area of the high-quality power supply and high power applications. The power supply generally has voltage sag, swell, harmonic and fluctuations problem due to more industrial load. Two and three-level inverter is mostly used in many industries, still its required high power and high voltage inverter. Rodriguez et al. [1], Franquelo et al. [2] and Rodriguez et al. [3] reported that a different inverter topologies were developed for reducing the harmonic and increase the voltage rating. Each topology has some merits and a demerit such as a diode-clamped multi-level inverter is required more no of the free-wheeling diode. Capacitor clamped multi-level inverter has a voltage balancing problem during capacitor charging and discharging period. Cascade multi-level inverter is required more no of switches and DC power supply [4, 5].

Many topologies are proposed for reducing the switches and DC power supply [6, 7]. Asymmetrical topology is proposed for reducing the dc power supply. In this method, the voltage source is taken unequally [8, 9]. This topology is used to reduce the system cost, size and improve the system stability. Mekhilef and Kadir [10] and Pak et al. [11] explained that a hybrid topology is also proposed for reducing the components and voltage source of the inverter [10, 11]. Bi-directional switches are used in the hybrid MLI to reduce the components count and improve the system performance [12-14]. These bi-directional switches are conducts in both directions. Many control methods were developed to improve the switching sequence and system performance. [15, 16].

In this paper, a new three-phase asymmetrical voltage source based multi-level inverter is proposed for reducing the components count and improve the system stability. The next sections explain the circuit operation, simulation results and, implementation results in one by one.

2. Circuit description

The new three-phase asymmetrical nine-level multilevel inverter circuit diagram is as shown in Fig. 1. This circuit is derived from a three-phase two-level inverter. It consists of three dc sources 1:2:4 ratios, bi-directional switches, and a two-level inverter. The bi-directional switches are used to block the high voltage and easy current flow from the midpoint to other directions. The fundamental frequency modulation method is used to control the proposed nine-level inverter. The required output voltage level is achieved by turn on the corresponding switch and source.

The inverter line-to-line voltage waveforms V_{ab}, V_{bc}, and V_{ca} with corresponding switching gate signals are depicted in Fig. 2 where V_{ab}, V_{bc}, and V_{ca} are related to V_{ag}, V_{bg}, and V_{cg} by:

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (1)$$

The inverter line-to-neutral voltages V_{aN}, V_{bN}, and V_{cN} may be expressed as:

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (2)$$

It is useful to recognize that the inverter voltages at terminals *a*, *b*, and *c* with respect to the midpoint (*o*) are given by:

$$\begin{bmatrix} v_{ao} \\ v_{b0} \\ v_{co} \end{bmatrix} = \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} - \begin{bmatrix} v_{og} \\ v_{0g} \\ v_{0g} \end{bmatrix} \quad (3)$$

where V_{og} is the voltage at midpoint (*o*) with respect to ground (*g*). V_{og} routinely fluctuates among three different voltage values V_{dc}, 2 V_{dc} and 3 V_{dc} as follows:

$$V_{og} = \begin{cases} 1V_{dc} & if\ S_a + S_b + S_b \leq 5 \\ 2V_{dc} & if\ S_a + S_b + S_b = 6 \\ 3V_{dc} & if\ S_a + S_b + S_b \geq 7 \end{cases} \quad (4)$$

The following equations can be used to derive *d* and *q* voltage components for all inverter vectors:

$$V_q = \frac{4V_{dc}}{3(N-1)}\ (2S_a - S_b - S_c) \quad (5)$$

$$V_d = \frac{4V_{dc}}{\sqrt{3}(N-1)}\ (S_c - S_b) \quad (6)$$

$$V = V_q - JV_d \quad (7)$$

THD% of the output voltage can be calculated by

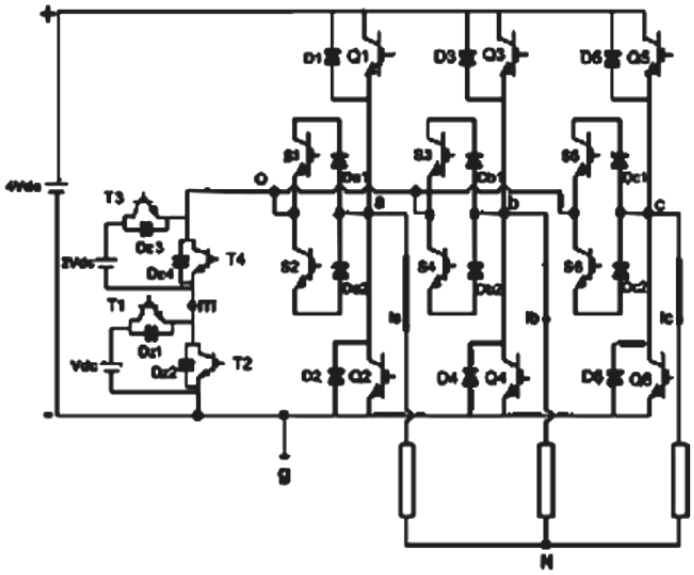
$$THD\% = \frac{\sqrt{\sum_{k=2}^{\infty} {V_k}^2}}{V_1} * 100\% \quad (8)$$

where V_1 and V_k are the fundamental component and harmonic order, respectively.

One semiconducting switch T2 is replaced with a diode from the proposed inverter circuit. As a result, the circuit control mechanism is simplified and driver circuit requirement is also reduced. The modified inverter also gives the same performance with the less conducting switch. The next section explains the simulation results.

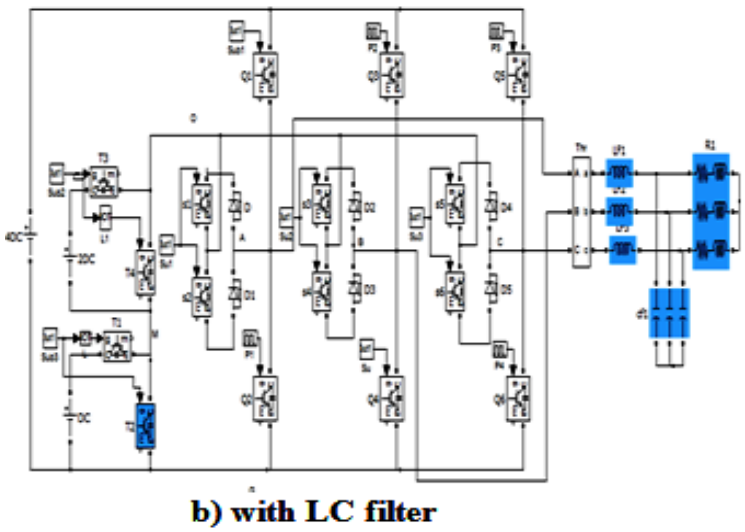
Table 1. Three-phase nine-level inverter switching pattern.

	Q1	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**T1**	**T2**	**T3**	**T4**
4 *Vdc*	1	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0
3 *Vdc*	1	0	0	0	0	1	0	0	1	1	0	0	1	0	1	0
2 *Vdc*	1	0	0	0	0	1	0	0	1	1	0	0	0	1	1	0
Vdc	1	0	0	0	0	1	0	0	1	1	0	0	1	0	0	1
0 *Vdc*	1	0	0	1	0	1	0	0	0	0	0	0	1	0	0	1
Vdc	0	1	0	0	1	0	0	0	1	1	0	0	1	0	1	0
-2 *Vdc*	0	1	0	0	1	0	0	0	1	1	0	0	1	1	1	0
-3 *Vdc*	0	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
-4 *Vdc*	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1



a) without LC filter

(a) Without LC filter.



b) with LC filter

(b) With LC filter.

Fig. 1. Proposed circuit diagram.

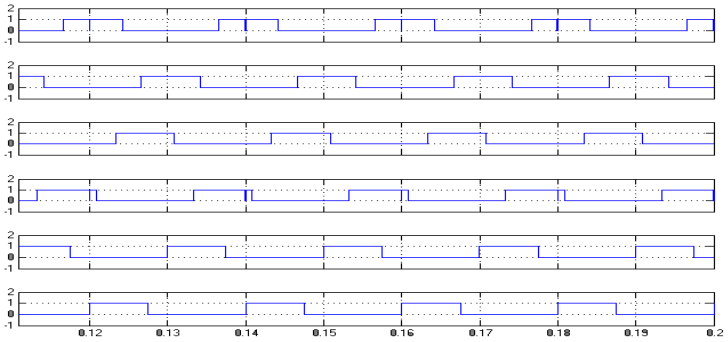


Fig. 2. Driving pulse for switch Q1, Q2, Q3, Q4, Q5 and Q6.

3. Simulation Results and Discussions

Figure 3 shows the Simulink model of the modified nine-level inverter circuit diagrams using LC filter. One semiconducting switch T2 is replaced with a diode from the proposed inverter circuit. This circuit is used to convert dc supply into nine-level AC output. The LC filter is used to convert staircase output into a sinusoidal output voltage and also reduce the harmonic.

The proposed nine-level inverter circuit diagrams without using an LC filter is used to convert dc supply into nine-level AC output. The LC filter is used to convert staircase output into a sinusoidal output voltage and also reduce the harmonic. Figure 4 shows the voltage across V_{og}. This output voltage represents the single source output from O point to g point via a bi-directional level switch. Figure 5 shows the voltage across V_{ao}. This output voltage represents the two voltage (1:2) source output from O point to a point via a bi-directional level switch. Figure 6 shows the voltage across phase to phase. This output voltage represents the three voltage (1:2:4) source output via two-level and a bi-directional switch.

Figure 7 shows the voltage across V_{og}. This output voltage represents the single source output from O point to g point via a bi-directional level switch. Figure 8 shows the voltage across V_{ao}. This output voltage represents the two voltage (1:2) source output from O point to a point via a bi-directional level switch.

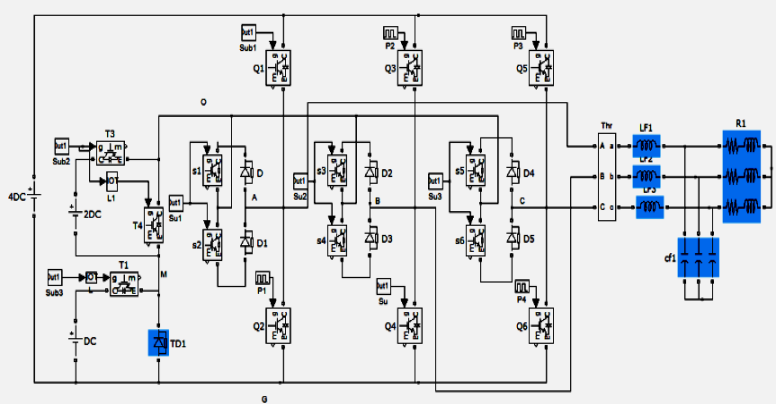


Fig. 3. Modified three phase nine-level inverter circuit diagram with LC filter.

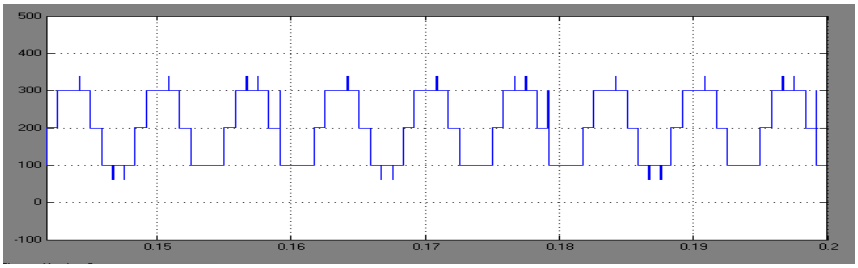


Fig. 4. Voltage across V_{og}.

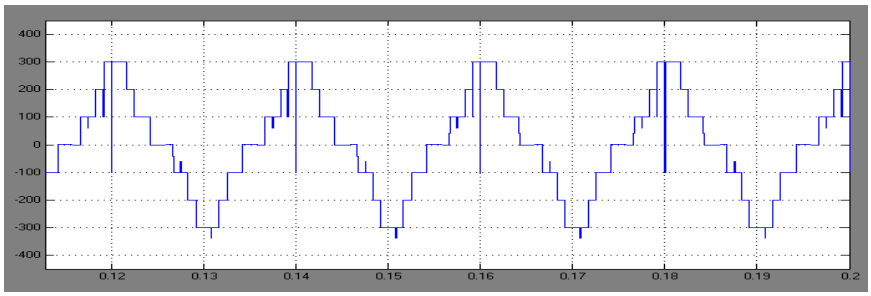


Fig. 5. Voltage across V_{ao}.

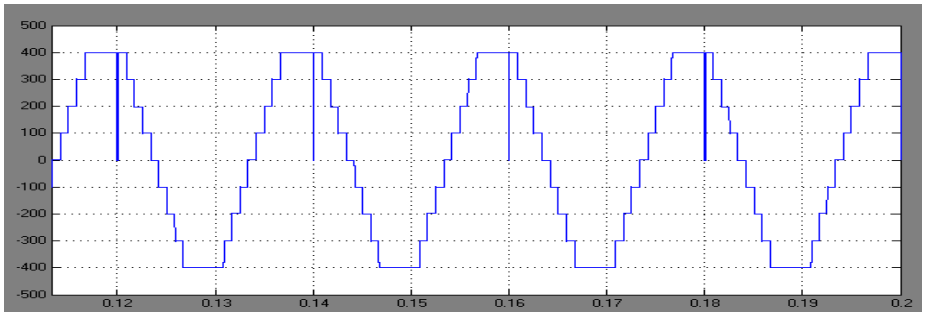


Fig. 6. Phase to phase voltage.

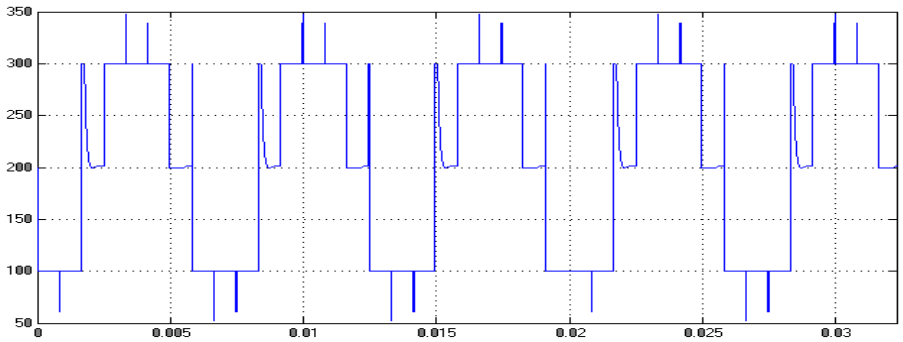


Fig. 7. Voltage across V_{og}.

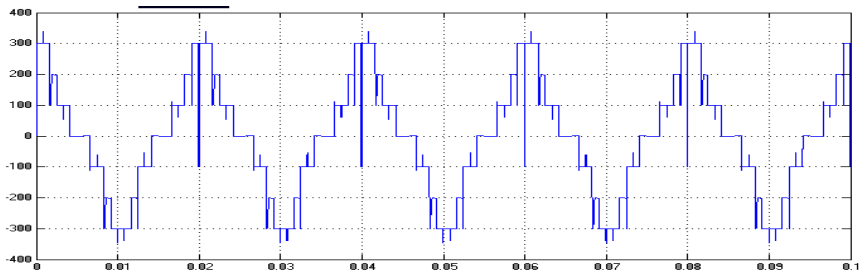


Fig. 8. Voltage across V_{ao}.

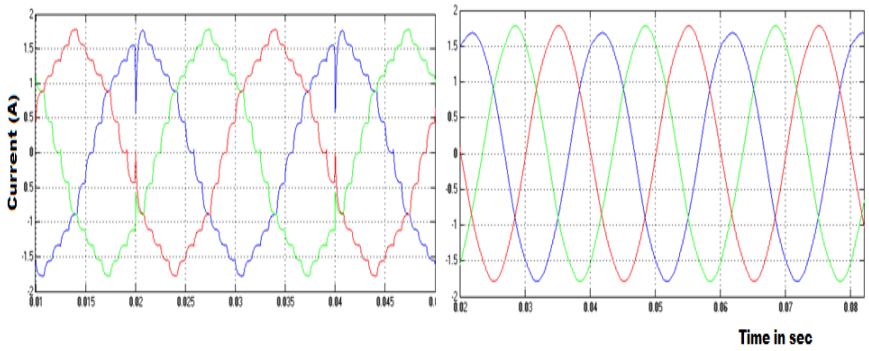
4. Comparative Analysis

The circuit performance is compared with simulation results. The proposed circuit output current is as shown in Fig. 9 using without a filter and with a filter. The current has some distortion and a staircase. The output current has more harmonic without filter circuit. This distortion and step wave is converted into sinusoidal form with the help of the LC filter. The output current has lower harmonic with a filter circuit. The inverter output voltage is as shown in Fig. 10 using without a filter and with a filter. The voltage has staircase output and spike. The output voltage has more harmonic without filter circuit. This distortion and step wave is converted into sinusoidal form with the help of the LC filter. The output voltage has a lower harmonic with a filter circuit. It is proven from Fig. 11. The current THD is as shown in Fig. 11 without and with a filter. The current has THD of 7.14% without filter and THD of 2.52% with a filter.

The circuit performance is compared with simulation results. The modified circuit output current is as shown in Fig. 12 using without a filter and with a filter. The current has some distortion and a staircase. The output current has more harmonic without filter circuit. This distortion and step wave is converted into sinusoidal form with the help of the LC filter. The output current has lower harmonic with a filter circuit. The inverter output voltage is as shown in Fig. 13 using without a filter and with a filter. The voltage has staircase output and spike. The output voltage has more harmonic without filter circuit. This distortion and step wave is converted into sinusoidal form with the he the LC filter. The output voltage has a lower harmonic with a filter circuit. It is proven from Fig. 14. The current THD is as shown in Fig. 14 without and with a filter. The current has THD of 7.74% without filter and THD of 2.56% with a filter. Both the proposed and modified circuit has performance except switch count. It is shown in Table 2.

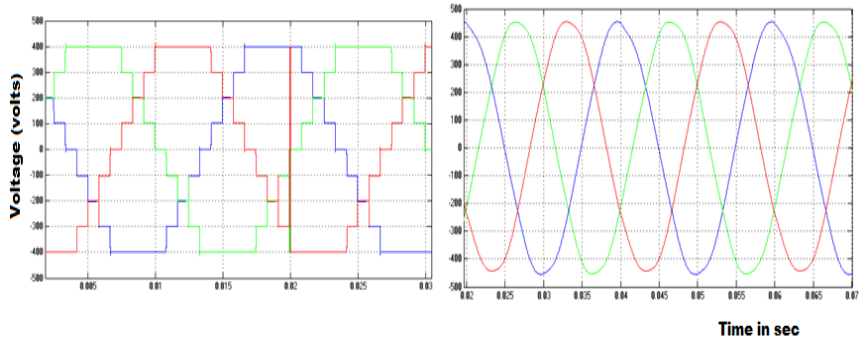
Table 2. Performance parameters.

Parameters	New 3-phase 9-level without a filter	New 3-phase 9-level with diode	New 3-phase 9-level with filter	New 3-phase 9-level with diode and filter
Input voltage (4 V_{dc})	400 V	400 V	400 V	400 V
No. of switches	16	15	16	15
No. of diodes	6	7	6	7
THD%		7.74	2.52	2.56



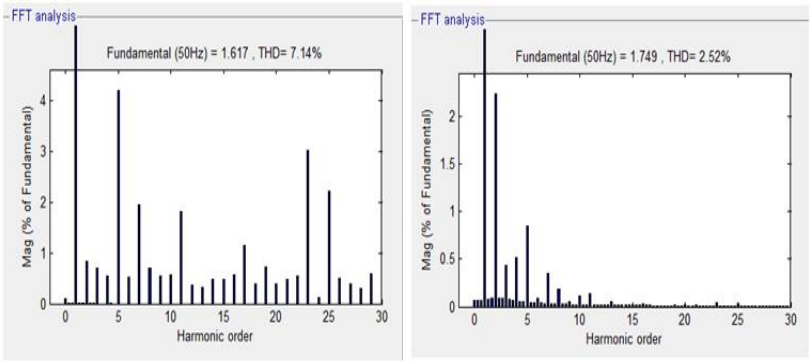
(a) **(b)**

Fig. 9. Proposed inverter output current a) Without LC filter, b) With LC filter.



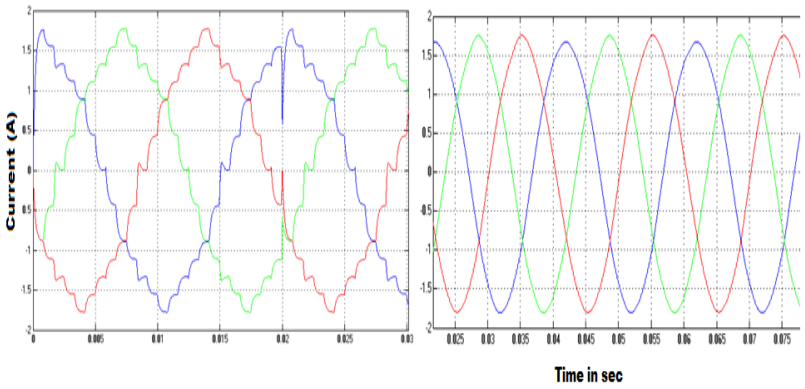
(a) **(b)**

Fig. 10. Proposed inverter phase to phase voltages (a) without LC filter, (b) with LC filter.



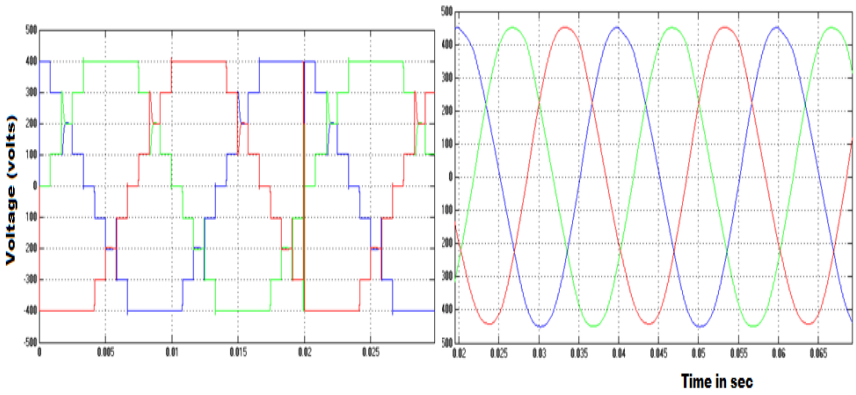
(a) **(b)**

Fig. 11. FFT analysis a) Without LC filter, b) With LC filter.



(a) **(b)**

Fig. 12. Modified inverter output current (a) Without LC filter, (b) With LC filter.



(a) **(b)**

Fig. 13. Modified inverter phase to phase voltage (a) Without LC filter, (b) With LC filter.

5. Implementation Results

Figure 14 shows a prototype layout of the modified asymmetrical nine-level inverter circuit diagram using a low voltage rating. Table 3 shows the components used in the implementation. This circuit consists of AC input, DC source 1:2:4 ratio, modified nine-level inverter and load. The inverter circuit is controlled using PIC16F877A pic controller. PIC controller is used to producing the required triggering pulse output. Figure 15 shows the voltage source V_{dc1} output. Figure 16 shows the voltage source V_{dc2} output. Figures 17 to 19 show the triggering pulse for switches S1, T1 and Q1. The inverter converts DC to AC voltage with steps. The output voltage has nine steps from +ve top to -ve bottom so it is called nine-level output. Figure 20 shows the Inverter output voltage.

Table 3. Hardware components rating.

Components	Rating
V_{dc1}	12 V
V_{dc2}	24 V
V_{dc3}	48 V
Capacitor C1, C2	1000 UF
Controller	PIC16F877A
Load resistor	1000 Ω
Diode	Uf4007

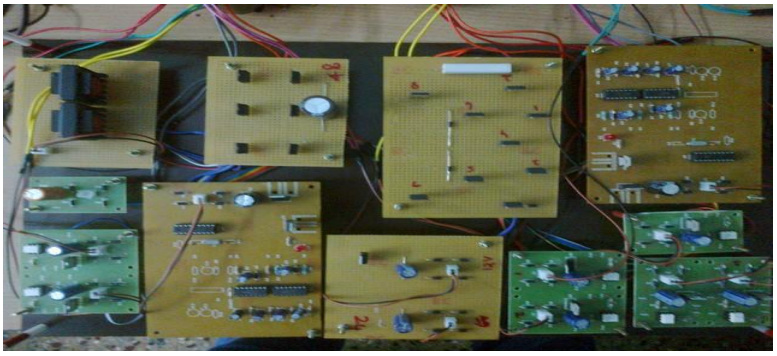


Fig. 14. Layout of modified asymmetrical nine-level inverter circuit diagram.

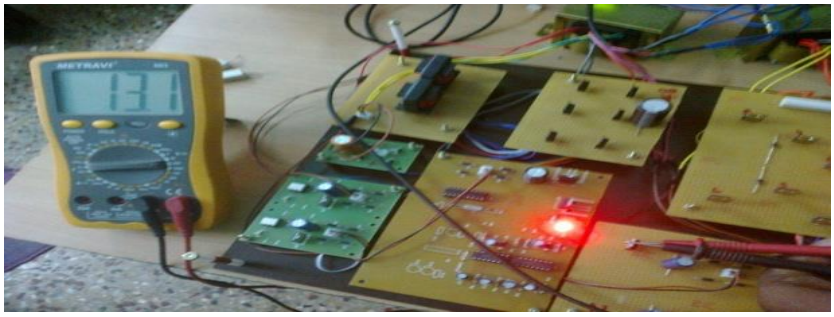


Fig. 15. DC link source voltage V_{dc1}.

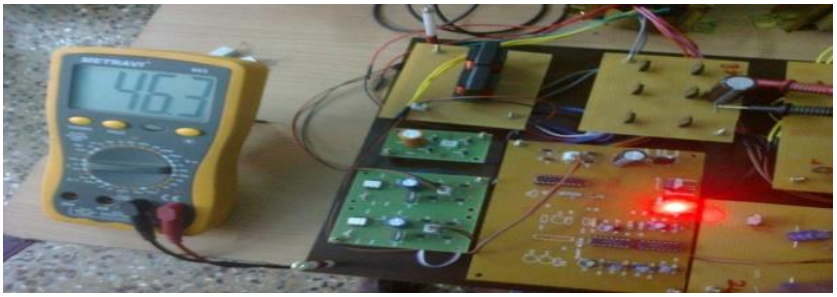


Fig. 16. DC link source voltage V_{dc2}.

Fig. 17. Triggering pulse for switches S1.

Fig. 18. Triggering pulse for switches T1.

Fig. 19. Triggering pulse for switch Q1.

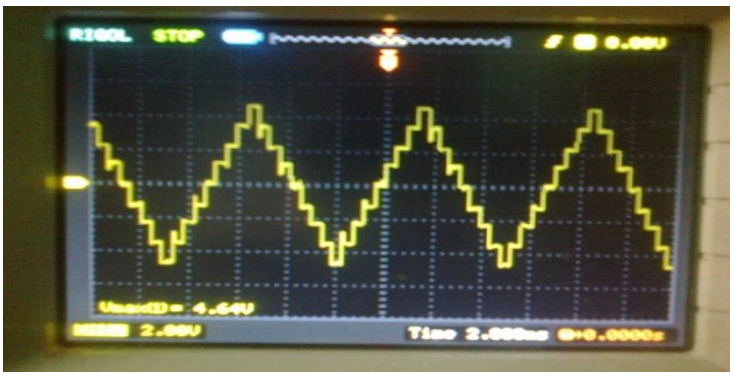


Fig. 20. Inverter output voltage.

6. Conclusions

Three phase asymmetrical nine-level multi-level inverter and modified asymmetrical nine-level multi-level inverter were proposed in this paper. The circuit operation and simulation results were presented and discussed. Both circuit performances are compared with simulation results. The proposed nine multi-level inverter has a lower harmonic compare than other lower-level (such as two five seven-level) multi-level inverter. The modified nine-level inverter circuits have less component count and less conduction loss compare than a proposed multi-level inverter. The circuit produced the nine-level output using an asymmetrical voltage source ratio 1:2:4. The results are verified by hardware and simulation results. This work further extended for interfacing with a renewable energy source.

Nomenclatures

Q1	Driving pulse for switch 1
Q2	Driving pulse for switch 2
Q3	Driving pulse for switch 3
Q4	Driving pulse for switch 4
Q5	Driving pulse for switch 5
Q6	Driving pulse for switch 6
S1	Switch 1
S2	Switch 2
S3	Switch 3
S4	Switch 4
S5	Switch 5
S6	Switch 6
T1	Trigger pulse for switch 1
T2	Trigger pulse for switch 2
T3	Trigger pulse for switch 3
T4	Trigger pulse for switch 4
V_{dc1}	Voltage source 1
V_{dc2}	Voltage source 2
V_{dc3}	Voltage source 3

Abbreviations

MLI	Multi-Level Inverter
THD	Total Harmonic Distortion

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