COMPARATIVE ANALYSIS OF VARIOUS MODULATION TECHNIQUES FOR CASCADED MULTILEVEL INVERTER BY IMPLEMENTING P&O ALGORITHM

S. SATISH KUMAR^{1,*}, A. SURESH¹, M. SASIKUMAR³, T. SASILATHA¹, D. LAKSHMI¹, P. SIVAPERUMAL¹, J. S.ASHWIN¹, ZURAIDAH HARITH²

¹AMET Deemed to be University, Chennai, India ²INTI International University, 71800, Negeri Sembilan, Malaysia ³C. Abdul Hakeem college of Engineering and Technology, Vellore, India *Corresponding Author: satishkumarjec@gmail.com

Abstract

This dissertation presents a comparative analysis of three modulation techniques, namely, Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD) techniques. The three modulation renewable techniques discussed above are suitable in Cascaded Multilevel Inverter (CMI) for PV systems by using Perturb & Observe (P&O).It is useful in high-power applications. The system behaviour was examined, and the benefits and downsides of each technique were thoroughly described. Total Harmonic Distortion (THD) and RMS voltage were the key comparison metrics used in the investigation. A comprehensive P&O study was conducted on the basis of system stability. Utilizing the P&O MPPT Algorithm and MATLAB/Simulink, the effectiveness of three modulation approaches were examined and validated using MATLAB/Simulink.

Keywords: Alternative phase opposition disposition, Multilevel inverter, Phase disposition, Phase opposition disposition, Total harmonic distortion.

1.Introduction

In the modern era, Multilevel Inverter is an emerging system for low voltage and high power applications, where it synthesizes the sinusoidal voltage waveform smoothly. In comparing with the traditional two-level inverter MLI inverter possess more advantages, where most researchers started focusing towards the MLI. The major advantage of Multilevel Inverter it has fewer harmonics in its output voltage as well as in output current, in addition, MLI has low voltage stress on the power switches and low Electromagnetic Interference (EMI) [1, 2]. There are three different categories for multilevel inverters: 1) diode-clamped multilevel inverters, 2) flying capacitor multilevel inverters, and 3) cascaded multilevel inverters (CMLI). Cascaded Multilevel Inverter is further divided into two categories as Symmetrical and Asymmetrical system, where Symmetrical CMLI has symmetrical ratios DC sources and Asymmetrical has in the different ratios of DC sources depending upon required output level of voltage [3-5]. This paper focuses mainly on Cascaded MLI with a symmetrical system for seven level output voltage. The performance analysis of seven-level inverter is performed with PWM techniques PD, POD and APOD. The main aim is to enhance the system stability to achieve better output voltage with less switching losses and to reduce the THD of the system [6]. The importance of choosing CMLI over Diode clamped and flying capacitor in this paper is due to the diode less and capacitor-less. In Fig. 1 CMLI is designed with a PV system is shown.



Generally, The solar PV system has a nonlinear feature that is mostly influenced by factors like temperature and irradiation. Consequently, The solar PV system's power is similarly non-linear [7]. Due to their capacity to produce the most power, solar PV systems are attracting study attention, which means that researchers must regularly examine this issue. Therefore, more scientists are concentrating on ways to getmore

power out of the system. The module's maximum power tracking method (MPPT), which is based on the current and voltage that the solar panel can produce. [8-10].

Taking the effect of leakage current in P-N junction into account, a parallel resistance R_P has been addition with the PV array [11, 12]. A current source is shown in parallel with a single diode in the equivalent circuit of the single-diode R_S and R_P in PV model. To create an accurate model, five unknown parameters must be determined [13]. Those five unknown parameters are the following: Photo current source (I_{ph}), Reverse saturation current (I_r), Diode ideality factors (A), Series resistor (R_S) and parallel rea sistor (R_P) [14]. Comparing this model to the ideal PV model, significant and effective results have been obtained. The simulation is more accurate thanks to the R_P cell model, but complexity increases because of the addition of parallel resistance. Basic expression for PV model as shown. The model of single diode R_S and R_P is displayed in Fig. 2.

The solar PV output current equation,

$$I = I_{pv} \cdot (I_d + I_p) \tag{1}$$

where,

$$I_p = \frac{V_d}{R_p} = V_p = \frac{V_{pv} + I_{pv} \cdot R_s}{R_p}$$
(2)

Equation indicates the I-V characteristic, Eq. (3)

$$I = I_{pv} - I_0 \left[\exp\left(\frac{V_{pv} + I_{pv} \cdot R_s}{V_t}\right) - 1 \right] - \frac{V_{pv} + I_{pv} \cdot R_s}{R_p}$$
(3)

where $V_{pv_{\square}}$ are the diode voltage, correspondingly I_{pv} diode current and V_t is thermal voltage. The MPPT approach is the most effective, according to the literature, for calculating the maximum power that can be used when solar PV systems are present. Power will remain constant under normal circumstances. Although it is simple to use electricity from the solar PV system, doing so in real time is not practical. To track maximum power, the Perturb and Observe (P&O) method was employed [15]. The following is how this paper is structured: Section 2 Discussion on PD, POD, and APOD PWM Techniques, Section 3 explanation on MPPT Algorithm Perturb and Observe for PV Systems, In Section 4 Simulation Results by comparing with PD, POD and APOD PWM Techniques, Finally, Section 5 gives Conclusion.

2. Analysis for PD, POD and APOD

2.1. Phase disposition

In Phase Disposition, all the carrier wave will in the same phase, for seven-level inverter there will be six carrier waveforms. In this carrier, waveform will be in the same phase and reference wave form will be in 120° phase shift. There will be (n-1) carrier waveform [16]. The reckoning for magnitude of Modulation Index is $m_{ap} = 2A_m/(m-1)A_c$



Fig. 2. Phase Disposition modulation technique.

When the reference is bigger than both of the carrier waveforms, the converter is switched to + Vdc / 2.When the reference exceeds the lower carrier waveform but falls short of the upper carrier waveform, the converter is turned to zero. The converter is switched to -Vdc / 2 when any carrier waveform is smaller than the reference. Figure 2 depicts the pulses used in the PD modulation approach.

2.2. Phase opposition disposition

The carrier wave forms above the origin are in phase in POD, while those below the origin are 180° out of phase. It also has (n-1) carrier with 'n' DC sources as PD [17]. Figure 3 depicts the POD pulse.





The reference signal will be greater than the converter's two below-described carrier waveforms when it is switched to +Vdc/2. When the converter is set to 0, the reference waveform is larger than the lower carrier waveform, while the higher carrier waveform is smaller. When the converter is set to -Vdc/2, the carrier waveforms are larger than the reference waveform.

Journal of Engineering Science and Technology

Special Issue 2/2024

2.3. Alternative phase opposition disposition

In this Modulation method, the following three carrier waveforms will be present above the zero level. The carrier will be 180 degrees out of phase with carrier 2 and carrier 3, and it will appear to carrier 1 with a different amplitude [18].

When switching, the carrier waveform will be less than reference when it is +Vdc/2. The reference is lower than the top carrier waveform and higher than all other carriers when operating for +Vdc/4. The reference for 0 is larger than the lower carrier waveform and less than the two uppermost carrier waveforms. The reference is greater than the lowest carrier waveform and less than all other carriers when the switch is running at -Vdc/4, and it is less than all carrier waveforms when the switch is operating at -Vdc/2. Figure 4 displays the switching pulses for APOD.



Fig. 4. Alternative phase opposition disposition modulation technique.

3.MPPT Algorithm (Perturb and Observant)

The P&O algorithm also goes by the name "hill-climbing", however, based on how the method was implemented, both titles applied to the same algorithm. The power converter's duty cycle is perturbed by the hill-climbing technique, and P&O aids in the DC link operating voltage perturbation between the PV array and the power converter [19].Modifying the duty cycle of the power converter in the hill-climbing scenario entails changing the voltage of the DC link between the PV array and the power converter, so identical names are mentioned in both techniques. The next perturbation size is determined using both approaches based on the previous perturbation's sign and the previous power increment's sign. When power is increasing on the left and voltage is increasing on the right at the same time, power is increasing on the right.

The size of the perturbation grows in the same direction as the rise in power. When power is reduced, the size of the disturbance invariably moves in the other direction. The P&O algorithm's primary operational feature is implemented in this publication. Figure 5 depicts the P&O algorithm's flowchart.



Fig. 5. Flowchart P&O algorithm.

Table 1. Description of 250W PV unit.

Parameter in solar panel	Datasheet
Open circuit voltage(V_{oc}), [V]	37.80
Short circuit current(I _{sc}), [A]	8.80
Maximum peak over voltage(V _{po}), [V]	30.60
Maximum peak over current(Ipo), [A]	8.20
Maximum power rating in watts (P _M), [W]	250
Series cell	60

4. Simulation Results

In Fig. 6, P & O MPPT algorithm is shown which is designed for a solar PV system, where it is designed with a flow chart. Each H-Bridge will be connected with a 1kw panel with a total of 3 kW input power. Cascaded Multilevel Inverter by utilizing PD, POD, APOD techniques are designed with MATLAB/Simulink.



Fig. 6. Modelling of P&O.

Journal of Engineering Science and Technology

Special Issue 2/2024

The output voltage of PD, POD, APOD are same, and it is displayed in Fig. 7. The output voltage is 475 V, and the current is 1.8 A. In detail, Vrms voltage and.



Fig. 7.The output voltage of APOD techniques.

THD (FFT) analysis for CMLI are shown in Figs. 8, 9, and 10. The Vrms for Phase Disposition (PD) technique is 315.3V, Phase Opposition Disposition (POD) technique is 312.1 V and for Alternative Phase Opposition Disposition (APOD) technique is 318.6 V.



Fig. 8. THD for PD technique.



Fig. 9. THD for POD technique.

The THD (%) for APOD is low compared to PD and POD, were APOD has 1.44%, PD has 2.74 % and POD has 2.61 %



Fig. 10. THD for APOD technique.

Table 2 shows the effectiveness of modulation techniques with modulation index. The Comparison of Total harmonics distortion for the various modulation techniques vs. Modulation index as shown in Fig. 11.

Modulation	% of THD in PD	% of THD in POD	% of THD in APOD
Index (M)	technique	technique	technique
0.7	5.32	7.29	5.77
0.8	5.05	6.65	4.59
0.9	4.96	5.38	2.36
1	2.74	2.61	1.44

Table 2. Comparision of modulation techniques with Modulation index.



Fig. 11. Comparison of Th.D. vs. Modulation index

5. Conclusion

In this paper, three modulation techniques PD, POD, and APOD are discussed, and comparative analysis is done by utilizing renewable energy source (PV system). The system is designed for seven level CMI. Perturb &Observant MPPT algorithm is modelled and implemented for comparison analysis. It is found that APOD modulation technique has low THD (%) compared to PD and POD. In future, this technique can be applied for a grid connected system by using various MPPT algorithms.

References

1. Mythili, V.; Suresh, A.; Devasagayam, M.M.; and Dhanasekaran, R. (2019). SEAT-DSR: Spatial and energy aware trusted dynamic distance source routing

Journal of Engineering Science and Technology

Special Issue 2/2024

algorithm for secure data communications in wireless sensor networks. *Cognitive Systems Research*, 58, 143-155.

- 2. Karthikeyan, V.; Jamuna, V.; and Christopher, I.W. (2021). Phase disposition PWM based multi level inverter with reduced number of switches. *Advanced Aspects of Engineering Research*, 7, 1-15.
- 3. Rodríguez, J.; Bernet, S.; Wu, B.; Pontt, J.O.; and Kouro, S. (2007). Multilevel voltage-source-converter topologies for industrial medium-voltage drives. *IEEE Transactions on Industrial Electronics*, 54(6), 2930-2945.
- 4. Kouro, S.; Rebolledo, J.; and Rodríguez, J. (2007). Reduced switchingfrequency-modulation algorithm for high-power multilevel inverters. *IEEE Transactions on Industrial Electronics*, 54(5), 2894-2901.
- Aghdam, M.G.H.; Fathi, S.H.; and Gharehpetian, G.B. (2008). Analysis of multi-carrier PWM methods for asymmetric multi-level inverter. *Proceedings* of the 2008 3rd IEEE Conference on Industrial Electronics and Applications. Singapore, 2057-2062.
- 6. Malinowski, M.; Gopakumar, K.; Rodriguez, J.; and Perez, M.A. (2009). A survey on cascaded multilevel inverters. *IEEE Transactions on industrial electronics*, 57(7), 2197-2206.
- Govindaraju, C.; and Baskaran, K. (2010). Efficient hybrid carrier based space vector modulation for a cascaded multilevel inverter. *Journal of Power Electronics*, 10(3), 277-284.
- Kumar, S.S.; and Sasikumar, M. (2016). An approach of hybrid modulation in fusion seven-level cascaded multilevel inverter accomplishment to IM drive system. *Proceedings of the 2016 Second International Conference on Science Technology Engineering and Management (ICONSTEM)*. Chennai, India, 383-387.
- 9. Sujitha, N.; Kumar, S.S.; and Sasikumar, M. (2014). Design and implementation of hybrid SPWM control for cascaded H-bridge multi level inverter for motor drives. *IU-Journal of Electrical & Electronics Engineering*, 14(1), 1721-1727.
- Kumar, S.S.; and Kumar, M.S. (2019). Diminution of harmonics in a cascaded multilevel inverter using third harmonics injection PWM technique. *International Journal of Recent Technology and Engineering (IJRTE)*, 8(3), 7493 7497.
- Sasilatha, T.; Subbiah, B.; and Kumar, P.S.M. (2018). Detection of multi-layer attack using anticipated relay algorithm in the wireless sensor networks. *International Journal of Mechanical and Production Engineering Research and Development (IJMPERD)*, 8(6), 2249-6890.
- Muthukumar, P.; Lekshmi Kanthan, P.S.; Baldwin Immanuel, T.; and Eswaramoorthy, K. (2018). FPGA performance optimization plan for high power conversion. In Zelinka, I.; Senkerik, R.; Panda, G.; and Lekshmi Kanthan, P. (Eds.). *Soft computing systems*. ICSCS 2018. Communications in Computer and Information Science, Vol. 837. Springer, Singapore, 491-502.
- Lakshmi, D.; Baskaran, S.; Ezhilarasi, G.; and Valli, C. (2020). Direct AC/DC power converter using auxiliary circuits. *International Journal of Advanced Science and Technology*, 29(7s Special Issue), 785-793.

- 14. Palanivel, P.; and Dash, S.S. (2011). Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques. *IET Power Electronics*, 4(8), 951-958.
- 15. Babaei, E.; Gowgani, S.S.; and Sabahi, M. (2015). A new cascaded multilevel inverter with series and parallel connection ability of DC voltage sources. *Turkish Journal of Electrical Engineering and Computer Sciences*, 23(1), 85-102.
- Chabni, F.; Taleb, R.; and Helaimi, M.H. (2017). ANN-based SHEPWM using a harmony search on a new multilevel inverter topology. *Turkish Journal of Electrical Engineering and Computer Sciences*, 25(6), 4867-4879.
- 17. Kumar, S.; and Kumar, M.S. (2020). Asymmetric hybrid multilevel inverter with reduced harmonic using hybrid modulation technique. *International Journal of Power Electronics and Drive System (IJPEDS)*, 11(2), 605-610.
- Matale, N.P.; Thakre, M.P.; and Borse, P. S. (2022). A seven-level cascaded multilevel inverter based on simplified SVPWM method. *International Journal of Engineering, Science and Technology*, 14(3), 85-93.
- Kumar, D.G.; Ganesh, A.; Sireesha, N.V.; Kshatri, S.S.; Mishra, S.; Sharma, N.K.; Bajaj, M.; Kotb, H.; Milyani, A.H.; and Azhari, A.A. (2022). Performance analysis of an optimized asymmetric multilevel inverter on grid connected SPV system. *Energies*, 15(20), 7665.