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FPGA IMPLEMENTATION OF PULSE WIDTH MODULATION FOR 9-LEVEL SWITCHED CAPACITOR INVERTER

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Abstract

Switched Capacitor Multilevel Inverters (SC-MLIs) serve as a compelling alternative to conventional MLIs due to their enhanced harmonic profile and high boosting capability. This work presents a novel 9-level SC-MLI topology with an optimised component count. The presented topology consists of six unidirectional switches, two bidirectional switches, three diodes, three capacitors, and a single DC voltage source. The proposed design focuses on reducing the voltage stress levels, improving the harmonic profile, optimising the component count, and achieving a high voltage boosting factor. The design utilised the Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) to generate the gate pulses. A comparative analysis was performed with the existing solutions, and the proposed design achieved a Total Standing Voltage (TSV) of 4.5 per unit (p.u.) and a voltage Total Harmonic Distortion (THD) of 8.83%. The dynamic response of the proposed topology was simulated with the Quartus II software and MATLAB/Simulink, followed by hardware validation with a Field Programmable Gate Array (FPGA) to generate the PWM signals.

Keywords: Field programmable gate array, Multilevel inverter, Switched capacitor, Total harmonic distortion, Total standing voltage.

1. Introduction

Multilevel Inverters (MLIs) have shown growing interest in multiple fields, such as Electric Vehicles (EVs), renewable energy systems, flexible Alternating Current (AC) transmission systems, and motor driver systems. This phenomenon is attributed to the greater power quality and performance of MLIs, such as improved harmonic performance, lower voltage stress on semiconductor switches, minimised filtering requirements, and lower rate of change of voltage (dv/dt) compared to two-level inverters [1, 2]. However, conventional MLIs, such as the Flying Capacitor (FC), Cascaded H-Bridge (CHB), and Neutral Point Clamped (NPC) topologies, each presented distinct limitations [1, 3, 4]. For instance, CHB-MLIs poses the need for multiple isolated DC sources as well as costly and bulky phase-shifting transformers in its topology. FC-MLIs face capacitor voltage balancing issues due to the lack of symmetrical charging and discharging sequences. Contrarily, the diodes required in NPC-MLIs greatly increase when attaining higher voltage levels, thus leading to a higher inverter cost [1]. Consequently, the ongoing research in MLIs emphasises the component count and self-boosting capabilities as it greatly affects the inverter cost and the necessity for additional DC-DC converters [4].

Therefore, Switched-Capacitor Multilevel Inverters (SC-MLIs) have emerged as a potential alternative in efforts to counter the limitations of conventional MLIs owing to their ability to achieve a greater output power quality and lower component count [5]. SC-MLIs also offer high self-boosting and self-balancing capacitor voltage capabilities even with fewer DC voltage sources [6]. The reduced isolated DC sources would then enable greater practicality and lower implementation complexity, especially in renewable energy systems [7]. The voltage boosting capability of SC-MLIs also complements the implementation of low DC voltage sources including, renewable energy sources and EVs, thus omitting the necessity for bulky inductors or transformers [8]. As the SC units are charged in parallel to a fixed voltage and discharged in a controlled order, this enables a consistent charging and discharging sequence. Consequently, the capacitor voltage would be balanced without the need of complex voltage control strategies [9]. This also leads to greater operational efficiency and reduced Electromagnetic Interference (EMI), thus resulting in greater practicality in high-power applications [10]. The extensive research on SC-MLIs is driven by achieving a high boosting factor, a reduced number of components and stress of the switches and maximising the use of the DC-link voltage [11].

In recent literature, SC-MLIs with various output voltage levels have been presented and were evaluated in terms of the boosting factor, number of components, Total Harmonic Distortion (THD), and the Total Standing Voltage (TSV). The two evaluation metrics – THD and TSV, express the similarity of the output waveform as compared to an ideal sine wave, and the Maximum Blocking Voltage (MBV) normalised to the boosted output voltage ($V_{Peak,Out}$) as depicted in Eq. (1) [9, 12].

$$\mathrm{TSV_{pu}} = \frac{\mathrm{MBV}}{\mathrm{V_{Peak,out}}} \tag{1}$$

A study proposed a 31-level SC-MLI, achieving a low voltage THD of 3.22% and a low TSV of 4.66 p.u.., as well as a significant boosting factor of 15. However, the significant performance required 52 components, including 20 unidirectional switches, 20 gate drivers, four diodes, six capacitors, and two isolated DC sources. Therefore, contributing to a high inverter cost to achieve a low THD, TSV, and a

high boosting factor [5]. Contrarily, a 13-level topology utilised fewer components, which was a total of 32 components, and achieved a voltage THD of 9.83% and a 6-fold boosting factor [12]. A lower-level SC-MLI topology, such as an 11-level SC-MLI was also presented. It only utilised 20 components and achieved a 5-fold boosting factor. However, it exhibited a voltage THD of 10.86%, a TSV of 5 p.u., and required 2 isolated DC sources with one having 3-fold of the voltage of the other DC source to achieve the mentioned boosting factor, resulting in high implementation complexity [13]. Moreover, several 9-level SC-MLIs was discussed in recent literature, where the best performing 9-level SC-MLI topology exhibited a THD of 9.31% and a 4-fold boosting factor with a single DC source, despite having a TSV of 5 p.u. and utilising 26 components [14]. The best performing 9-level SC-MLI in literature highlighted the potential of 9-level SC-MLIs in achieving a good harmonic profile with fewer components as it achieved a voltage THD of 9.31% with 26 components, while a 13-level SC-MLI achieve a voltage THD of 9.83% with 32 components. However, the majority of the SC-MLIs in the literature faced high TSV, including 9-level SC-MLIs. Thus, this highlights the trade-off required for achieving a topology with a high boosting factor, low voltage stress, and an optimised component count.

Apart from the development of novel topologies, various control strategies have also been highlighted in literature due to their significant effect on the output power quality and the efficiency of the inverter system. The research on various Pulse Width Modulation (PWM) strategies is driven by minimising low-order harmonics and switching loss in MLIs. PWM schemes can be categorised as high frequency switching and low frequency switching. High frequency PWM schemes enable the harmonics to be shifted to a higher frequency range, thus allowing effective filtering via an additional filter circuit. Whereas low frequency PWM schemes aim to eliminate low order harmonics [15]. Low frequency PWM schemes include Selective Harmonic Elimination Pulse Width Modulation (SHE-PWM) and Nearest Level Control Pulse Width Modulation (NLC-PWM), whereby the NLC-PWM scheme determines the switching angle by referring to a reference voltage, and the SHE-PWM scheme eliminates low order harmonics by deriving the solutions to nonlinear expressions to obtain the optimised switching duration [9, 16].

Among high frequency PWM schemes, Phase Disposition Pulse Width Modulation (PD-PWM), a branch of Level-Shifted Pulse Width Modulation (LS-PWM), was utilised in a 9-level SC-MLI topology and achieved a voltage THD of 14.64% [2]. Another branch of LS-PWM- Phase Opposition Disposition Pulse Width Modulation (POD-PWM) scheme was implemented in an 11-level SC-MLI topology and resulted in a voltage THD of 10.86% [13]. Conversely, low frequency PWM schemes such as the NLC-PWM scheme were integrated in another 9-level SC-MLI topology and achieved a voltage THD of 9.31% [14]. The SHE-PWM scheme was also integrated in a 13-level SC-MLI topology and resulted in a voltage THD of 7.02% [17]. The recent literature suggests a research gap in achieving a lower voltage THD with minimal output voltage levels by implementing an effective PWM scheme.

In addition to the design of PWM schemes, the platform used to execute switching would also affect the performance and cost of the inverter system. Research has implemented various control platforms which include, dSPACE controllers, Digital Signal Processors (DSPs), microcontrollers, as well as Field Programmable Gate Arrays (FPGAs). Each platform differs in their features and capabilities. For instance,

microcontrollers and DSPs execute low complexity programs but have limited Input/Output (I/O) pins, sampling rate, processing speed, as well as a lack of parallel processing capabilities. Therefore, recent research has integrated FPGAs as the control device owing to their parallel processing capability, greater number of I/O pins, and the customisable hardware architecture [15, 18].

Considering the ongoing trends and trade-offs in various SC-MLI topologies, the literature suggests the need to develop an optimal SC-MLI topology and an effective PWM scheme on a suitable hardware control platform to achieve a high boosting factor, minimised THD and TSV with an optimised component count. Hence, the objectives of this study are listed as follows.

- To design a novel SC-MLI topology that achieves a high voltage boosting factor and minimises the TSV with an optimised number of components and a single DC source.
- To design an efficient PWM scheme that minimises the THD of the output voltage and current.

The paper is arranged in the given order: Section 2 discusses the working principle of the proposed topology including the load current and charging current paths. While section 3 describes the research methodology which contains the design of the topology and PWM scheme. The simulation and experimental results are then discussed in section 4. Finally, section 5 concludes the article.

2. The Novel 9-Level SC-MLI Topology

A novel 9-level SC-MLI topology was proposed due to the potential of 9-level SC-MLIs in achieving a high voltage gain and low voltage THD as compared to higher-level SC-MLIs such as 13-level SC-MLIs and 11-level SC-MLIs [12-14]. It is composed of a single DC voltage source, three capacitors (C1-C3), three diodes (D1-D3), six unidirectional switches (S1-S4 and S7-S8), and two bidirectional switches (S5-S6) as shown in Fig. 1.

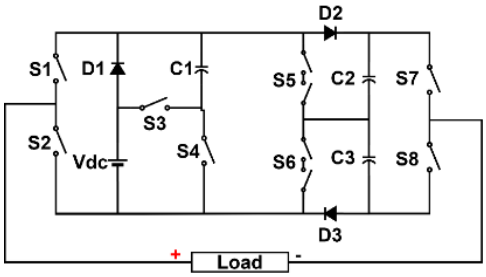


Fig. 1. Schematic of the novel 9-level SC-MLI model.

The topology charges the capacitor, C1 to a voltage magnitude of $1V_{DC}$, and the other two capacitors are charged to a voltage magnitude of $2V_{DC}$ in parallel, thus achieving a 4-fold boosting factor. The load current and charging current paths for each output voltage level are illustrated in Fig. 2, where the blue track indicates the load current path and the green track indicates the capacitor charging path. As shown in Fig. 2, there are two different load and charging current sequences for the first output voltage level ($0V_{DC}$), this is to ensure that both capacitors, C2 and C3,

are charged symmetrically at low modulation indices. As shown in Fig. 2(a), the capacitor C2 is charged via a series connection with the DC source. Whereas the capacitor C3 would be charged in the alternative sequence for the first output voltage level as illustrated in Fig. 2(b). For the second output voltage level ($1V_{DC}$), the voltage source is connected to the capacitor C3 and capacitor C2 in series in the positive and negative half cycle, respectively, while the capacitor C1 is charged in parallel simultaneously. For the third output voltage level ($2V_{DC}$), the capacitor C1 discharges by having a series connection with the voltage source and charges the capacitor C3 and capacitor C2 in the positive and negative half cycle, respectively. For the fourth output voltage level ($3V_{DC}$), the capacitor C3 and C2 discharges a voltage magnitude of $2V_{DC}$ in the positive and negative half cycle, respectively, whereas the capacitor C1 charges in a parallel connection with the DC source. Finally, two capacitors, C1 and C2, discharge in a series connection with the voltage source during the positive half cycle, and the capacitor C3 discharges during the negative half cycle for the fifth output voltage level.

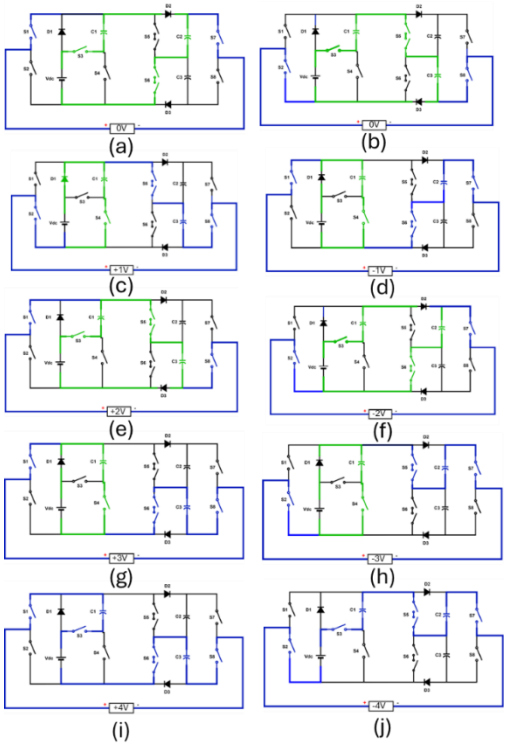


Fig. 2. Switching scheme of the novel 9-level SC-MLI model. (a) & (b) V_{output}=0V, (c) V_{output}=1V, (d) V_{output}=-1V, (e) V_{output}=2V, (f) V_{output}=-2V, (g) V_{output}=3V, (h) V_{output}=-3V, (i) V_{output}=4V, (j) V_{output}=-4V.

3. Research Methodology

As mentioned in section 1, the article would be focused on attaining two main objectives in efforts to achieve an optimal 9-level SC-MLI topology paired with an

effective PWM scheme to achieve a high boosting factor, low TSV and THD using an optimised number of components on an FPGA.

3.1. Topology design methodology

Since the first research objective is targeted towards minimising the TSV, a novel topology was developed and evaluated based on the validity of the load and charging paths according to the derived switching patterns and capacitor behaviours, including reverse current paths to ensure adaptability in combined resistive and inductive (RL) load applications. Considering that the proposed design aims to achieve a 4-fold boosting factor, the TSV of the proposed topology would be minimised by ensuring only two switches experience a MBV of $4V_{DC}$, and the majority of the switches experience an MBV of $2V_{DC}$ or lower with less than 26 components. The proposed topology was then modelled and simulated with MATLAB/Simulink to verify the successful generation of all nine output voltage levels, followed by evaluating the TSV by comparing it to the baseline study which exhibited a TSV of 5 p.u., with the use of 26 components [14].

3.2. Pulse width modulation (PWM) design methodology

The methodology of designing the PWM first focused on achieving a lower THD by integrating a high-frequency PWM scheme, specifically the Phase-Disposition PWM (PD-PWM) scheme with reduced carriers to optimise resource consumption. The output voltage THD resulted from the implementation of the PD-PWM scheme would then be evaluated based on the baseline study which exhibited a voltage THD of 9.31%. However, if the PD-PWM scheme is unable to achieve a greater harmonic profile as compared to the baseline study, a low-frequency PWM scheme, particularly the SHE-PWM scheme would be implemented to achieve a lower THD.

The PD-PWM scheme operates based on the comparison between multiple in-phase carrier signals with a modulating sine wave signal. In efforts to reduce the required carrier signals, a half sine wave signal was used instead of a full-modulating sine wave signal as illustrated in Fig. 3. The modified PD-PWM scheme used only (N-1)/2 carrier wave signals for a N-level MLI instead of the typical number of carriers (N-1). Hence, only four carriers would be utilised in the PD-PWM scheme. The amplitudes of the four triangular carrier signals are indicated as A_cr1, A_cr2, A_cr3, and A_cr4, and the modulating sine wave is indicated as V_ref. A similar approach was presented in a 17-level SC-MLI topology, where a low output voltage THD of 4.83% was achieved by utilizing (N-1)/2 carrier signals in its PD-PWM scheme where the number of output voltage levels is represented by N [19].

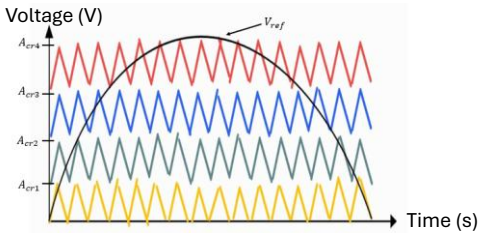


Fig. 3. Comparison between triangular carrier signals and modulating sine wave signals.

The architecture of the PD-PWM scheme includes a comparator module to generate the comparison logic which would be further utilised for producing the gate pulses by implementing a multiplexer module. After verifying the gate pulses through testbench simulations via the Quartus II Modelsim software, the Verilog program was then imported into MATLAB/Simulink with the built-in function (importHDL()) from the HDL coder library. Prior to conducting a full system level verification, the capacitor sizing was determined based on each of their Maximum Discharging Period (MDP) and the desired ripple factor. Considering that the capacitor C1, discharges when the output voltage of $2V_{DC}$ and $4V_{DC}$ are generated, and the capacitors C2 and C3, discharge in a symmetrical pattern when generating the output voltage of $1V_{DC}$, $3V_{DC}$, and $4V_{DC}$, the minimum capacitance of each capacitor was determined to achieve a ripple factor of 10% as shown in Eq. (2). The capacitor sizing was then implemented, and a full system level verification was conducted.

$$\Delta Q_{C1} = C_1 \times \Delta V_{C1} = \int_{\frac{\theta_2}{w_m}}^{\frac{\theta_3}{w_m}} \frac{2V_{dc}}{R_L} dt + \int_{\frac{\theta_4}{w_m}}^{\frac{\pi-\theta_4}{w_m}} \frac{4V_{dc}}{R_L} dt + \int_{\frac{\pi-\theta_3}{w_m}}^{\frac{\pi-\theta_2}{w_m}} \frac{2V_{dc}}{R_L} dt$$
$$= \frac{4V_{dc}}{R_L W_m}[\theta_3 - \theta_2 + \pi - 2\theta_4]$$
$$\Delta Q_{C2} = C_2 \times \Delta V_{C2} = \int_{\frac{\theta_3}{w_m}}^{\frac{\pi-\theta_3}{w_m}} \frac{4V_{dc}}{R_L} dt + \int_{\frac{\theta_1}{w_m}}^{\frac{\theta_2}{w_m}} \frac{V_{dc}}{R_L} dt + \int_{\frac{\pi-\theta_2}{w_m}}^{\frac{\pi-\theta_1}{w_m}} \frac{V_{dc}}{R_L} dt = \frac{2V_{DC}}{R_L W_m}[2\pi - 4\theta_3 + 2\theta_2]$$
$$\theta_1 = \sin^{-1}\left(\frac{A_{cr1}}{A_{ref}}\right);\ \theta_2 = \sin^{-1}\left(\frac{A_{cr2}}{A_{ref}}\right)$$
$$\theta_3 = \sin^{-1}\left(\frac{A_{cr3}}{A_{ref}}\right);\ \theta_4 = \sin^{-1}\left(\frac{A_{cr4}}{A_{ref}}\right)$$
$$C_1 \geq \frac{40}{w_m R_L}[\theta_3 - \theta_2 + \pi - 2\theta_4]$$
$$C_2 = C_3 \geq \frac{20}{w_m R_L}[2\pi - 4\theta_3 + 2\theta_2] \quad (2)$$

In the development of a low frequence PWM scheme, a Finite State Machine (FSM) alternates between five states, where each state would be alternated based on the pre-determined duration (t1-t5) for each output voltage level by having a counter to increment the duration variable at a one microsecond interval. The pre-determined duration was determined based on the optimal switching angles obtained with the use of a Genetic Algorithm (GA). The GA derived the optimal switching angles based on tournament selection, whereby several chromosomes were selected and evaluated based on the fitness equation as expressed in Eq. (3), where a_j is the order of the targeted harmonics, V_1 is the fundamental element, and V_d is the desired fundamental element.

$$fitness = \min\left\{\left(\frac{100(V_d - V_1)}{V_d}\right)^4 + \sum_{j=3}^{n} \frac{\frac{1}{a_j}\left(50Va_i\right)}{V_1}\right\} j \neq 2,4,6,8 \quad (3)$$

4. Simulation and Experimental Results

4.1. Simulation results

The novel 9-level SC-MLI topology was simulated with MATLAB/Simulink using a combined resistive and inductive (RL) load of 80Ω and 200mH, respectively. The load voltage and current waveform simulated with the PD-PWM scheme is illustrated

in Figs. 4(a) and 4(b), respectively. The load voltage waveform showed a peak voltage of 400V as the input voltage was 100V, thus justifying the 4-fold boosting factor of the proposed topology. Furthermore, a smooth current waveform was shown in the simulated output current waveform due to the presence of an RL load.

The harmonic profile of the novel topology with the PD-PWM scheme was simulated as shown in Fig. 5, where the THD of the load voltage and current is 13.45% and 0.35%, respectively. Since the THD resulted from the PD-PWM scheme is higher than the THD presented in the baseline study (9.31%), and large harmonics were shown to be concentrated at the lower order harmonics, the SHE-PWM scheme was implemented in the novel topology. The load voltage and current waveform resulted from the SHE-PWM scheme are depicted in Figs. 6(a) and 6(b), respectively. The output voltage waveform showed no fluctuations between the targeted voltage level and the previous voltage level as the voltage levels are switched based on the optimised switching durations, which in turn would lead to a lower THD value.

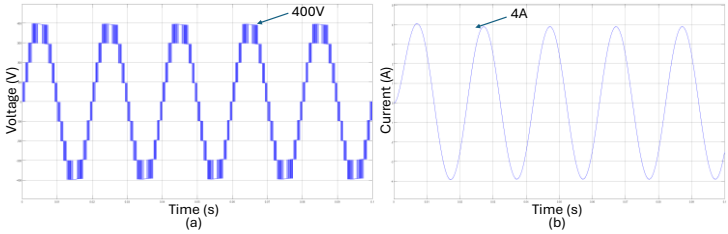


Fig. 4. Simulated output waveform with the PD-PWM Scheme. (a) Voltage waveform, (b) Current waveform.

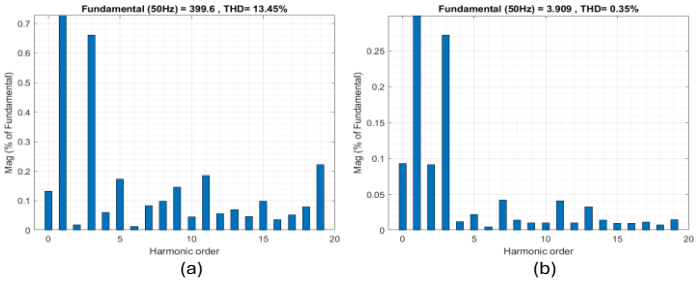


Fig. 5. Simulated harmonic profile of the PD-PWM scheme. (a) Load voltage, (b) Load current.

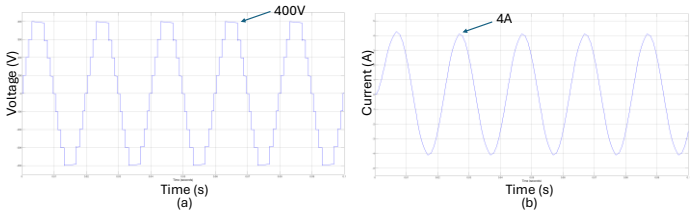


Fig. 6. Simulated harmonic profile of the SHE-PWM scheme(a) Voltage waveform, (b) Current waveform.

The harmonic analysis of the novel topology with the SHE-PWM scheme was then evaluated as shown in Fig. 7. The THD of the load voltage and current waveform was depicted to be 8.83% and 1%, respectively, which is a notable reduction in the voltage THD as compared to the voltage THD resulted from the PD-PWM scheme. Furthermore, the achieved voltage THD with the SHE-PWM scheme is 5.16% lower than the voltage THD presented in the baseline study, thus concluding that the second objective has been fulfilled.

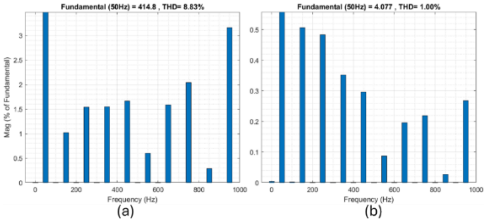


Fig. 7. Simulated harmonic profile of the SHE-PWM scheme. (a) Load voltage, (b) Load current.

Furthermore, a voltage stress analysis was conducted as shown in Fig. 8, where it showed that four switches (S1, S2, S5, and S6) experienced an MBV of 2V_DC, two switches (S3 and S4) experienced an MBV of 1V_DC, and two other switches (S7 and S8) experienced an MBV of 4V_DC. By dividing the total MBV of all switches with the 4-fold boosting factor of the proposed topology, the TSV was calculated to be 4.5 p.u., which is a 10% reduction in the TSV presented in the baseline study, thus achieving the first objective.

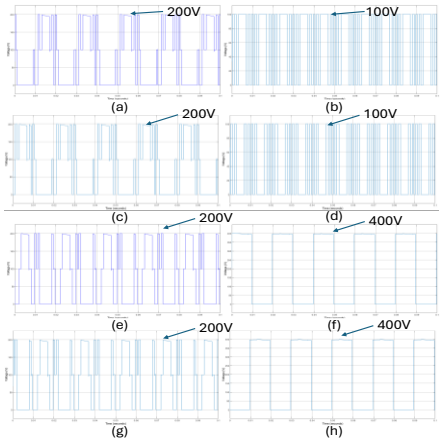


Fig. 8. MBV of all switches. (a) S1, (b) S3, (c) S2, (d) S4, (e) S5, (f) S7, (g) S6, (h) S8.

4.2. Experimental results

An experimental setup for the novel 9-level SC-MLI topology was constructed as depicted in Fig. 9. The load voltage waveform is illustrated in Fig. 10(a), where it depicts a 4-fold boosting factor as the input voltage applied in the experimental setup was 10V. The experimental setup was also tested with varying modulation

index, ranging from 0.2 to 0.95, as depicted in Fig. 10(b). The FPGA resource consumption summary also showed a low resource consumption of the total logic elements of less than 1% of the available logic elements in the FPGA, as well as 148 registers and 12 pins.

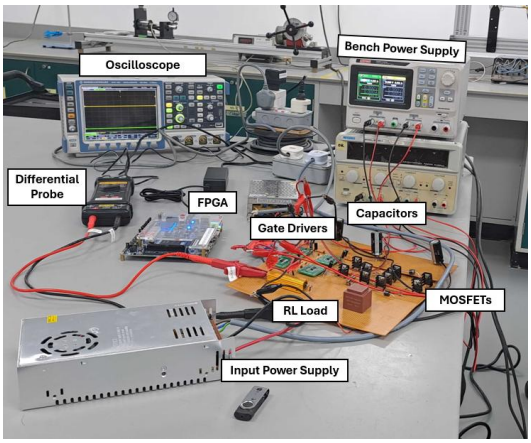
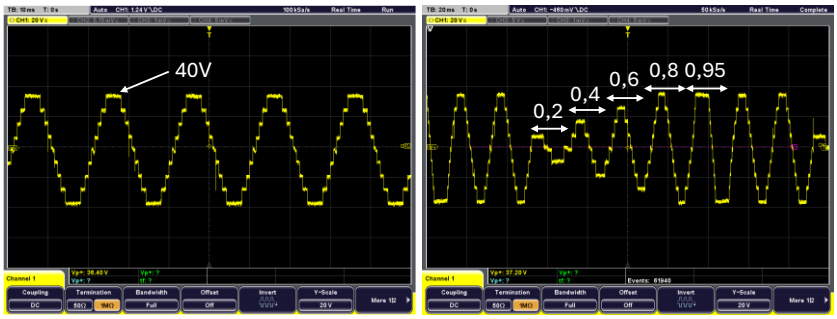


Fig. 9. Experimental setup for the novel 9-level SC-MLI model.



(a) (b)

Fig. 10. Output voltage waveform. (a) Constant modulation index, (b) Varying modulation index.

The harmonic profile of the output voltage waveform was also evaluated by parsing the load voltage waveform into MATLAB as illustrated in Fig. 11. The THD of the load voltage was shown to be 9.035%, which is 2.95% lower than the voltage THD presented in the baseline study. A voltage stress analysis was also conducted with the experimental setup, where the voltage across each switch was evaluated as shown in Fig. 12. Similar to the voltage stress analysis presented in the simulation results, four switches experienced an MBV of $2V_{DC}$, while two switches experienced a MBV of $1V_{DC}$, followed by two remaining switches experiencing a MBV of $4V_{DC}$, thus resulting in a TSV of 4.5 p.u.. The experimental results indicated that the novel 9-level SC-MLI topology achieved a low voltage stress and an improved harmonic profile in real-time with the use of an FPGA as the control platform, with an optimal resource consumption.

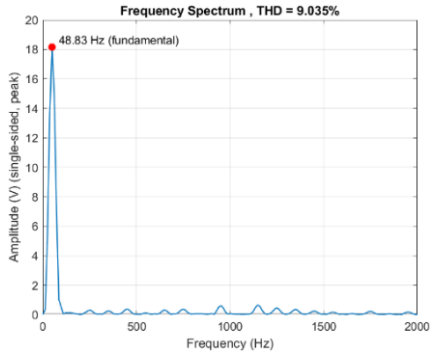


Fig. 11. Harmonic profile of the load voltage waveform.

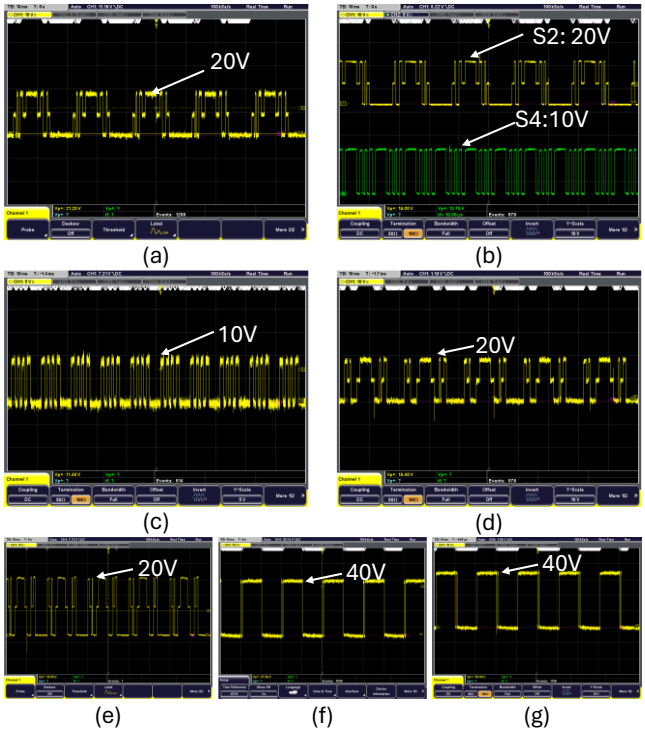


Fig. 12. MBV of all switches with experimental setup (a) S1, (b) S2 and S4, (c) S3, (d) S5, (e) S6, (f) S7, (g) S8.

A comparative analysis was conducted between the existing 9-level SC-MLI topologies and the novel topology as shown in Table 1. The existing topologies and the novel topology were compared based on the total component count (N_T), which comprises the quantity of switches (N_{SW}), quantity of gate drivers (N_{GD}), quantity of diodes (N_D), quantity of capacitors (N_{SC}), and the quantity of voltage sources (N_S). The topologies were also compared based on the Total Standing Voltage (TSV), the boosting factor (β), and the voltage THD. The proposed topology presented the lowest voltage THD and TSV as well as a 4-fold boosting factor by implementing only 25 components.

Table 1. Comparative analysis between existing 9-level topologies and the novel topology.

Ref	N_{SW}	N_{GD}	N_D	N_{SC}	N_S	N_T	TSV	β	THD (%)
[20]	12	12	1	3	1	29	5.75	4	12.80
[16]	10	9	1	3	1	24	5.50	4	10.00
[21]	9	9	1	2	1	22	5.25	4	14.64
[14]	11	11	1	2	1	26	5.00	4	9.31
Proposed	10	8	3	3	1	25	4.50	4	8.83

5. Conclusion

The proposed 9-level topology utilised 25 components and achieved a 4-fold boosting factor and a TSV of 4.5 p.u. which is a 10% reduction in the TSV presented in the baseline study. Through the implementation of the SHE-PWM scheme, a voltage THD of 8.83% was achieved in the simulation results, thus improving the harmonic profile by 5.16% as compared to the baseline study. An experimental setup of the proposed 9-level topology was constructed with a combined resistive and inductive load of 80Ω and 10mH, respectively. The experimental results presented a TSV of 4.5 p.u. alongside a voltage THD of 9.034%. Additionally, the SHE-PWM scheme utilised fewer than 1% of the total logic resources, followed by 148 registers and 12 pins. Results showed that the proposed topology was functional under varying modulation index, thus justifying the potential of the novel topology in motor drivers and industrial power supplies.

A comparative analysis of the existing topologies and the novel topology indicated that the proposed topology achieved the lowest TSV and voltage THD by using only 25 components. Owing to the high boosting factor, low voltage stress, and low THD of the single-source novel topology, it can be integrated into renewable energy systems and omitting the necessity of costly DC-DC converters. Therefore, contributing to the advancement of MLI research and supporting global sustainable goals. Further research will explore the potential of refining the architecture of the GA model in the SHE-PWM scheme to further enhance the harmonic profile of the novel topology.

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Nomenclatures

N	Quantity of output voltage levels
N_D	Quantity of didoes
N_{GD}	Quantity of gate drivers
N_S	Quantity of voltage sources
N_{SC}	Quantity of capacitors
N_{SW}	Quantity of switches
N_T	Total component count
p.u.	Per unit
V_{DC}	Input DC voltage

$V_{Peak,Out}$	Boosted output voltage

Greek Symbols

β	Boosting factor
θ	Optimised switching angle, rad

Abbreviations

AC	Alternating Current
CHB	Cascaded H-Bridge
DC	Direct Current
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
EV	Electric Vehicle
FC	Flying Capacitor
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GA	Genetic Algorithm
I/O	Input/Output
MBV	Maximum Blocking Voltage
MDP	Maximum Discharging Period
MLI	Multilevel Inverter
NLC	Nearest Level Control
NPC	Neutral point Clamped
LS	Level-Shifted
PD	Phase Disposition
POD	Phase Opposition Disposition
PWM	Pulse Width Modulation
SC	Switched Capacitor
SHE	Selective Harmonic Elimination
THD	Total Harmonic Distortion
TSV	Total Standing Voltage

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