LOW POWER AND IMPROVED SPEED
1T DRAM USING DYNAMIC LOGIC

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Abstract

The new trend of the DRAM design is to characterize by its reliability, delay, low power dissipation, and area. This paper dealt with the design of 1-bit DRAM and efficient implementation of a sense amplifier. The proposed 1-bit DRAM designed using dynamic logic design. The proposed circuit consists of buffers, 1 transistor, and capacitor. The circuit is schematized by DSCH2 and layout designs are generated by Microwind CAD tool. The designed and proposed circuits are considered bypass logic and Boolean reduction technique that reduced number of transistors per designed cell logic. The circuits are simulated in various feature sizes namely CMOS 70 nm, CMOS 90 nm, CMOS 120nm and corresponding voltages 0.7 V, 1 V, 1.2 V respectively. Our proposed dynamic logic DRAM circuit has compared with the designed circuit and other existing circuits. Our proposed and designed circuit gives better results in terms of power dissipation, speed, and Area. (R-2) The projected 1-bit DRAM has an outcome and achieved low power 0.229 μW, the area of $22\times13\mu m$, the propagation delay of 21 ps and a speed of 0.17 GHz.

Keywords: DRAM, Dynamic logic, Low power and speed, Propagation delay.

1. Introduction

The DRAM is a device, which stores their contents as a charge on a capacitor, rather than in a feedback loop. DRAM has higher integration density and small cell area compared to SRAM. In VLSI circuit design, clocked logic (dynamic logic) is a design methodology in combinatorial logic circuits, particularly those implemented in PTL technology. It is distinguished from the static logic by exploiting temporary storage of information in stray and gate capacitances. The manufacturing cost of

Nomenclatures

B_L	Bit line
C_{BL}	Bit line capacitor
C_S	Cell capacitance
D_{in}	Input data
I_{LEAK}	Leakage current
V_{BL}	Bit line voltage
V_{out}	Output voltage
V_{SI}	Stored voltage
V_{TN}	N-channel threshold voltage

Greek Symbols

β_N	Current gain
τ_N	Storage delay

Abbreviations

BSIM	Berkeley Short-Channel IGFET Model
CPU	Central Processing Unit
DRAM	Dynamic Random Access Memory
tDQSCK	DQS Rising Edge Output Access Time from the Rising Edge of CK

each storage cell is cheap. DRAM has the much larger capacity per unit of surface than SRAM. It is usually used for main memory because of its low manufacture cost. Structurally, SRAM requires a lot more transistors in order to accumulate a certain quantity of memory [1]. A DRAM unit only requires a transistor and a capacitor for every bit of information where SRAM requires 6 transistors because the number of transistors in a memory unit states its capacity. In a DRAM unit, dynamic random access memory (DRAM) is the type of random access memory (RAM) generally used for personal computers and workstations.

In this memory, the arrangement of electrically stored points is used to store the data in the form of 0s and 1s. In Random access memory, the central processing unit (CPU) can access any element of the memory straight rather than having to keep in sequence from some starting place. In a DRAM storage cell, a capacitor and a transistor [2] are used to store each bit. The refreshing is done to avoid the charge loss in capacitors. Several approaches are reported for DRAM commonly known as the memory schemes. The memory schemes are based on 1-bit DRAM cell. This paper dealt with minimizing transistor size. For that new proposed 1-bit DRAM, this can be used as a core element of memory devices. Earlier research has paid attention to minimizing area and delay in DRAM circuit.

There are two kinds of DRAM design such as storage elements and sleep transistor based DRAM design [3]. This paper deals with storage element DRAM and sleep transistor based DRAM. The sleep transistor based DRAM based on 3T and designed by Boolean reduction technique. The proposed technique is designed depends upon charging and discharging based on the word line and bit line [4]. This kind of design faster than dynamic memory cell due to activate on a word line. The designer of dynamic storage elements DRAMs is designed based on word line

logic. Our proposed techniques based on PTL and dynamic logic. The dynamic logic reduced transistor per logic.

In this proposed paper, we have intended a two kind of DRAM and implemented into sense amplifier circuit. These circuits are validated by BSIM4. These proposed DRAMs are implemented into 4-bit DRAM and application circuit such as sense amplifier circuit. The analyses of parametric characteristics such as power dissipation of the chip, propagation delay, operating frequency are studied from outline simulations of BSIM 4. This paper mainly focused on improving the speed of minimum power and area. By taking into account, the power is considerably reduced in the dynamic logic DRAM circuit. The content of the paper is prepared as follows:

- Section II: explains the related works and underlying prompt behind our design.
- Section III: describes the design method.
- Section IV: presents outcomes and discussion, and
- Section V: states the conclusions the paper.

2. Related Works

According to Joseph and Ravindran [5], the DRAM design has oxide type resistive part added for non-volatile operation. The author proposed two non-volatile DRAM cells, such as the threshold voltage for the refresh operation. The HSPICE simulation is used to find the impacts of the non-volatile circuitry. The critical charge and the area of cell layout are established for both volatile and non-volatile DRAM cells as well as memory arrays.

Minjie et al. [6] proposed to create the DRAM array unlock its spare to off-chip access by adjusting the minimized architecture and improve the design of defective address comparison and the remapping redundant address by means of an efficient architecture on logic die to achieve equal memory repair. Three-dimensional (3D) integration is capable to provide better performance and energy efficiency improvement to 3D logic DRAM integrated computing system. This paper explores a way to control logic DRAM code sign to reactivate unused spares and thereby enable the cost-efficient technique to repair 3D integration induced defective DRAM cells after die stacking. Specifically, the Simulation results show that the projected repair technique for stacked DRAM can improve potential yield loss, minimum area and power consumption overhead and negligible timing effect.

Lee et al. [7] paper, Delay Locked Loops (DLLs) of analog-based topologies are analysed in Dynamic Random Access Memory (DRAM). The analysis of this paper starts with an explanation of technology trends concerning DLL for DRAM in the early 1990s and explains the significant DLL specifications and design approaches necessary for DLL use in DRAM: lock time, lock range, lock cycles, tDQSCK (DQS rising edge output access time from the rising edge of CK), and wake-up time from power down modes. Finally, this paper referring to studies published from 2000 to 2011, trends regarding power consumption, jitter, the relationship between power and jitter, lock range, clock cycles, and wake-up time from power down are analyzed.

According to Singh and Somkuwar [8], proposed Memory circuits are extremely regular that is increased of chip complexity. The significant features namely low power, reliable performance, circuit techniques for high speed by using dynamic

circuits, and low leakage current, these will give a better advantage. This paper gives a suggestion about 4T DRAM (dynamic random access memory) which is implemented by means of a self-controllable voltage level technique. This technique reduces the leakage current and increases the performance.

Simulation is done by using a Micro wind 3.1 and DSCH3, 90 nm technologies to implement a 4T DRAM, which gives the benefit of 67% reduction in leakage current. This reduction gives an advantage of high performance and low leakage current, by controlling the parameter speed is automatically increases.

According to 4×4 Dynamic RAM design principle, the row and column operation logic is shown in Table 1. According to a clock signal, the signal is passing to PMOS transistor. The PMOS transistor output feeds into NMOS transistor source. The NMOS transistor gate input is WL logic. According to PMOS and NMOS dynamic logic operation, the word logic and bit logic are activated in the 4 ×4 bit DRAM cell. (R-2) When row R1 is active for the column values of C2 and C4. Similarly, for the other rows will take the respective column values. Table 2 is illustrating the column and ROW cell of the transistor actions.

Table 1. Related works.

Ref.	Paper	Study description	Purpose	Results
[5]	Implementation of non-volatile 4×4 4T1D DRAM cell in 0.18 μm technology	Two non-volatile DRAM cells	Made non-destructive read and longer retention time	Area increases, power dissipation is 941.88 μW and delay is 1.350ns
[6]	Logic-DRAM co-design to exploit the efficient repair technique for stacked DRAM	Enhanced 3-D DRAM	Achieved potential yield loss	The compound yield changed from 72.35% to 91.27%
[7]	A 1.6 V 1.4 Gbp/s/pin consumer DRAM with self-dynamic voltage scaling technique in 44 nm CMOS technology	DLL based DRAM cell	Adaptive dynamic voltage scaling for SDRAM	When supply voltage becomes below 300 mv then the life time of the IC increases 23 times than the conventional
[8]	Used self-controllable voltage level technique to reduce leakage current in DRAM 4×4 in VLSI	Self-controllable voltage level technique DRAM	Reduces the leakage current	Leakage current reduces by 37% to conventional.

Table 2. Row and column operation of 4×4 DRAM [14].

R1	R2	R3	R4	C1	C2	C3	C4
1	0	0	0	0	1	0	1
0	1	0	0	0	0	1	1
0	0	1	0	1	0	0	1
0	0	0	1	0	1	1	0

3. Design Method

In the contemporary DRAM chip, several smaller memory arrays are structured to achieve a larger memory size. For instance, 1,024 smaller memory arrays, each consist of 256 kilobits, may constitute a 256-Mega (256 million bits) DRAM. To read a data R/W pin is HIGH and the chip enables pin "CE" is in the LOW state. To write a data R/W pin is LOW with valid data present on the D_{in} pin.

The DRAM is always in need to refresh internally. To restore the DRAM, we from time to time have to access the memory with every feasible row address arrangement. This paper contains two kinds of the DRAM, which is based on the cell that has two Word Lines (WLs) and two Bit Lines (BLs) for reading and store operations accordingly. The DRAM circuits have designed by Boolean identities and pass transistor logic, which gives transistor reduction and higher performance. The basic block of DRAM design cell is shown in Fig. 1.
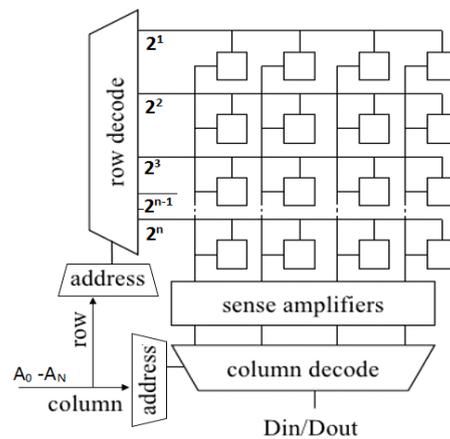

Fig. 1. Block diagram of DRAM design cell.

3.1. 3T Dynamic memory cell

3T DRAM utilizes gate of the transistor and a capacitance to store the data value. When writing the date, write signal should be activated and the bit line data is available in the cell. When reading the data, read line is activated and data is read through the bit line.

In dynamic random access memory (DRAM), a split capacitor inside a built-in circuit supplies every bit of data. During pre-charge contention will take place, because both PMOS and NMOS transistor will be ON. The input WWL cannot be guaranteed to be logic "0" during pre-charge [9]. Therefore, we have to add NMOS transistor to avoid contention. The newly added footed transistor is used to estimate the logical effort. The charging or discharging of the capacitor is represented as logic "1" and logic "0". The capacitor charge is to be refreshed periodically; because of the capacitor discharging effect. The design of Dynamic 3T RAM cell is shown in Fig. 2.

3.2. 3T DRAM sleeping mode

This paper design and the analysis of DRAM logic compatible 3T cell as shown. The designed and proposed 3T DRAM is universally used by the advanced processor for on-chip data and program memory due to its high density and low cost of memory.

This projected sleep transistor 3T DRAM circuit contains two voltage supplies, which are connected to B_L and respectively [10]. Switching of the main transistor is done by W/L, which is at a logic low level for write function and logic high level for read function. The simulation results carried out for different voltage levels from 0.7 V to 1.3 V, and then it is noted that low voltage operation is appropriate for low slew rate or low read access time. If the operating voltage increases, then the leakage current decreases. The 3T sleeping mode DRAM is shown in Fig. 3.
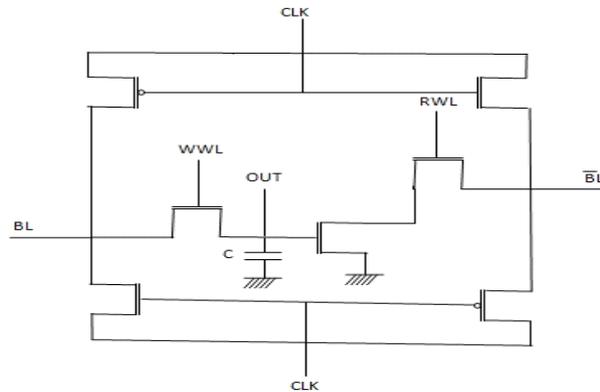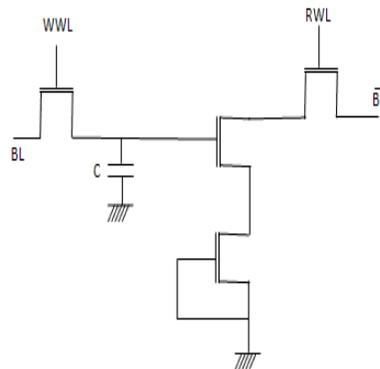

Fig. 2. 3T Dynamic memory cell.

Fig. 3. 3T Sleeping mode DRAM.

3.3. 4T DRAM

The 4T DRAM cell is shown in Fig. 4. According to the circuit arrangement, the left side transistor is used as a write transistor, the right side transistor assumes to be a read transistor. The bit lines are connected as a source input of write/read transistors [11]. The data is stored in the DRAM in the form of charge at the capacitor, which is attached to the storage transistor. According to input, the current will flow through the drain of the transistors. The storage node draws no current for restoring the data when a word line is at logic 0. It leads to drop off-leakage current thereby data loses.

The dynamic RAM memory has a better density in the memory matrix because it uses only one transistor instead of using 6 transistors in SRAM. In the design of

1T DRAM, the analysis is explained in terms of the first-order model. According to charging sharing theory, the resultant bit line voltage upon closure of the transistor is:

$$V_R = \frac{Q_T}{C_T} = \frac{C_{BL}V_{BL} + C_S V_{S1}}{C_{BL} + C_S} \qquad (1)$$

The bit line voltage changed after the switch closure. The changing signal must be amplified. The change in bit line voltage can be expressed in Eq. (2).

$$\Delta V = V_R - V_{BL} = \frac{V_{S1} - V_{BL}}{1 + \dfrac{C_{BL}}{C_S}} \qquad (2)$$

where V_{S1} is the stored voltage level representing as one, V_{BL} is bit line voltage, C_{BL} is total bit line capacitance, C_S is cell capacitance and is changed signal due to bit line voltage.
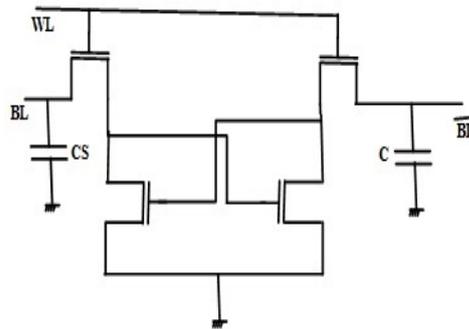

Fig. 4. 4T DRAM cell.

3.4. IT-Dynamic RAM

The dynamic cell is chosen for a read/write function by asserting its word line high (S = 1). This connects the storage capacitance to the bit line. The write function is done by the contact transistor saturated and non-saturated mode of operations by substituting either high voltage or low voltage to the bit line [12]. The column voltage switches to either '1'or '0' during the read function. The sense amplifier is used to improve the difference of this voltage levels. Note that the read function spoils the charge stored on the storage capacitance C1. Therefore, the data must be refreshed every time the read function is done.

The Dynamic 1-bit DRAM cell is shown in Fig. 5 (R-2). The bit line has the information; the storage capacitor C_S is charged to logic"1" when the word line is activated. Deactivating the write line, the storage capacitor remains same in the logic "1". The reading cycle is disparaging for the stored information so that the C_S holds logic "1". The pre-charging of a B_L voltage is VP (V_{DD} /2). When the write line is high, the bit lines are connected together and the charges are mutually shared between these nodes.

Due to this, there is a small increase of the voltage VP by ΔV. There is a small decrease in the pre-charge voltage of VP-ΔV when the C_S holds a zero. In summary, for logic "1", the bit line voltage is VP + ΔV and for logic "0", the bit line voltage is VP- ΔV.
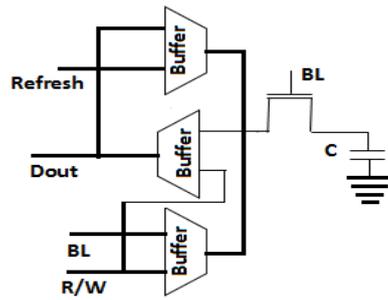
Fig. 5. Dynamic 1-bit DRAM cell.

The design of the 1T DRAM design analysis is explained in terms of first order model. According to charging sharing theory, the resultant bit line voltage upon closure of the transistor is expressed in Eq. (3).

$$V_R = \frac{Q_T}{C_T} = \frac{C_{BL}V_{BL} + C_S V_{S1}}{C_{BL} + C_S} \tag{3}$$

The change bit line voltage after the switch closure is shown in Eq. (4). The changing signal must be amplified by source voltage. The change in bit line voltage can be expressed as:

$$\Delta V = V_R - V_{BL} = \frac{V_{S1} - V_{BL}}{1 + \frac{C_{BL}}{C_S}} \tag{4}$$

where V_{S1} is the stored voltage level representing as one, V_{BL} is bit line voltage, C_{BL} is total bit line capacitance, C_S is cell capacitance and is changed signal due to bit line voltage. Either logic "0" or logic "1" and D_{in} by asserting it low or high respectively depends upon the WL, the value is stored the value in the memory cell. The read /write values are high, to activate the read unit. When NMOSFET gets logic "1", the drain terminal flow of charge-discharge from the capacitor, which gives it to the indicator.

3.5. 4×4 IT dynamic DRAM

Memory arrays are generally large and need to optimize their cell design for area and performance [13]. In the 4×4 IT dynamic DRAM, the dynamic footed logic is used to construct the 4×4 memory array.

When a global clock signal input is logic "1", the upper PMOS transistors are logical "0" and the output of NMOS transistors retrieve the previous information, which is already available in the capacitor. When global clock signal input attains skew values, the upper PMOS transistors are logical "1" which are stored based on the input values. The refresh, make it high, the capacitor refreshes the logic cell and memory cell continuously up to refresh is dropped to low. To activate a memory

cell by selecting R/W input. For example, to activate first memory cell (1, 1), R/W1 and Row 1 signals are activated. The 4×4 1T dynamic DRAM is shown in Fig. 6.
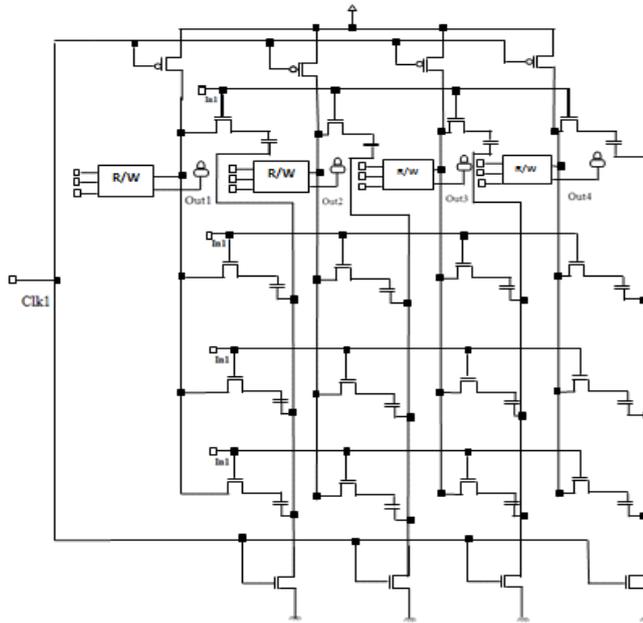

Fig. 6. 4×4 1T dynamic DRAM.

3.6. Design method of the sense amplifier

The sense amplifier is the most critical circuit in the design of sense amplifier there is a common design problem, that is:

- maintaining high performance in spite of reducing biasing voltage
- maintaining sufficient sensitivity and
- reducing the chip size.

According to our proposed dynamic logic, the based design would satisfy above-mentioned condition. The charge transfer is designed for NMOS DRAMS with bit line pre-charged to ground. Here, the NMOS transistor working as an amplifier of individual circuit. However, this approach is not extendable to VCC/2 CMOS DRAMS. The proposed circuit has implemented into replication circuit of sense amplifier circuit, which is shown in Fig. 7. (R-4). There are three major functions in sense amplifier.

- It senses the small change in potential voltage, which is stored in the capacitor.
- It restores the capacitor cell voltage which is sensed and amplified in the bit line.
- It is also used as a short-term data storage element.

The sense amplifier is designed for dynamic CMOS logic. This sense amplifier designed by ROW of transistor and column transistor, which shows the read and B_L of the DRAM circuits. This row circuit is fully different from SRAM. Each and every row of bit design capable to store a bit, which is used a read/write form of the bit. The design of the sense amplifier is implemented by 1-bit DRAM cell. The standard aspect ratio is given in the design of design.

4. Results and Discussion

In this paper, each design was tested using two levels of simulation. At first, the designs were simulated for schematic design following their respective truth table using DSCH2 CAD software. Secondly, each design's layout was generated for layout versus schematic tests to analyze its performance as VLSI design using Microwind2 layout editor. Furthermore, a comparative analysis of the proposed full adder design has also been shown with other full adder designs with respect to power, current, and Power Delay Product (PDP). As per design methodology, a test bench was created for each design and the designs were verified using known input values following their respective truth tables.

All the simulations of the designs were carried out in two levels, at first, the schematics were simulated for test bench verification and the secondly the layout verification for the power and voltage versus time response. Furthermore, a comparative analysis of the proposed full adder design with other full adder design has also been shown in this section.
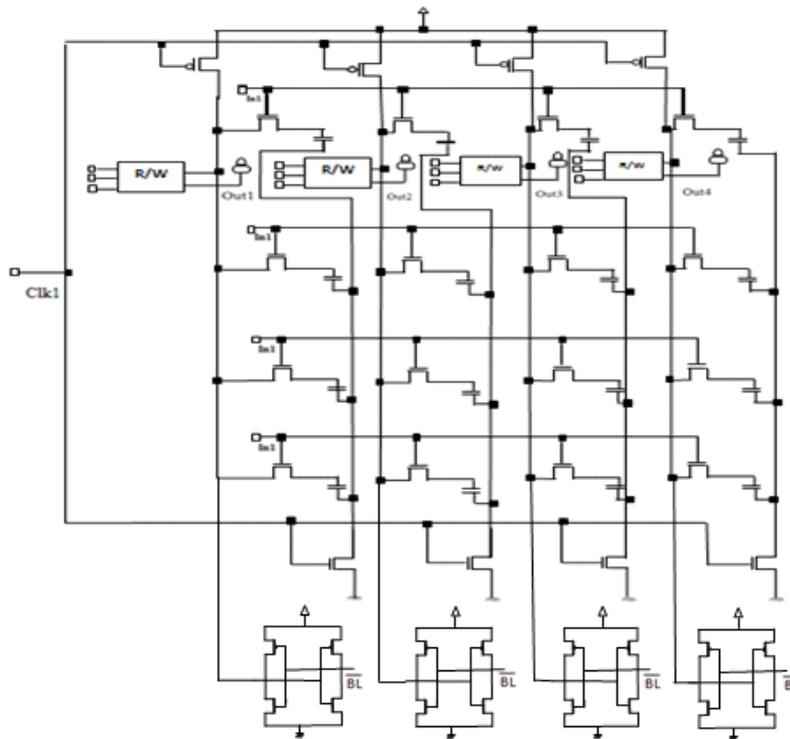

Fig. 7. 4×4 1T Dynamic DRAM with sense amplifier.

4.1. Proposed 1T DRAM

This is circuit has designed by dynamic logic design, which consists of function design placed in middle govern with PMOS and NMOS transistor. The proposed 1T DRAM timing diagram is shown in Fig. 5. The temporary storage of DRAM

circuit depends on the signal values on the capacitance at high impedance nodes and it requires n + 2 transistors:

$$V_{s(t)} = (V_{DD} - V_{TH}) \left(\frac{t/2\tau s}{1 + t/2\tau s} \right)$$ (5)

The logic inputs to the designed 1-bit DRAM circuit can make at most one transition during evaluation.

$$\tau_s = \left(\frac{C_S}{\beta_n (V_{DD} - V_{Tn})} \right)$$ (6)

$$V_s(t) = V_s(0) \left(\frac{2e^{-t/\tau_S}}{1 + e^{-t/\tau_S}} \right)$$ (7)

The proposed 1-bit DRAM is simulated by various feature size namely 120 nm, 90 nm and 70 nm and corresponding voltage are 1.2 V, 1 V and 0.7 V respectively. The simulation results of 1 T DRAM, 4×4 bit DRAM, and sense amplifier circuits are analysed based on power dissipation, area, propagation delay, throughput, and Latency. The designed circuit simulation results are in Table 3.

The designed circuit sense amplifier circuit output voltage is varying with the input voltage. Other designed circuits are changing depends upon layout capacitance values. (R-4) The current mirror effect of sense amplifier circuits is maintaining the logical level, which gives the linear growth effect in sense amplifier DRAM circuit. According to Eq. (8), the hold time of the DRAM cell is calculated.

$$t_H = \left[\frac{C_S}{I_{LEAK}} \right] (V_{MAX} - V_1)$$ (8)

The DRAM input voltage versus output voltage is shown in Fig. 8. The output voltage measured from the layout for corresponding applying input voltage. The inputs are fed into logic transition. The DRAM simulation voltages versus output voltages are also shown in the Fig. 8.

The parametric study of voltage versus power dissipation of the designed circuit is shown in Fig. 9. The transient power consumption of the designed DRAM cell results from currents flowing within the device when internal transistors switch states during operation.

The internal layout switching currents required to charge the internal nodes and the shoot-through or layout currents that flow through a DRAM device when both p-channel and n-channel transistors conduct a current during switching. The operating frequency has measured by switching event rise and fall times of the switching signals, which has a direct effect on the transient power dissipation.

Table 3. Simulation results of designed circuits.

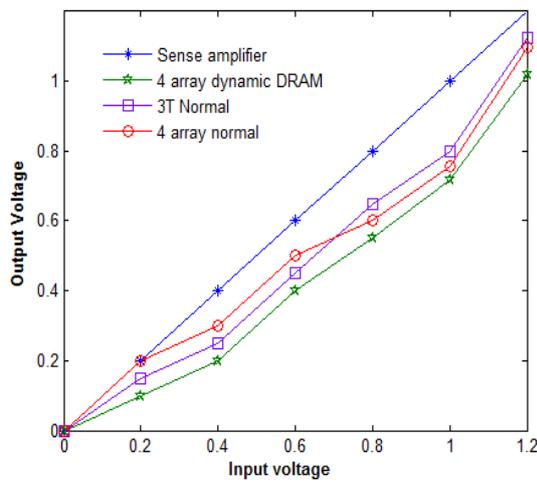|	Para Meter	Output voltage (V)	Average current (mA)	Power dissipation (μW)	Frequency (MHz)	Delay (PS)	Area (μm²)
120 nm	1T D	0.9	0.143	0.422	170	995	286
	4×4	0.83	0.09	0.286	250	62	598
	S.A	0.83	0.021	0.144	250	31	1862
90 nm	1T D	1	1.111	0.064	130	20	180
	4×4	0.63	0.074	0.096	250	528	1005
	SA	0.6	0.163	0.098	250	518	1376
70 nm	1T D	0.96	0.184	0.111	400	11	190
	4×4	0.88	0.195	0.151	250	14	1088
	SA	0.82	0.028	0.154	250	60	1602

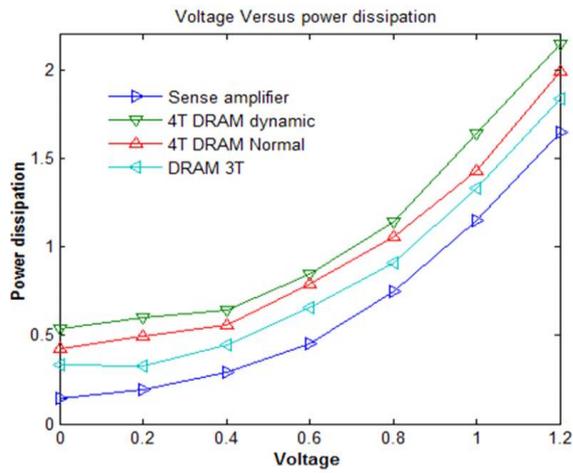**Fig. 8. DRAM input voltage versus output voltage.**

Fig. 9. Supply voltage versus power dissipation.

The internal layout switching currents required to charge the internal nodes and the shoot-through or layout currents that flow through a DRAM device when both p-channel and n-channel transistors conduct a current during switching. The operating frequency has measured by switching event rise and fall times of the switching signals, which has a direct effect on the transient power dissipation.

The shoot-through currents are small compared to the switching currents required to charge the internal nodes for fast rise and fall times. Our designed and proposed circuit reduced the switching node in dynamic logic design technique. According to dynamic power dissipation, the capacitance values increased and power dissipation values increased exponentially. The capacitance current is calculated first order equation, which is shown in Eqs. (9) and (10).

$$I = C_{OUT} = \left(\frac{dV_{out}}{dt} \right) = \left(\frac{\beta_n}{2} (V_{DD} - V_{OUT} - V_{TN}) \right)^2 \tag{9}$$

$$V_{OUT}(t) = (V_{DD} - V_{Tn}) \left(\frac{t/2\tau_n}{1 + (t/2\tau_n)} \right) \tag{10}$$

The operating frequency has measured by switching event rise and fall times of the switching signals, which has a direct effect on the transient power dissipation.

The shoot-through currents are small compared to the switching currents required to charge the internal nodes for fast rise and fall times. Our designed and the proposed circuit is reduced the switching node by dynamic logic design technique. According to dynamic power dissipation, the capacitance values increased and power dissipation values increased exponentially.

4.2. Comparison circuit

Our proposed circuit characteristics such as power dissipation, delay, area, throughput, and latency are analysed with various existing circuits such as 3T DRAM, 3T DRAM sleep transistor, 4 T DRAM circuit. Our designed and proposed circuit gives better performance than the other existing circuits. Comparison Table 4 shows an improved percentage of reduction.

The existing author circuit is designed in the same version of the software and simulated in same feature size. According to analyses, our proposed circuit is given output voltage 53.76% improvement than 3T dynamic DRAM, 1.07% than 3T DRAM and 2.15% than 4T DRAM cell.

Our proposed circuit is designed based on dynamic logic, which is reducing the number of transistor and logic path. Our proposed dynamic logic design gives lower power dissipation compared than 3T DRAM cell, 3T Dynamic DRAM and 4T DRAM cell due to logic transitions in the transistor circuit is reduced due to the number of connection node decreased.

According to power dissipation formula, the parasitic capacitances are reduced in our proposed design. Therefore, the active capacitance is less, which gives higher switching activities. Due to the equal tree structure of design, the speed of DRAM cell is increased.

Based on the simulation results, our proposed circuit gives better improvement than 3T dynamic RAM 57.5% and 68.75% than 3T DRAM and 57.5% than 4T DRAM cell. This is clearly shown in Table 4.

Table 4. Comparison tables.

	1 Bit DRAM proposed	3T D. DRAM	3T DRAM	4T DRAM	4×4 DRAM	Sense amplifier
Output voltage	0.96	0.88	0.92	1.2	0.88	0.82
% of reduction	---	53.76%	1.07%	2.15%	10.75%	10.75%
Average Current	0.184	4.534	3.273	1.012	0.90	1.021
% of reduction	---	46.73%	26.21%	39.80%	12.26%	11.85%
Power dissipation	2.422	22.9	44	212	286	144
% of reduction	---	89.42%	94.49%	98.85%	25.87%	49.65%
Frequency	400	170	125	170	250	250
% of reduction	---	57.5%	68.75%	57.5%	37.5%	37.5%
Delay (ps)	11	21	2000	1000	14	60
% of reduction	---	47.61%	99.45%	98.9%	21.42%	81.66%

5. Conclusions

This paper proposed 1-bit DRAM and sense amplifier circuit with reduced transistor count, power and delay. The DRAM has been designed using the dynamic CMOS based 4-transistor XOR model. The design has been simulated at the lower voltage at room temperature using 70nm technology. The design has achieved enhanced driving capability and faster operation with slightly more power consumption in comparison to other existing circuits. The driving capability mainly depends on a capacitor and the capacitor effectively retrieves the stored information without any soft errors. Although full voltage swing was not achieved unlike the 4T model, the circuit is well enough for energy efficient logical operation and can be used as part of very large logical operations.

In spite of degradation in the output voltage at some input conditions, it was still outperformed many proposed designs in terms of speed, power, and computational complexity. The area-weighted energy consumption of the proposed design is also superior in comparison to other higher gate count DRAM designs. Moreover, the proposed design is fully functional at extremely low supply voltage with very little degradation at the output voltage. Furthermore, the proposed DRAM design has been implemented in to sense amplifier circuit to further reduce power consumption and delay for a more optimized hardware implementation.

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