

DESIGN OF LOW EPI AND HIGH THROUGHPUT CORDIC CELL TO IMPROVE THE PERFORMANCE OF MOBILE ROBOT

P. VELRAJKUMAR*, C. SENTHILPARI, G. RAMANAMURTHY, EK WONG

Faculty of Engineering and Technology, Multimedia University, Melaka, Malaysia

*Corresponding Author: p.velraj Kumar@mmu.edu.my

Abstract

This paper mainly focuses on pass logic based design, which gives an low Energy Per Instruction (EPI) and high throughput COordinate Rotation Digital Computer (CORDIC) cell for application of robotic exploration. The basic components of CORDIC cell namely register, multiplexer and proposed adder is designed using pass transistor logic (PTL) design. The proposed adder is implemented in bit-parallel iterative CORDIC circuit whereas designed using DSCH2 VLSI CAD tool and their layouts are generated by Microwind 3 VLSI CAD tool. The propagation delay, area and power dissipation are calculated from the simulated results for proposed adder based CORDIC cell. The EPI, throughput and effect of temperature are calculated from generated layout. The output parameter of generated layout is analysed using BSIM4 advanced analyzer. The simulated result of the proposed adder based CORDIC circuit is compared with other adder based CORDIC circuits. From the analysis of these simulated results, it was found that the proposed adder based CORDIC circuit dissipates low power, gives faster response, low EPI and high throughput.

Keywords: Robot, CORDIC, EPI, Throughput, BSIM4.

1. Introduction

The autonomous mobile robot's basic feature is the capability to operate independently in unknown environments. Soft computing technologies were used to design a robust autonomous mobile robot control system, which is suitable for online applications with real-time requirements [1]. The robotic system's applications require a real-time operation to interface speed constraints is one of the major trends in current robotic research. It is essential to perform a large amount of computation at high speed because the robot must respond quickly to

Nomenclatures

P_D	Power dissipation, μW
T_A	Ambient temperature, $^{\circ}\text{C}$
T_J	Junction temperature, $^{\circ}\text{C}$
T_{JMAX}	Maximum junction temperature, $^{\circ}\text{C}$

Greek Symbols

θ_{CS}	Case-to-heat sink thermal resistance, K/W
θ_{JA}	Junction-to-ambient thermal resistance, K/W
θ_{JC}	Junction-to-case thermal resistance, K/W
θ_{SA}	Heat sink-to-ambient thermal resistance, K/W
τ	Propagation delay, ps

the environmental movement [2]. An area-efficient hardware directed solution were developed by Vachhani et al. [3] by using CORDIC algorithm.

Volder [4] originally proposed CORDIC algorithm and later Walther [5] generalized CORDIC for computation of logarithms, exponentials and square-root functions along with the trigonometric functions like sine, cosine and arctangent. This algorithm attracts more and more attention in elementary function evaluation and signal processing applications [6, 7]. The advances in VLSI technology have extended the application of CORDIC algorithm to the field of biomedical signal processing [8], Neural networks [9] and robotic exploration [3] to mention a few.

In the present paper, an adder cell is proposed and implemented into bit-parallel iterative CORDIC circuit. Our proposed CORDIC cell is designed using PTL technique. This paper describes the design of proposed adder and CORDIC cell for robotic applications. CORDIC circuit is designed using VLSI CAD tool such as DSCH2 for schematic and Microwind 3 for layout design. The proposed adder based CORDIC cell simulated and the results are compared with other published adder based CORDIC cell in terms of power dissipation, propagation delay, EPI and throughput. Based on the simulation results, our proposed adder based CORDIC circuit gives better performance in terms of delay, power, EPI and throughput, compared to other adder based CORDIC circuits.

2. Design Method

The main concept behind this design is reduced the EPI, power, delay, improving speed and high throughput. The pass logic design is better suitable to improving aforesaid for small scale circuit. The CORDIC circuit mainly used in robotic for rotation of arm, neck, eye and movements which should be in faster response within allotted time. A PTL circuit can be designed using any of tools which gives flexibility, contributes to a low design cost and encourages regular and easily automated layout styles.

2.1. Proposed full adder design

The full adder performs computing function of the CORDIC. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input

bits that consists of three inputs and two outputs [10]. The third input C represents carry input to the first stage. The proposed full adder sum circuit is designed using PTL technique and Boolean identities. According to Eq. (1), the $A \oplus B$ is designed by multiplexing control input techniques. The output of $A \oplus B$ is given swing restoration in output node. This node is directly connected into C and its compliment for sum circuit. According to pass logic the swing restoration node is connected to another node, the output node became differential node of obtained input of $A \oplus B$. After connecting C and its compliment, the sum output behaving as swing restoration node gives better results of summing input.

The carry circuit design using Eq. (2), the $A \oplus B$ input is directly fed into pass transistor gate input. C is connected as a source input of transistor. The AND logic A and B is derived from pass logic, which is implemented into the circuit. The circuit according to Boolean identities, the V_{IH} and V_{IL} is minimum which is opposing the output. So, the additional circuit is supporting the AND gate and minimizing the voltage noise margin of the transistors. According to this full adder circuit, the design sacrificed extra two transistors but the output swing, noise margin and switching events are minimized. The complete design of proposed full-adder circuit is shown in Fig. 1.

$$SUM = A \oplus B \oplus C \tag{1}$$

$$CARRY = AB + C(A \oplus B) \tag{2}$$

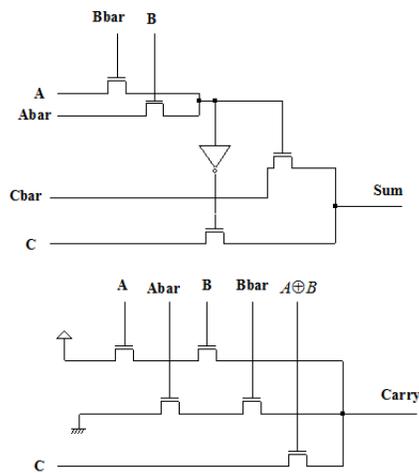


Fig. 1. Proposed Full Adder.

2.2. Bit-parallel iterative CORDIC design

A bit-parallel iterative CORDIC circuit is shown in Fig. 2. The conventional design of CORDIC circuit is occupying more transistor count than PTL design. The pass transistor design could be reduced to two transistors per logic gates. So the pass transistor based bit-parallel iterative CORDIC circuit gives less power and high speed. The hardware structure of CORDIC circuit, each branch consists of an adder/subtractor, shift unit and register for buffering the output [11]. The initial values fed into register by multiplexer, where Most Significant Bit (MSB) of stored

value in z -input, determines the operation mode for adder/subtractor. Signals x and y inputs pass shift units and added/subtracted from not changing signal in the opposite path [4]. The z input arithmetically combines registers values with values taken from Look-Up Table (LUT) whose address changed according to number of iteration. For ' n ' iterations, outputs are mapped back to the registers before initial values fed in again and final sine value can be accessed at output stage. According to selection input, bit words are stored in the register which is transferred into adder/subtractor cell [12]. Depending upon the register output, full adder sum/carry gets activated and gives the results.

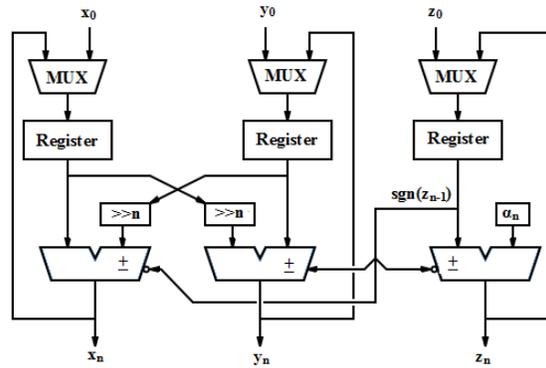


Fig. 2. Bit-Parallel Iterative CORDIC.

3. Results and Discussion

The proposed adder based CORDIC circuit and other adder based CORDIC circuits are simulated by known C_{Load} and constant simulated values. The four adder based CORDIC circuits were designed for feature size CMOS 130 nm technology and corresponding supply voltage 1.2 V. The speed of proposed adder based CORDIC circuit can be determined by maximum delay along the critical path. The worst-case delays were measured for all inputs set to logic low to high (000 – 111). The bit-parallel iterative CORDIC cell gives an output according to LUT constraints. The delay is minimised due to less critical path which is shown in timing diagram in Fig. 3., whereas X_0, Y_0, Z_0 are inputs and X_n, Y_n, Z_n are output signals. The power dissipation of the circuit is minimised due to faster switching events in NMOSFET of the designed cell.

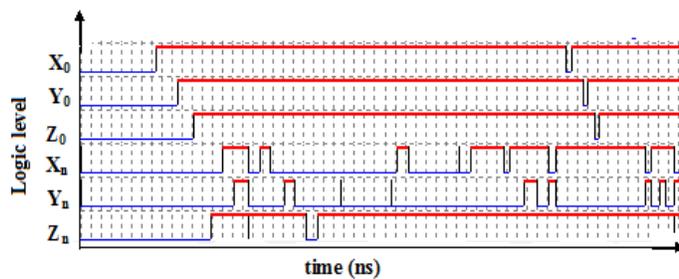


Fig. 3. Timing Diagram of Proposed Adder Based CORDIC Cell.

The layout simulation of proposed adder, MCIT 7T, mixed Shannon and Shannon adder based CORDIC circuit are analysed by using CMOS 130nm and corresponding supply voltage 1.2 V. The power dissipation (P_D), propagation delay (τ), area, number of transistors, EPI, latency and throughput are measured and illustrated in Table 1. From the simulated results, it is clear that the CORDIC circuit designed based on the proposed adder cell gives better performance in terms of power and delay than the other three adder based CORDIC cells. The Energy per instruction (EPI) is product of capacitance toggled while processing the instruction and supply voltage of corresponding feature size [13]. EPI is a measure of amount of energy expanded by a circuit for each instruction that the circuit execute which gives power efficiency of a circuit. It records the average amount of energy expanded per instruction processed by circuit.

The EPI is calculated for four different types adder based CORDIC cells in order of pico-watts/instruction per second (pW/IPS), which is denoted in Table 1. If the latency increases then the circuit's operating speed would decrease [14, 15]. The observation of proposed adder based CORDIC cell obtained lower latency than other adder based CORDIC cell due to cell arrangements and less critical path in entire circuits. So our proposed adder based CORDIC cell also gives better throughput than the other adder based CORDIC cells.

Table 1. Power, Propagation Delay, Area, EPI, Latency and Throughput of the CORDIC Cells.

CORDIC Cell	P_D (μW)	τ (ps)	Area (μm²)	# of Trans	EPI (pW/IPS)	Latency (ns)	Throughput (Gbps)
MCIT 7T	3.3	40	1656	98	60.588	2.54	0.3937
M.Shannon	3.166	58	1890	107	64.566	3.558	0.281
Shannon	1.835	79	2560	119	62.888	3.079	0.3247
Proposed	1.705	35	1900	104	56.159	2.035	0.492

Thermal effects are indeed of importance in Micro-ElectroMechanical Systems (MEMS) [16] and integrated circuits. In the devices, the thermal conductivity of the component often determines and limits the sensitivity of the devices, whereas in integrated circuits, the relevant thermal conductivities determine their power dissipation capability. Temperature dependent thermal conductivities of CMOS layers reported in [17]. Measuring thermal properties of CORDIC cell, such as their thermal conductivity, thermal flux, are an important and challenging task in layout. The feature size geometric would shrink and device densities increased when power became drastically increased in the integrated circuit. The dissipation of heat is important to maintain an optimal operating temperature.

There are three ways to dissipate heat from a device such as radiation, conduction and convection. Thermal resistance is the measure of a substance's ability to dissipate heat or the efficiency of heat transference across the boundary between different media. Table 2 shows the operational conditions of proposed adder based CORDIC cell layout parameter in robotic applications. In the mobile robot a weighting memory for storing a plurality of weighting values that are set for correlatively weighting set operation commands to avoid a local portion optimum condition. When the mobile robot became in the local portion

optimum condition after analysing an operation history, set mobile robot and for output a weighting values corresponding to operation analysis circuit. The adder based CORDIC circuit used for steering angle control is one of the core components of mobile robot circuit [18].

Table 2. Operating Condition of Proposed Adder Based CORDIC Cell Layout Parameters.

Dimensions (μm)	$100 \times 19 \times 2 \times 10^{-9}$
Number of layers	11
Layer thickness	$2 \times 10^{-9} \mu\text{m}$
Power	$1.705 \mu\text{W}$
Maximum T_A	60°C
Maximum T_J	120°C

The temperature analysis of layout has been done by BSIM4 advanced analyzer. To find thermal resistivity and conductivity, the junction temperature is important which finalises the output current in output node at maximum node temperature. According to Raph Remsburg [19], the layout temperature is varying with feature size corresponding 100°C to 120°C . In this analysis, the CORDIC layout has taken maximum junction temperature. The junction temperature calculated for determines the necessity of heat sink which is denoted in Eq. (3)

$$T_J = T_A + P \times \theta_{JA} \quad (3)$$

The ambient temperature is break through point of current flow maximum which depends upon junction capacitance and power dissipation. The measurement and analysis has done using by BSIM4 and Eq. (4) is illustrated.

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad (4)$$

In the other way of ambient thermal resistance also calculated for lower feature size which is indicated in Eq. (5).

$$\theta_{SA} = \frac{T_{JMAX} - T_A}{P} - (\theta_{JC} + \theta_{CS}) \quad (5)$$

From the simulated results, it is clear that the CORDIC circuit designed based on the proposed adder gives better performance in terms of thermal conductivity and thermal flux than the other three adder based CORDIC cells, which is identified in Table 3. As per device analysis, this paper may involve studying of temperature effect, which is finding the value for chip ambient temperature, assembling tolerance temperature and parasitic effect temperature. According to low power dissipation, high speed, high EPI and throughput this paper may be used in all mobile devices, which require minimum power in order to accommodate many advanced features. The transistors that have been used in this CORDIC circuit were connected correctly into the tree taking into serious account the critical path, therefore it gives better performance in terms power dissipation, propagation delay, EPI and throughput.

Table 3. Leakage Current, Temperature Coefficient, Thermal Conductivity and Thermal Flux of the CORDIC Cells.

CORDIC Cell	Leakage Current (mA)	Temperature Coefficient (mV/°C)	Thermal Conductivity (W/m°C) $\times 10^{-8}$	Thermal Flux (W/m ²) $\times 10^{-6}$
MCIT 7T	0.17	4.0	5.5	8.8
M. Shannon	0.019	4.2	5.28	8.45
Shannon	0.018	1.8	3.06	4.9
Proposed	0.011	2.6	2.84	4.54

Figure 4 shows the variation of leakage current with temperature (°C) for CORDIC circuits designed with proposed adder cell and other three adder cells. The temperature analysis was carried out using BSIM4 advanced layout analyzer for various temperatures. The maximum drain current was used to determine the transistor operating points. Electron mobility decreased with increases in temperature, hence the total current of the circuit decreased at high temperature [20]. At all temperatures, the proposed adder based CORDIC cell has lower leakage current. The proposed adder based CORDIC cell can be used in low power applications even when the temperature is increased to 120°C due to consuming low power. Our proposed adder based CORDIC cell provides the least leakage current variation with temperature compared to other adder based CORDIC cells.

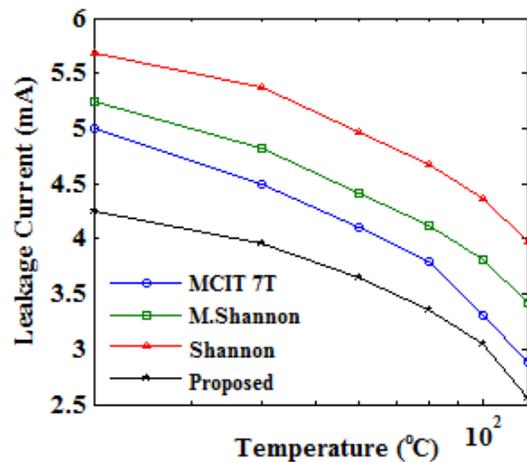


Fig. 4. Temperature versus Leakage Current for Different Adder Based CORDIC Cell.

4. Conclusions

The bit-parallel iterative CORDIC circuit is designed using our proposed adder cell using by PTL technique. The proposed adder based CORDIC circuit is simulated and results are compared with other three adder based CORDIC circuits in terms of power, delay, EPI and throughput. The proposed adder based CORDIC cell gives

improvement in all these parameters. The proposed adder based CORDIC cell consumes low power, gives lower delay and improved speed than other three adder based CORDIC cells. Our proposed adder based CORDIC cell can be used in robotic applications due to its lower delay, low power dissipation, improved speed and high throughput.

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