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A NOVEL DESIGN OF MULTIPLEXER BASED FULL-ADDER CELL FOR POWER AND PROPAGATION DELAY OPTIMIZATIONS

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Abstract

This paper presents a novel high-speed and high-performance multiplexer based full adder cell for low-power applications. The proposed full adder is composed of two separate modules with identical hardware configurations that generate Sum and Carry signals in a parallel manner. The proposed adder circuit has an advantage in terms of short critical path when compared with various existing previous designs. Comprehensive experiments were performed in various situations to evaluate the performance of the proposed design. Simulations were performed by Microwind 2 VLSI CAD tool for LVS and BSIM 4 for parametric analysis of various feature sizes. The simulation results demonstrate clearly the improvement of the proposed design in terms of lower power dissipation, less propagation delay, less occupying area and low power delay product (PDP) compared to other widely used existing full adder circuits.

Keywords: Multiplexer, Full adder, Low-power, Propagation delay, Parametric analysis.

1. Introduction

With the explosive growth in laptops, portable personal communication systems and the evolution of shrinking technology, the research effort in low-power microelectronics has been intensified and low-power Very Large Scale Integration (VLSI) systems have emerged to be high in demand [1]. There are an increasing number of portable applications requiring small-area, low-power and high-speed circuitry in recent trends. Therefore, circuits with low power consumption have become the major identities for design of microprocessors and system-components [2-4]. However, the battery technology does not advance at the same rate as the microelectronics technology, and there is a limited amount of power

Nomenclatures

A_n	Area of the layout (NMOS), m^2
a_i	i^{th} Complement of Boolean variable, 1 or 0
a_i	i^{th} Boolean variable, 1 or 0
C_{DBn}	Depletion drain bulk capacitance per unit area (NFET), F/cm^2
C_{Dn}	Drain node capacitance per unit area (NFET), F/cm^2
C_{FET}	FET capacitance, F
C_{GSn}	Parasitic gate-source capacitance (NFET), F/cm^2
C_{jn}	Junction capacitance per unit area, F/cm^2
C_{jswn}	Junction sidewall capacitance per unit perimeter (NFET), F/cm
C_L	Load capacitance, F
C_{out}	Total output node capacitance, F
C_{ox}	Gate oxide capacitance per unit area, F/cm^2
C_X	Unknown load capacitance per unit area, F/cm^2
f	Frequency, Hz
I_{DDQ}	Average operating drain current, A
L	Drawn channel length, m
P	Total dynamic power dissipation, W
P_n	Perimeter length of the layout (NMOS), m
Q_e	Charge of mobility carriers (NFET), C
R_n	Layout sheet resistance, ohms
t	Time, s
V_{DD}	Biasing voltage, V
V_G	Gate voltage, V
V_{in}	Input voltage, V
V_{max}	Transistor saturation region voltage, V
V_{min}	Transistor active region voltage, V
V_{out}	Output voltage, V
V_{Tn}	Threshold voltage (NFET), V
V_{Tp}	Threshold voltage (PFET), V
W_n	Channel width (NFET), m
Greek Symbols	
τ	Propagation delay, s
τ_n	Propagation delay (NFET), s

available for the mobile systems. The goal of extending the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation, although low power consumption does not necessarily imply low energy. To execute an arithmetic operation, a circuit can consume very low power by clocking at an extremely low frequency but it may take a very long time to complete the operation. Therefore, designers have been facing many constraints in terms of high speed, low power, and small layout area [5].

Addition is one of the fundamental arithmetic operations and is used mostly in many VLSI systems. The main objective of addition is adding two binary numbers; it is the base of many other useful operations such as subtraction, multiplication, division, and ALU circuits [2, 6]. The adder plays an important role in most of these systems, to estimate the critical path, which determines the overall performance of the system, and the full adder is the fundamental element of complex arithmetic circuits. The main aim of today's research is to enhance the

performance of 1-bit full-adder cell. Lowering the supply voltage appears to be the most well-known means of reducing power dissipation [7]. However, scaling supply voltage also increases circuit delay and degrades the drivability of cells designed with certain logic styles. Recently, clustered voltage scaling and dual voltage supply schemes have been proposed to maintain the chip throughput by selectively lowering the supply voltage for non-critical sub-circuits [8].

The proposed adder and other six types of existing adder circuits are mainly designed and simulated by CMOS 90 nm technology for parametric analysis. The proposed adder is compared with the six existing adders in terms of power dissipation, propagation delay, PDP and area. Reducing the supply voltage and increasing the transistor count are the major constraints for the design of the adder cell, which is eliminated in the proposed design. The proposed adder circuit has a very short critical path and reduced transition activity compared to the existing adders [9, 10]. The energy consumption is measured by the product of average power and worst-case delay. The power-delay product (PDP) represents a tradeoff which is optimised between two conflicting criteria of power dissipation and circuit latency. The rest of this paper is organised as follows. Section II explores a review of the full adder design in six existing logic styles. A new multiplexer based adder cell is presented in Section III. In Section IV the new adder cell along with the existing circuits is simulated, and the results of power dissipation, propagation delay, power-delay product, and area efficiency are analysed and compared. Proposed adder cell is compared for capacitance versus power dissipation, supply voltage versus power dissipation, capacitance versus frequency and supply voltage versus frequency in parametric analysis with the existing designs in Section V. Finally, Section VI concludes the paper.

2. Review of Full-Adder Designs

There are standard implementations with various logic styles that have been used in the past to design full-adder cells and they are also used for comparison in this paper. Although they all have similar functions, the way of generating the intermediate nodes, the outputs, the loads on the inputs, and the transistor count varies. Different logic styles tend to favour one performance aspect at the expense of the others [11]. Some of them use one logic style for the whole full adder and others use more than one logic style for their implementation known as hybrid logic design style. A ***Complementary Pass Transistor Logic (CPL) full adder*** [12] gate consists of two NMOS logic networks (one for each signal rail), two small pull-up PMOS transistors for swing restoration, and two output inverters for the complementary output signals. The design depicts a two-input multiplexer which represents the basic and minimal CPL gate structure [12]. The advantages of the CPL style are the small input loads, the efficient XOR and multiplexer gate implementations, the good output driving capability due to the output inverters and the fast differential stage due to the cross-coupled PMOS pull-up transistors. ***Mixed Shannon full adder*** [10] circuit combines the multiplexing control input technique (MCIT) for the sum operation and the Shannon Theorem for the carry operation. In this logic style, the sum and carry circuits were designed based on Eqs. (1) and (2). An input B and its complement were used as the control signals of the sum circuit. The output node of the two-input multiplexer circuit is the differential node. In order to avoid increasing number of transistors due to the

addition of a third input, the following arrangement was made; the X-OR gate output was fed through the NOT gate from the differential node to the C and $\overline{C}$ inputs of the full adder thereby reducing the number of transistors to six in the sum circuit. The C and $\overline{C}$ output node is called the differential node of the circuit. The differential node output is a summing output, as given in Eq. (1).

$$Sum = \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\,\overline{C} + ABC \tag{1}$$

$$Carry = AB + AC + BC \tag{2}$$

$$f(a_0, a_1, a_2, ..., a_i, ..., a_n) = a_i' f(a_o, a_1, a_2, ..., 0, ...a_n) + a_i f(a_0, a_1, a_2, ..., 1, ..., a_n) \tag{3}$$

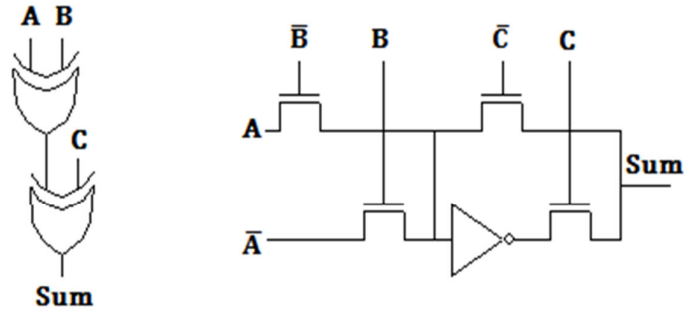
The carry circuit was designed by Shannon complementary pass transistor logic and which used A, B and C inputs. It was designed using the fundamental Shannon equation, given in Eq. (3). The source inputs were connected with logic '1', yielding an always 'on' condition for the transistor. In the carry circuit, all of the pass inputs were connected at V_{DD} line so that the pass gates are always on. The ***Shannon full adder*** [13] sum and carry circuits were designed based on the Shannon theorem. The ***MUX-14T full adder*** [14], an input B and its complement are used as the control signals of the sum circuit. The two-input XOR gate is developed using the multiplexer method. The C and $\overline{C}$ output node is called the differential node of the circuit. The two complementary ($\overline{C}$ and $\overline{B}$ *)* inputs were used in the full adder carry circuit, for balancing of the circuit to avoid the floating wire concept. The ***XOR-10T*** [15] adder circuit CPL technique has logical control of A and $\overline{A}$, B and $\overline{B}$ inputs with adding inverter at the output. Pass variables are directly sent from the inputs to the outputs according to the complementary principle in CPL. ***MCIT-7T*** adder circuit combines the MCIT for the sum operation and the Boolean reduction technique for the carry operation [16]. In the multiplexing method, input B and its complement were used as the control signals of the sum circuit. The output node of the two-input multiplexer circuit is the differential node.

3. Proposed Full Adder

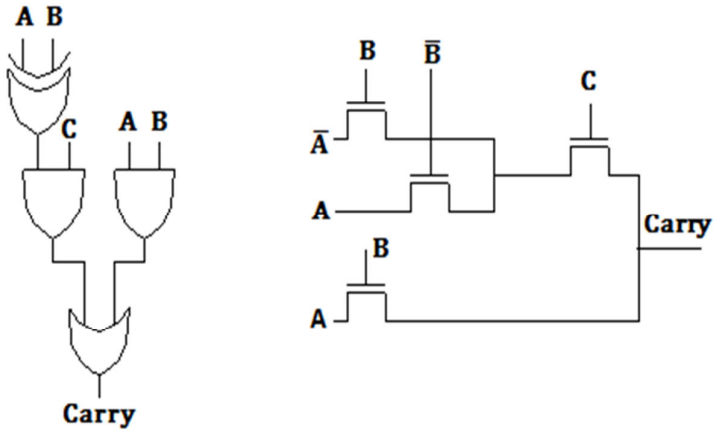
The proposed full adder circuit is designed by multiplexing method and Boolean identities. After the simplification of Boolean identities, the equations of sum and carry are shown in Eqs. (4) and (5). The simplest way of approach to the A⊕B is designed according to the multiplexer method. The exclusive of C and its complement input nodes are directly fed into A⊕B which generates the sum and its schematic form is shown in Fig. 1(a). According to carry Eq. (5), the A⊕B circuit and C input node are combined in the form of logical AND. The exclusive of this output node along with AB circuit generates the carry output according to Eq. (5), and its schematic form is shown in Fig. 1(b). This circuit uses multiplexing method efficiently to reduce the number of nodes to 12. The proposed full adder circuit eliminates the power guard problem due to regular arrangement of the transistor input nodes. Thus, the proposed circuit gives less power dissipation, lower propagation delay, and low PDP when compared to widely use existing full adder circuits.

$$Sum = A \oplus B \oplus C \tag{4}$$

$$Carry = AB + (A \oplus B)C \tag{5}$$



(a) *Sum* Circuit.



(b) *Carry* Circuit.

Fig. 1. Proposed Multiplexer Based Full Adder.

4. Results and Discussion

The seven different adder circuits such as CPL, XOR-10T, Mixed Shannon, Shannon, MUX-14T, MCIT-7T and the proposed adder are designed by pass-transistor logic and also schematised by DSCH2 CAD tool. The proposed full adder and six existing full adder layouts are analysed by 0.35 µm, 0.25 µm, 180 nm, 130 nm, 90 nm, and 65 nm feature sizes at the supply voltages of 3.5 V, 2.5 V, 2 V, 1.2 V, 1 V and 0.7 V respectively. The proposed full adder circuit is balanced for sum and carry due to the proper arrangement of transistors. The proposed full adder is further verified by Boolean identities, and the result timing diagram is shown in Fig. 2. The worst delay for sum and carry are calculated by different combinations of inputs. The worst case delay is measured by varying the

inputs from A=0, B=0, and C=0 to A=1, B=1, and C=1 which results to reduced delay due to less critical path.

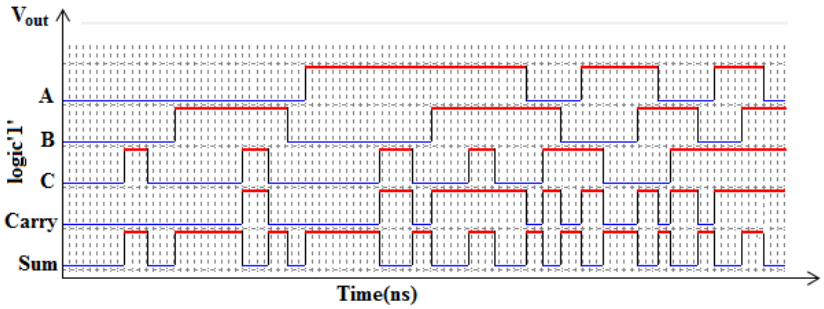


Fig. 2. Proposed Multiplexer Based Adder Timing Diagram.

The full adder circuit performance depends on the transistor count as well as the design concept. The CPL circuit designed by differential node concept used 22 transistors, where the power consumption and propagation delay is increased due to restoration concept. The XOR-10T adder circuit suffers a problem of differential node in sum and carry circuits and the power consumption and propagation delay is high. The mixed Shannon and Shannon circuits were designed by MCIT and the Shannon theorem technique. Due to this hybrid concept, the sum and carry circuits produce NMOSFET drivability problem. The Shannon theorem based adder gives voltage swing restoration. These problems lead to high power consumption and low speed operation in the Shannon and mixed Shannon adder circuits. The MUX-14T adder circuit was designed by multiplexer concept which had a complex node in its design. The drivability of input consumes high power to transmit the voltage level. The MCIT-7T adder circuit was designed by multiplexing control input technique. The transient of input nodes consume more power which leads to high power consumption in the circuit.

The proposed adder circuit gives less power dissipation, propagation delay and less occupying area compared to existing adder circuits as shown in Table 1 due to multiplexing design concept, reducing transistor number and switching transistor event.

Table 2 shows a comparison of 1-bit proposed adder cell, power dissipation, propagation delay, and PDP with the other published authors' results. The proposed adder circuit is compared with Navi et al. [17] for 90 nm feature size. The proposed circuit gives 67.29% reduction in power, 36.56% reduction in propagation delay and 79.25% reduction in PDP. The power dissipation in the proposed circuit is reduced due to the high tasked flow of current and the absence of swing restoration. The majority adder circuit gives 26.06% lower delay than the proposed circuit due to less switching activity in NMOSFET. Navi et al. [17] CPL full adder for 90 nm feature size gives lower propagation delay (-38.18%) compared to proposed design mainly because of the presence of the intermediate node in the output, so the transition is faster than the other adder circuits.

The proposed method gives 10.74% less power dissipation, 27.01% lower delay and 34.88% low PDP when compared with Alioto et al. [18] for 180 nm and 90 nm feature sizes due to lower transistor count. The proposed adder

circuit is compared with Hassoune et al. [19] CPL and ULPFA full adder circuits give better propagation delay than due to high transition activity in NMOSFET than ULPFA adder circuits, but power dissipation (-56.91%) more than the ULPFA adder circuit due to less transistor count. Hassoune et al. [19] CPL circuit has lower delay (-24.52%) than the proposed circuit due to the intermediate node concept.

The proposed circuit gives 89.95%, 82.82% and 98.27% better performance compared to Fartash et al. [20], P-10T, 78.87%, 75.97% and 94.92% better performance than Fartash et al. [20], N-10T, 86.50%, 83.29% and 97.74% better performance than Fartash et al. [20], P11-T, 77.09%, 76.30% and 94.57% better performance than Fartash et al. [20], N-11T circuits for 0.18 µm feature size for power, delay and PDP respectively due to the complex design of the circuits.

The proposed circuit gives 79.37%, 94.91% and 98.95% better performance compared to Kiseon et al. [21] circuit for 0.25 µm feature size for power, delay and PDP respectively due to the presence of repetitive input pattern in adder circuits. The proposed circuit gives 83.63%, 95.5% and 99.26% better performance compared to Gustavo [22] et al. circuit for 0.25 µm feature size for power, delay and PDP respectively due to coupling voltage swing in adder circuits.

The area comparison of the proposed adder circuit with the published authors' adders is shown in Table 3. The proposed adder circuit occupies 4.3% less area when compared with Navi et al. [23], but Navi et al. [23] 10-T and 14-T full adder circuits occupy less area due to the lower number of transistor count.

Table 1. Comparison of 1-bit Proposed, CPL, XOR-10T, MCIT-7T, MUX14-T, Mixed Shannon and Shannon Adder Cell Power Dissipation, Propagation Delay and Area.

Adder type	Supply Voltage	65 nm	90 nm	130 nm	180 nm	0.25 µm	0.35 µm
This work (Proposed adder)	Power µW	0.137	**0.482**	1.172	2.10	19.8	31.8
	Delay (ps)	101.8	**127.3**	106.1	136.2	117.6	260.0
	Area (μm^2)	9x8	**10x9.3**	27x11	56x23	62x35	114x56
CPL	Power µW	2.565	**3.435**	4.675	6.333	27.865	51.908
	Delay (ps)	502.6	**628.7**	1050	1268	1115	1390
	Area (μm^2)	18x12	**24x16**	23x11	48x23	62x35	98x56
XOR-10T	Power µW	1.392	**2.733**	2.96	3.87	21.00	36.98
	Delay (ps)	402.6	**876.0**	562	893	1118	1194
	Area (μm^2)	17x7	**17x10**	21x13	45x19	57x30	90x48
Mixed Shannon	Power µW	1.534	**2.535**	3.817	25.35	49.78	141
	Delay (ps)	200.1	**968**	997	974	982	930
	Area (μm^2)	16x9	**17x7**	19x9	40x19	52x30	82x48
Shannon	Power µW	1.849	**2.309**	2.278	25.09	47.9	175
	Delay (ps)	220	**214**	370	153	970	326
	Area (μm^2)	22x10	**23x8**	27x10	56x21	72x32	114x52
MUX-14T	Power µW	1.564	**4.771**	7.88	6.52	32	78
	Delay (ps)	906	**780**	1400	570	809	998
	Area (μm^2)	25x8	**30x7**	32x8	56x19	72x30	114x48
MCIT-7T	Power µW	0.312	**3.99**	1.471	6.04	7.75	63.87
	Delay (ps)	498	**459**	165	660	260	876
	Area (μm^2)	12x11	**13x7**	15x8	31x18	40x30	64x48

Table 2. Comparison of 1-bit Proposed Adder Cell, Power Dissipation, Propagation Delay, and PDP with the other Published Authors' Results.

Adder type	Feature size	Power µWatt	% reduction	Delay ns	% reduction	PDP fJ	% reduction
This work	0.18 µm	2.10	----	0.136	----	0.285	----
	0.25 µm	19.8	----	0.117	----	2.316	----
	130 nm	1.172	----	0.106	----	0.124	----
	90 nm	0.482	----	0.127	----	0.061	----
Navi et al.[17] proposed	90 nm	1.473	67.29	0.200	36.56	0.295	79.25
Navi et al.[17] majority	90 nm	1.575	69.39	0.093	-26.06	0.147	58.61
Navi et al.[17] hybrid	90 nm	1.579	69.48	0.220	42.35	0.347	82.40
Navi et al.[17] 14T	90 nm	3.332	85.53	0.347	63.47	1.158	94.71
Navi et al.[17] TGA	90 nm	1.779	72.91	0.234	45.91	0.417	85.35
Navi et al. [17] TFA	90 nm	1.745	72.39	0.325	61.01	0.568	89.23
Navi et al.[17] CPL	90 nm	1.768	72.74	0.078	-38.18	0.138	55.90
Navi et al.[17] CMOS	90 nm	1.589	69.67	0.127	0.31	0.202	69.76
Navi et al.[17] proposed	0.18 µm	5.845	64.07	0.191	29.05	1.152	75.21
Navi et al.[17] majority	0.18 µm	6.322	66.78	0.185	26.64	1.172	75.63
Navi et al.[17] hybrid	0.18 µm	6.395	67.16	0.274	50.41	1.172	75.64
Navi et al.[17] 14T	0.18 µm	12.731	83.50	0.382	64.46	4.782	94.02
Navi et al.[17] TGA	0.18 µm	8.476	75.22	0.294	53.88	2.499	88.57
Navi et al. [17] TFA	0.18 µm	8.255	74.56	0.288	52.81	2.379	87.99
Navi et al. [17] CPL	0.18 µm	7.723	72.80	0.184	26.20	1.423	79.93
Navi et al.[17] CMOS	0.18 µm	6.234	66.31	0.292	53.53	1.824	84.34
Alioto et al.[18]	0.18 µm	7.51	72.03	0.309	55.98	2.32	87.68
Alioto et al.[18]	90n m	0.54	10.74	0.174	27.01	0.094	34.88
Hassoune et al. [19] CMOS	130 nm	1.43	18.04	0.124	14.51	0.177	29.81
Hassoune et al. [19] CPL	130 nm	1.72	31.86	0.080	-24.52	0.138	9.97
Hassoune et al. [19] PT	130 nm	1.49	21.34	0.110	3.89	0.164	24.25
Hassoune et al. [19]ULPFA	130 nm	0.505	-56.91	0.595	82.18	0.030	-75.85
Hassoune et al. [19] Hybrid	130 nm	1.57	25.35	0.142	25.35	0.224	44.54
Fartash et al.[20] P-10T	0.18 µm	20.9	89.95	0.792	82.82	16.552	98.27
Fartash et al.[20] N-10T	0.18 µm	9.94	78.87	0.566	75.97	5.626	94.92
Fartash et al.[20] P-11T	0.18 µm	15.56	86.50	0.814	83.29	12.665	97.74
Fartash et al.[20] N-11T	0.18 µm	9.17	77.09	0.574	76.30	5.263	94.57
Kiseon[21]	0.25 µm	96	79.37	2.3	94.91	220.8	98.95
Gustavo[22]	0.25 µm	121	83.63	2.6	95.5	314.6	99.26

Table 3. Area Comparison of the Proposed Full Adder with the Published Full Adders for 90 nm Feature Size.

	CCMOS	CPL	TFA	TGA	14T	10T	Hybrid	Navi	Proposed
Length (µm)	17.45	11.20	9.58	14.07	12.10	11.2	9.85	11.43	10
Width (µm)	7.11	12.20	10.08	9.59	6.11	6.30	10.97	8.51	9.3
Area (μm^2)	124.07	136.36	96.57	134.88	73.93	70.56	108.05	97.26	93

5. Parametric Analysis

The layout parameters are calculated from total transistors of the circuit, wires and input/output pads. Power in modern digital CMOS integrated circuits has traditionally been dominated by dynamic switching power. However, as technology scale leakage currents become increasingly large, measures must be taken into account to minimize total power consumption [24]. Once the magnitude and general shape of the curve has been examined, the measurements can be done using a linear scale for current. The proposed full adder is compared with the other six existing adders in parametric analysis such as capacitance

versus power dissipation, voltage versus power dissipation, capacitance versus frequency and voltage versus frequency by BSIM 4. The circuit layout capacitance versus power dissipation of the adder circuits is shown in Fig. 3. The layout dimensions of full adder circuits and the capacitance C_{Dn} at the output node is as shown in Eq. (6)

$$C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2} C_{ox} L' W_n + C_{jn} A_n + C_{jswn} P_n \tag{6}$$

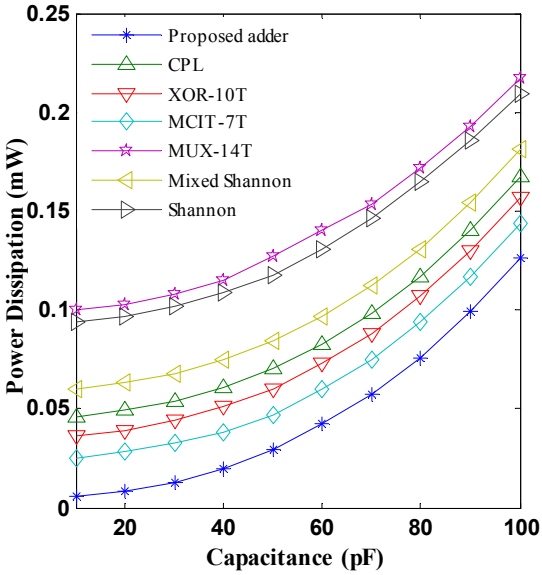


Fig. 3. Capacitance vs. Power Dissipation for the Proposed Adder.

It is significant to remember that increasing the channel width of a FET increases the parasitic capacitance values in the adder circuit. The total output capacitance is calculated using the switching times of the transistor to drive an external load capacitance $C_{L.}$ Thus, the total output capacitance of the full adder circuit is as shown in Eq. (7).

$$C_{out} = C_{FET} + C_L \tag{7}$$

According to parametric analysis, it is evident that the parasitic internal contributions cannot be eliminated. These add to C_L since as all elements are in parallel. The total output capacitance C_{out} is the load that the gate must drive and the numerical value varies with the load. The charging level of the FET is as shown in Eq. (8).

$$Q_e = C_{out} V_{DD} \tag{8}$$

The total output dynamic power dissipation of the adder circuit can be calculated by the sum of average power and short circuit power as shown in Eq. (9) over a single cycle with a period of T

$$P = V_{DD} I_{DDQ} + C_{out} V_{DD}^2 f \tag{9}$$

The dynamic power dissipation in an adder circuit is directly proportional to the signal frequency. The proposed adder gives lower power dissipation than CPL, XOR-10T, Mixed Shannon, Shannon, MUX-14T, and MCIT-7T circuits. The load capacitance (C_L) represents the power dissipated during a switching event. The output node voltage makes a power transition, when load capacitance values are increased irrespective of supply voltage level. Generally, in digital CMOS circuits, dynamic power is dissipated when energy is drawn from the power supply voltage to charge up, which is clearly identified in Fig. 4.

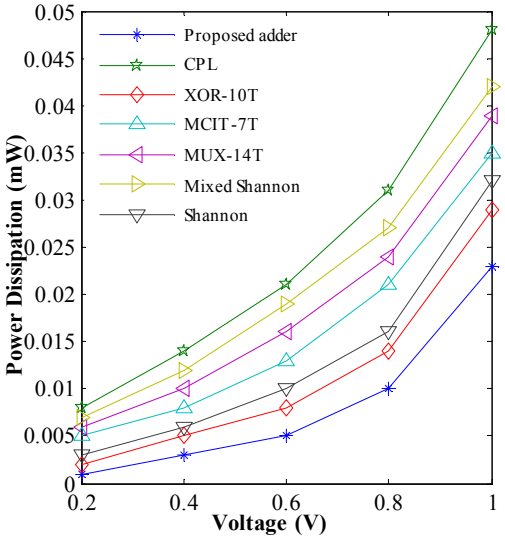


Fig. 4. Voltage vs. Power Dissipation for the Proposed Adder.

The full adder NFET pass circuit is controlled by the gate voltage V_G. By placing a logic '1', the input voltage of $V_G = V_{DD}$ drives the NFET active, and the current can flow through the output transistor load capacitance values. For the case of a logic '1' transfer, the proposed adder circuit uses an input voltage of $V_{in}=V_{DD}$. Assuming an initial condition of $V_{out}=0$, the value can be analysed as shown in Eq. (10).

$$V_{out}(t) = V_{\max}\left(\frac{t/2\tau_n}{1+t/2\tau_n}\right) \tag{10}$$

The maximum voltage transferred through an NFET of the proposed adder circuit can be identified by a limit of feature size voltage as shown in Eq. (11).

$$\lim_{t\to\infty} V_{out}(t) = 0 \tag{11}$$

According to diode equation [25], the power in the circuits increases exponentially after it passes the threshold voltage obeying the Ohm's law. The proposed circuit gives lower power dissipation when compared to other six existing circuits irrespective of the supply voltage.

The proposed adder circuit is simulated at various feature sizes and corresponding supply voltages. This paper analyses 90 nm feature size at 1V. The output analysis of logic '1' transfers the data according to data inputs. The voltage versus frequency response of the proposed adder and the existing six adders is as shown in Fig. 5. The adder input data analysis in clock cycles fall time needed for the output to change from V_{max} to the 10% voltage $0.1V_{max.}$ The output waveforms' charge and discharge levels depend upon the threshold voltage of N and P layouts and is shown in Eq. (12).

$$V_{\min} = |V_{Tp}| = |V_{Tn}| \tag{12}$$

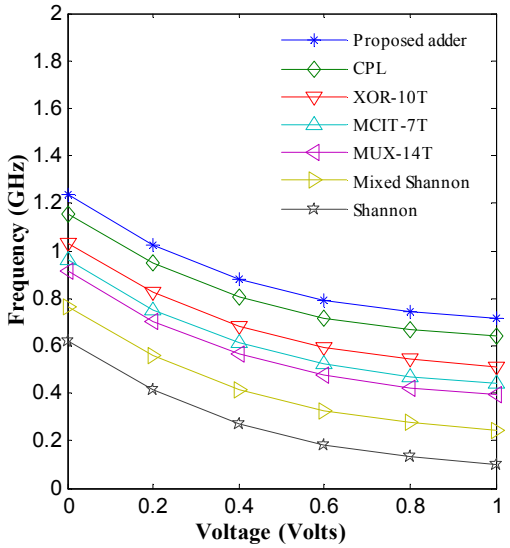


Fig. 5. Voltage vs. Frequency for the Proposed Adder.

The analysis shows that pass transistors cannot be accurately modelled as simple RC circuits, because of the ignorance of the threshold losses and the asymmetrical rise and fall times.

The proposed adder circuit analyses the fall time t_f. The fall time is calculated using $t = RC_{out}$ where C_{out} discharges through the series-connected NFET chain. The proposed adder circuit discharges through C_{out}, and the time cycle is complicated by the presence of the inter-FET capacitance C_L between the two n-channel transistors. In the worst case analysis, C_L charge flows through NFET to ground, since the current through a FET is limited by its aspect ratio (W/L). The discharge rate is limited by the current that can be maintained by the output FET.

The discharge can be described by modelling the output voltage in the exponential form as shown in Eq. (13).

$$V_{out}(t) = V_{DD}e^{-t/\tau_n} \tag{13}$$

According to Elmore formula, the time constant of the proposed adder circuit with inter FET capacitances is shown in Eq. (14).

$$\tau_n = C_{out}(R_n + R_n) + C_L R_n \tag{14}$$

Here the time constant for C_L discharges through the output NFET transistor with a resistance R_n.

The propagation time for Elmore formulation for RC ladder-type networks illustrates that series-connected FETs lead to longer delays in CMOS circuits. The capacitance versus frequency response of the proposed adder and the other six existing adders is shown in Fig. 6. The proposed adder circuit provides the higher frequency compared to others as it is clearly evident in Fig. 6. The total propagation time of the proposed full adder circuit in terms of layout, interconnect and inter FET capacitance is shown in Eq. (15).

$$\tau_n = R_n\left(2C_{out} + C_L\right) \tag{15}$$

This clearly shows the effect of the series-connected FETs in the term R_n and the increase due to the parasitic capacitance C_L.

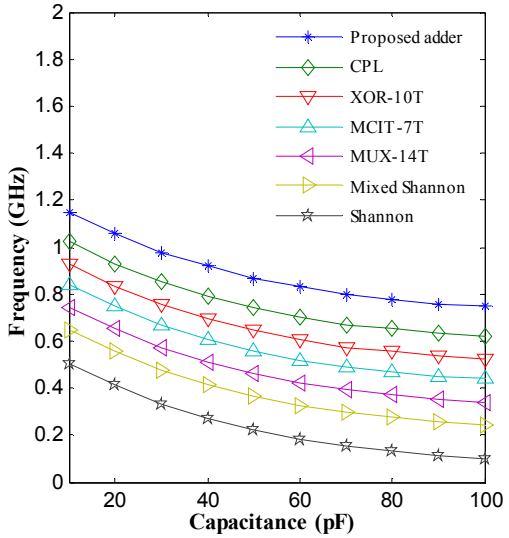


Fig. 6. Capacitance vs. Frequency for the Proposed Adder.

6. Conclusions

In this paper, a novel multiplexer based full adder circuit has been proposed. The proposed circuit along with six other existing circuits are designed by DSCH 2 CAD tool and layouts are generated by Microwind 2 CAD tool. The parametric analysis is done by BSIM 4 analyser. The proposed adder circuit performance is compared with the most promising recently proposed topologies. The comparison for the proposed circuit has been carried out in terms of power consumption, propagation delay, and area and power-delay product for circuit optimisation. The proposed adder circuit is analysed in the parametric analysis, and the results show better performance than the other six existing adder circuits. The proposed adder circuit may be suitable for use as low voltage, and in high speed circuits.

References

1. Rabaey, J.M.; and Pedram, M. (1995). *Low power design methodologies*. Kluwer Academic Publishers, Boston.
2. Alito, M.; and Palumbo, G. (2002). Analysis and comparison of the full adder block. *IEEE Transactions on VLSI*, 10(6), 806-823.
3. Shalem, R.; John, E.; and John, L.K. (1999). A novel low power energy recovery full adder cell. *Proceedings of the Great Lakes Symposium on VLSI*, 380-383.
4. Pedram, M.; and Rabaey, J.M. (2002). P*ower aware design methodologies*. Kluwer Academic Publishers, Boston.
5. Soudris, D.; Piguet, C.; and Goutis, C. (2002). *Designing CMOS circuits for low power European low-power initiative for electronic system design*. Kluwer Academic Publishers, Boston/Dordrecht/London.
6. Song, P.J.; and Micheli, G.D. (1991). Circuit and architecture trade-offs for high speed multiplication. *IEEE Journal of Solid-State Circuits*, 26(9), 1119-1184.
7. Chandrakasan, A.P.; and Brodersen, R.W. (1995). *Low power digital CMOS design*. Kluwer Academic Publishers, Norwell, MA.
8. Kuroda, T.; and Hamada, M. (2000). Low-power CMOS digital design with dual embedded adaptive power supplies. *IEEE Journal of Solid-State Circuits*, 35(4), 652-655.
9. Senthilpari, C.; Ajay, K.S.; and Arokiasamy, A. (2006). Statistical analysis of power delay estimation in adder circuit using non-clocked pass gate families. *IEEE 4th International Conference on Electrical and Computer Engineering*, Dhaka, Bangladesh, 509-513.
10. Senthilpari, C.; Ajay K.S.; and Diwakar, K. (2008). Design of a low power, high performance, 8×8 bit multiplier using a Shannon based adder cell. *Microelectronics Journal*, 39(5), 812-821.
11. Marković, D.; Nikolić, B.; and Oklobdžija, V.G. (2000). A general method in synthesis of pass-transistor circuits. *Microelectronics Journal*, 31(11-12), 991-998.
12. Zimmermann, R.; and Fichtner, W. (1997). Low-power logic styles: CMOS versus pass-transistor logic. *IEEE Journal on Solid-State Circuits*, 32(7), 1079-1090.
13. Senthilpari, C.; Diwakar, K.; and Ajay, K.S. (2009). Low energy, low latency and high speed array divider circuit using a Shannon theorem based adder cell. *Journal of Recent Patents on Nanotechnology*, 3(1), 61-72.
14. Senthilpari, C.; Kavitha, S.; and Joseph, J. (2010). Lower delay and area efficient non-restoring array divider by using Shannon based adder technique. *IEEE International Conference on Semiconductor Electronics*. Melaka, Malaysia, 140-144.
15. Wong, K.T.; Woon, T.S.; Wong, J.H.; Jude, J.; and Senthilpari, C. (2007). Low power, low latency and area efficient array multiplier using complementary pass transistor logics adder cell. *IEEE Proceedings of Regional Symposium on Microelectronics*. Penang, Malaysia, 90-94.

16. Senthilpari, C.; Zuraida, I.M.; and Kavitha, S. (2011). Proposed low power, high speed adder-based 65 nm square root circuit. *Microelectronics Journal*, 42(2), 445-451.
17. Navi, K.; Foroutan, V.; Rahimi Azghadi, M.; Maeen, M.; Ebrahimpour, M.; Kaveh, M.; and Kavehei, O. (2009). A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter. *Microelectronics Journal*, 40(10), 1441-1448.
18. Alioto, M.; Cataldo, G.D.; and Palumbo, G. (2007). Mixed full adder topologies for high-performance low-power arithmetic circuits. *Microelectronics Journal*, 38(1), 130-139.
19. Hassoune, I.; Flandre, D.; O'Connor, I.; and Jean-Didier, L. (2010). ULFA: A new efficient design of a power-aware full adder. *IEEE Transactions on Circuits and Systems-I: Regular Papers*, 57(8), 2066-2074.
20. Vasefi, F.; and Abid, Z. (2005). Low power n-bit adders and multiplier using lowest-number-of-transistor 1-bit adders. *IEEE Canadian Conference on Electrical and Computer Engineering*, Saskatoon, Canada, 1731-1734.
21. Cho, K.; and Song, M. (2002). Design methodology of a 32-bit arithmetic logic unit with an adaptive leaf-cell based layout technique. *Journal of VLSI Design*, 14(3), 249-258.
22. Gustavo, A.R. (1998). Evaluation of three 32-bit CMOS adders in DCVS logic for self-timed circuits. *IEEE Journal of Solid State Circuits*, 33(4), 604-613.
23. Navi, K.; Maeen, M.; Foroutan, V.; Timarchi, S.; and Kavehei, O. (2009). A novel low-power full-adder cell for low voltage. *Integration, the VLSI Journal*, 42(4), 457-467.
24. Behrooz, P. (2000). *Computer arithmetic algorithms and hardware designs*. Oxford University Press, 19: 512583-512585.
25. Donald, A.N. (2007). *Microelectronics: circuit analysis and design*. (3rd Ed.), McGraw-Hill Higher Education, Boston, M.A, ISBN 007-125443-9, 137-139.