

EVALUATION OF VARIOUS UNIPOLAR MULTICARRIER PWM STRATEGIES FOR FIVE LEVEL FLYING CAPACITOR INVERTER

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Abstract

This paper presents the comparison of unipolar multicarrier Pulse Width Modulation (PWM) techniques for the Flying Capacitor Multi Level Inverter (FCMLI). Due to switch combination redundancies, there are certain degrees of freedom to generate the five level AC output voltage. This paper presents the use of Control Freedom Degree (CFD) combination. The effectiveness of the PWM strategies developed using CFD are demonstrated by simulation and experimentation. The results indicate that the multilevel inverter triggered by the developed USHPWM strategy exhibits reduced harmonics. PWM strategies developed are implemented in real time using dSPACE/Real Time Interface (RTI). The simulation and experimental output closely match with each other validating the strategies presented.

Keywords: CFD, dSPACE, FCMLI, PWM, Unipolar PWM, dSPACE.

1. Introduction

Multilevel inverter has drawn tremendous interest in high power applications because it has many advantages: it can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. When the number of output levels increases, harmonics of the output voltage and current as well as EMI decrease. Nabae et al. [1], Lai and Peng [2] and Carrara et al. [3] investigated three PWM methods with different vertical and horizontal combinations leading to the quantification of their output harmonics. Multilevel PWM methods based on control degrees of freedom combination and their theoretical analysis are discussed by Yan Deng et al. [4]. Anshuman Shukla et al. [5] used capacitors called flying capacitors for clamping the voltage across the power semiconductor devices

Nomenclatures

| | |
|-------|-----------------------------|
| A_c | Carrier amplitude, V |
| A_m | Reference amplitude, V |
| f_c | Carrier frequency, Hz |
| f_m | Reference frequency, Hz |
| m | No. of levels at the output |
| m_a | Modulation index |
| m_f | Frequency ratio |

Abbreviations

| | |
|-----------|---|
| CFD | Control Freedom Degree |
| DF | Distortion Factor |
| EMI | Electro Magnetic Interference |
| FCMLI | Flying Capacitor Multi Level Inverter |
| PWM | Pulse Width Modulation |
| RMS | Root Mean Square |
| THD | Total Harmonic Distortion |
| UCOPWM | Unipolar Carrier Overlapping PWM |
| UISCOPWM | Unipolar Inverted Sine Carrier Overlapping PWM |
| UISCPSPWM | Unipolar Inverted Sine Carrier Phase Shift PWM |
| UISCSPWM | Unipolar Inverted Sine Carrier Sub Harmonic PWM |
| UPSPWM | Unipolar Phase Shift PWM |
| USHPWM | Unipolar Sub Harmonic PWM |

in FCMLI. The FCMLI is not as common but it has some distinct advantages over diode-clamped topology including the absence of clamping diodes and the ability to regulate the flying capacitor voltages through redundant state selection even if the number of voltage levels is greater than three. Unlike the output series H-bridge inverter, isolated voltage sources are not required. Yuan et al. [6] discussed the self balancing of the clamping capacitor voltages in the multilevel capacitor-clamping inverter under sub-harmonic PWM. Considering these advantages, Meynard et al. [7] discussed the basic concepts of FCMLI and many practical applications in industry. The FCMLI is increasingly used in many high power applications because it is easier to increase number of levels in this inverter than the diode clamped multilevel inverters. Lee et al. [8] presented the carrier based PWM method for voltage balancing of FCMLI. Kang and Hyun [9] suggested a simple harmonic analysis method for multi carrier PWM techniques using output phase voltage in multilevel inverter. Jeevanandan et al. [10] have reviewed the carrier based PWM methods which offer many more degrees of freedom than traditional two level PWM. This paper discusses a comparative study carried out on unipolar PWM strategies for chosen five level FCMLI both by simulation and real time implementation. Bensraj and Natarajan [11] focuses on Multicarrier Trapezoidal PWM (MCTPWM) techniques with Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and PS of carrier for the chosen CMLI. It is observed that PD method provides output with the lowest distortion. Of the four strategies developed, POD is found to perform relatively better since it provides relatively higher fundamental RMS output voltage and relatively lower stress on the devices for moderate modulation index.

2. Flying Capacitor Multilevel Inverter

Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load. FCMLI is a multiple voltage level inverter topology which uses capacitors (called flying capacitors) for clamping the voltage across the power semiconductor devices. Fig.1 shows structure of a single phase five level FCMLI which requires 8 semiconductor switches, 3 flying capacitors and 2 DC link capacitors. This FCMLI consists of four switching pairs (S1 S1'), (S2 S2'), (S3 S3') and (S4 S4'). If one switch of the pair is switched on, the other complementary switch of same pair must be off. The switches are clamped by DC-link together with flying capacitors. The four switches (S1-S4) must be connected in series between DC input and load and likewise for (S1'-S4'). The three flying capacitors C3, C4 and C5 are charged to different voltage levels. By changing the transistor switching states, the capacitors and the DC source are connected in different ways to produce various load voltages. Typical switch combinations for obtaining different output voltage levels are shown in Table 1 where '+' denotes charging and '-' denotes discharging of capacitors while 'NC' indicates neither charging nor discharging.

The gate signals for the chosen five level FCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter. The simulation and experimental results are compared and evaluated.

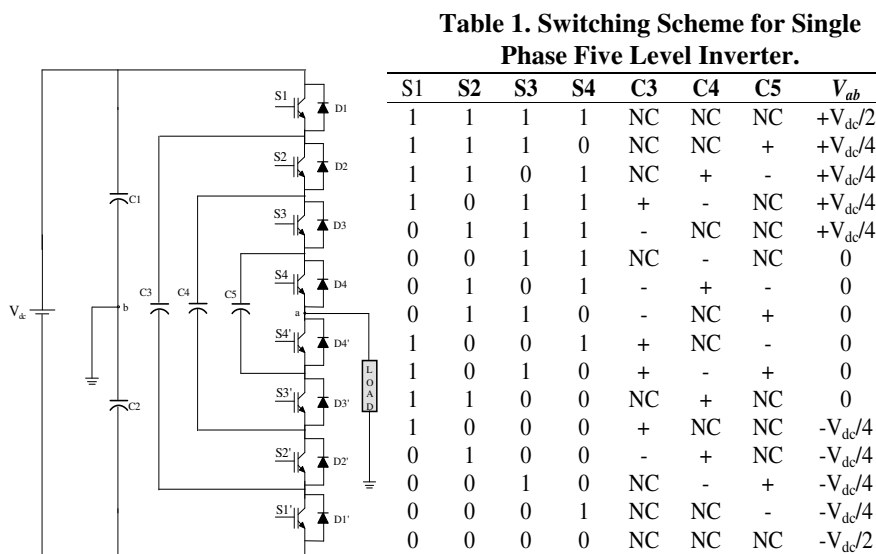


Fig. 1. Five Level Flying Capacitor Inverter.

3. Modulation Strategies Based on CFD

MLIs have several CFDs. Multilevel carrier based PWM methods have more than one carrier option that can be triangular waves, saw tooth wave, a new function etc. As far as the particular carrier signals are concerned, there are multiple CFD including function, frequency, amplitude, phase of each carrier and offset between carriers. The modulation wave of multilevel carrier based PWM method can be a sinusoidal or a trapezoidal wave or a novel function. As far as the particular reference wave is concerned, there are also multiple CFD including function, frequency, amplitude, phase angle of the reference wave. Therefore multilevel carrier based PWM method can have multiple CFD. These CFD combinations added with the basic topologies of MLI will produce many multilevel carrier based PWM strategies. The carrier waves can be either bipolar or unipolar. In this work, the unipolar multicarrier PWM based on CFD is considered. Triangular and inverted sine carriers are used in sub-harmonic, carrier overlapping and phase shift PWM strategies. The modulating/ reference wave of multilevel carrier based PWM strategy is sinusoidal in this work.

4. Unipolar Multicarrier PWM Strategies

For an m -level inverter using unipolar multicarrier technique, $(m-1)/2$ carriers with the same frequency f_c and same peak-to-peak amplitude A_c are used. The reference waveform has amplitude A_m and frequency f_m , and it is placed at the zero reference. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. The frequency ratio m_f is defined in the unipolar PWM strategy as follows: $m_f = f_c/f_m$. In this paper, $m_f = 21$.

4.1. Unipolar sub harmonic PWM (USHPWM) strategy

For a five level inverter, two triangular carriers of the same frequency f_c and the same peak-to-peak amplitude A_c are disposed so that the bands they occupy are contiguous. The carrier set is placed above the zero reference. m_a for USHPWM strategy is $= A_m/(n.A_c)$ where n is the number of carriers. Carrier arrangement for five level USHPWM are shown in Fig. 2 for $m_a=0.8$.

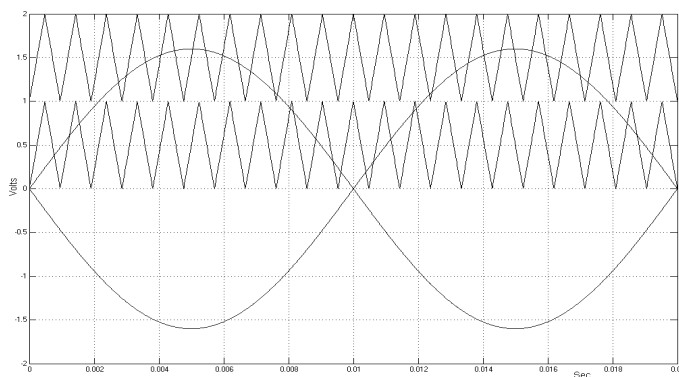


Fig. 2. Carrier Arrangement for USHPWM Strategy.

4.2. Unipolar carrier overlapping PWM (UCOPWM) strategy

The UCOPWM uses two carrier signals of peak-to-peak amplitude A_c and they overlap with each other. The gate signals for the MLI are derived by comparing the two overlapping carriers with two sinusoidal references. The amplitude modulation index is defined for this strategy as follows: $m_a = A_m / ((m/4) A_c)$.

Figure 3 shows the carrier arrangement for the chosen MLI with UCOPWM strategy for $m_a=0.8$.

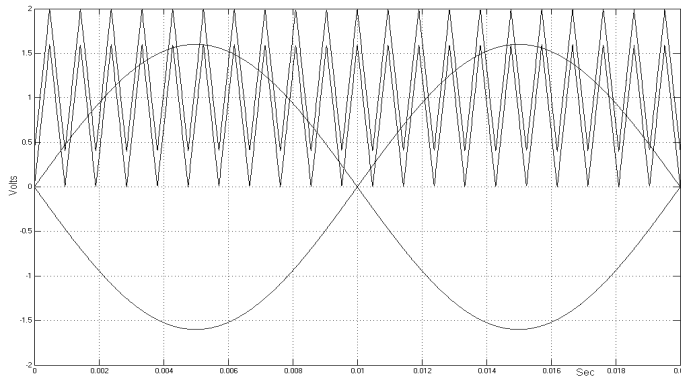


Fig. 3. Carrier Arrangement for UCOPWM Strategy.

4.3. Unipolar phase shift PWM (PSPWM) strategy

The UPSPWM uses $(m-1)/2$ carrier signals of same peak-to-peak amplitude and frequency which are phase shifted by $360 / ((m-1)/2)$ degrees to one another to generate m level output. The gate signals for the chosen MLI are derived by comparison of two carriers with two sinusoidal references of same amplitude and frequency but of opposite phase. Carriers for chosen five level inverter with UPSPWM strategy are illustrated in Fig. 4 for $m_a=0.8$. The amplitude modulation index $m_a = A_m / A_c$.

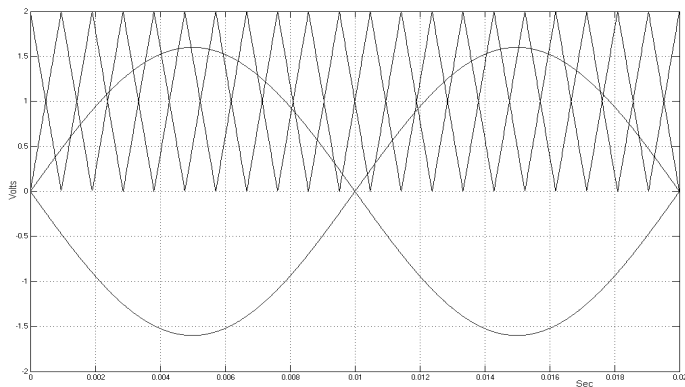


Fig. 4. Carrier Arrangement for UISCSHPWM Strategy.

4.4. Unipolar inverted sine carrier sub harmonic PWM (UISCSHPWM) strategy

This control scheme uses inverted (high frequency) sine carriers which are placed above zero reference. The fundamental frequency sinusoids of 0 and 180° phase are selected as the modulating waves. m_a for this strategy is same as that of USHPWM. Carriers for 5-level inverter with UISCSHPWM strategy are shown in Fig. 5 for $m_a=0.8$.

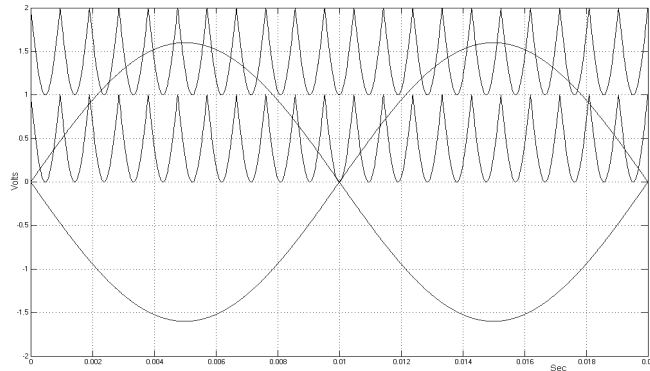


Fig. 5. Carrier Arrangement for UISCSHPWM Strategy.

4.5. Unipolar inverted sine carrier overlapping PWM (UISCOPWM) strategy

In this pattern, the two inverted sine carriers overlap with other. Carriers for five level inverter with UISCOPWM strategy are shown in Fig. 6 for $m_a=0.8$. Inverted sine carriers generated by using (i) sinusoidal voltage source and rectifier blocks in Simpower system module of Simulink or (ii) sine wave generator block and s-function based rectifier block.

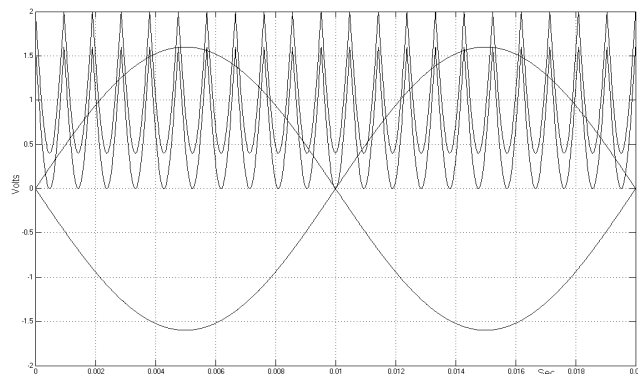


Fig. 6. Carrier Arrangement for UISCOPWM Strategy.

4.6. Unipolar inverted sine carrier phase shift (UISCPSPWM) strategy

The triangular carrier waves of UPSPWM are replaced by inverted sine waves in the UISCPSPWM scheme. m_a for this strategy is same as that of UPSPWM

strategy. The carrier arrangement for chosen five level inverter using UISCSPWM strategy is shown in Fig. 7 for $m_a=0.8$.

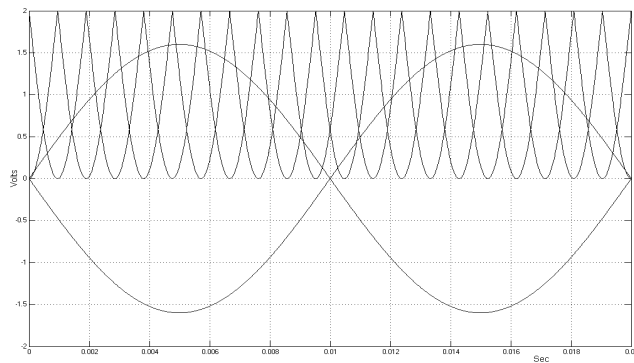


Fig. 7. Carrier Arrangement for UISCSPWM Strategy.

5. Results and Discussion

5.1. Simulation Results

The flying capacitor five level inverter is modeled in SIMULINK using power system block set. Simulations are performed for different values of m_a ranging from 1 to 0.5 and the corresponding % THD are measured using the FFT block and their values are shown in Table 2. Figs. 8-19 show the simulated output voltage of FCMLI and their harmonic spectra with above strategies but for only for one sample value of $m_a = 0.8$.

Figure 8 displays the five level output voltage generated by USHPWM switching strategy and its FFT plot is shown in Fig. 9. Figure 10 shows the five level output voltage generated by UCOPWM switching strategy and its FFT plot is shown in Fig. 11. Figure 12 shows the five level output voltage generated by UPSPWM switching strategy and its FFT plot is shown in Fig. 13. Figure 14 shows the five level output voltage generated by UISCSPWM switching strategy and its FFT plot is shown in Fig. 15. Figure 16 shows the five level output voltage generated by UISCOPWM switching strategy and its FFT plot is shown in Fig. 17. Figure 18 shows the five level output voltage generated by UISCSPWM switching strategy and its FFT plot is shown in Fig. 19. Tables 3 and 4 show the Distortion Factor (DF) and V_{RMS} (fundamental) of the output voltage of chosen MLI. The following parameter values are used for simulation: $V_{DC} = 200$ V, $R(\text{load}) = 100$ ohms, $f_c = 1050$ Hz and $f_m = 50$ Hz.

It is observed from Table 2 that the harmonic content is found to be minimum in USHPWM strategy for chosen modulation indices except $m_a=0.5$. Table 3 shows that the variation in harmonic content of the output voltage after second order attenuation indicated by % DF is relatively less in UPSPWM strategy. From Table 4, it is found that the carrier overlapping strategies provide relatively higher DC bus utilization. It is also observed that the carrier overlapping strategies with inverted sine carriers provide higher DC bus utilisation than with triangular carriers.

It is inferred from FFT plot that (i) 3rd order harmonic is dominant in all the carrier overlapping PWM strategies (ii) Highly dominant lower side band harmonic (20th order) is present in all the PWM strategies (iii) Non-overlapping

PWM strategies with triangular carriers have relatively more number of dominant harmonics of higher order.

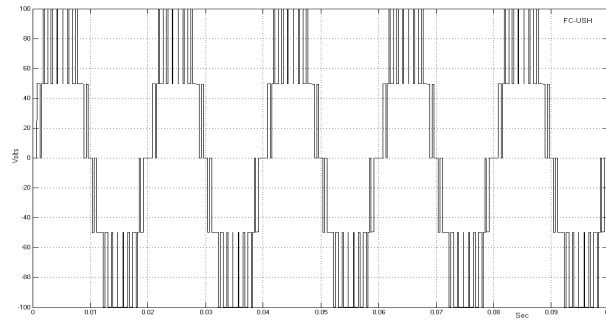


Fig. 8. Output Voltage with USHPWM Strategy.

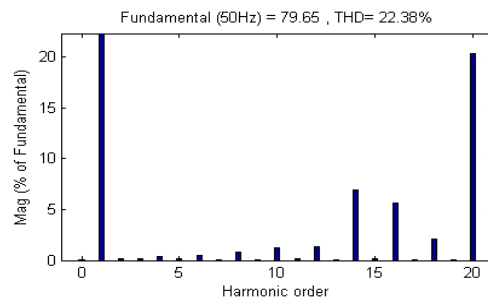


Fig. 9. FFT Plot of USHPWM Strategy.

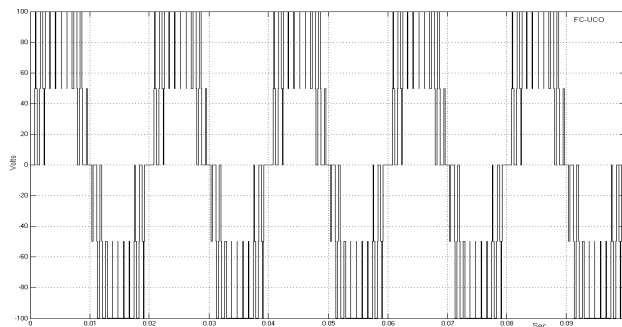


Fig. 10. Output Voltage with UCOPWM Strategy.

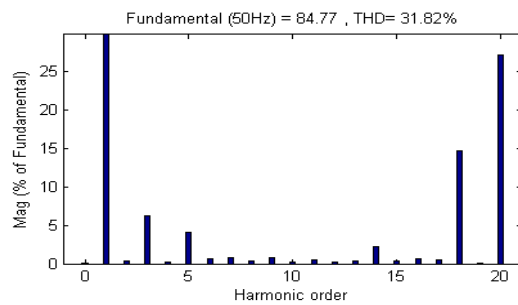


Fig. 11. FFT Plot of UCOPWM Strategy.

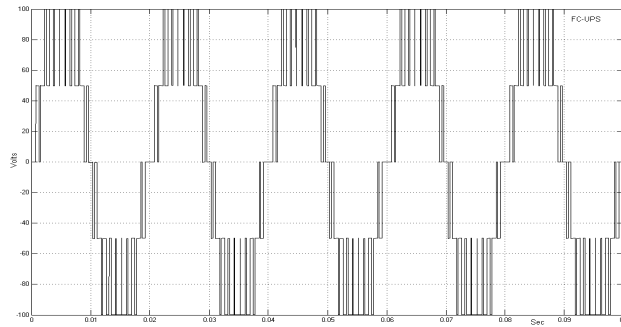


Fig. 12. Output Voltage with UPSPWM Strategy.

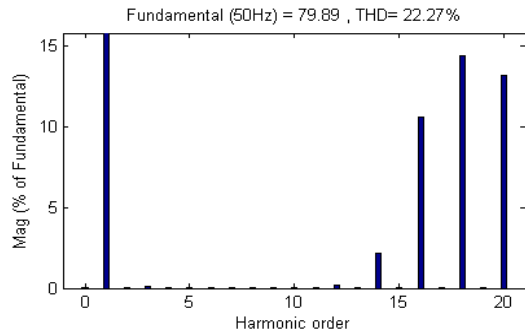


Fig. 13. FFT Plot of UPSPWM Strategy.

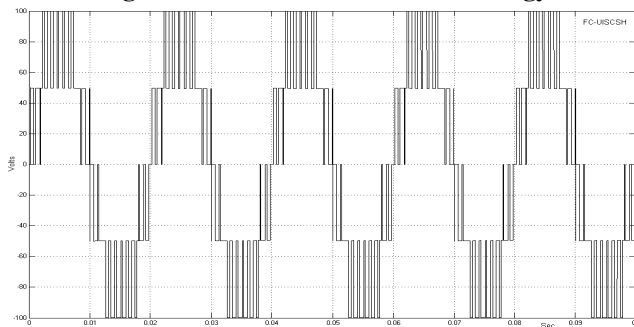


Fig. 14. Output Voltage with UISCSPWM Strategy.

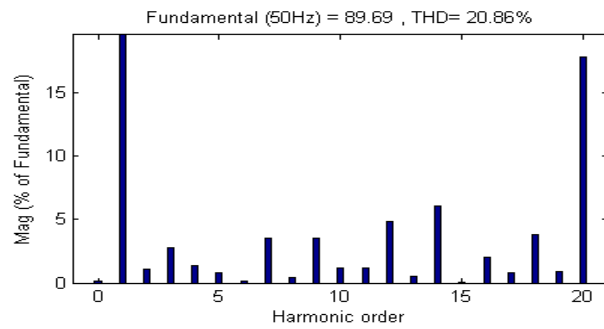


Fig. 15. FFT Plot of UISCSPWM Strategy.

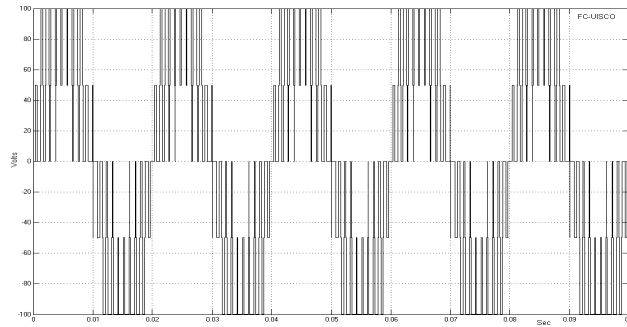


Fig. 16. Output Voltage with UISCOPWM Strategy.

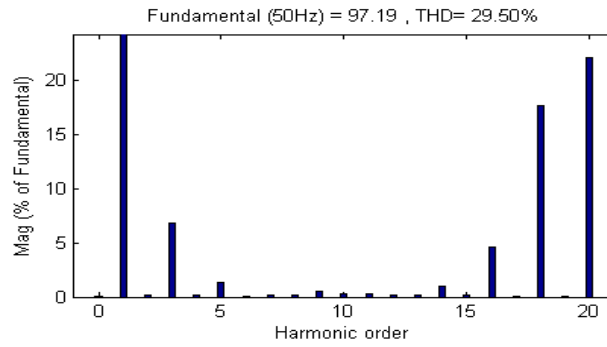


Fig. 17. FFT Plot of UISCOPWM Strategy.

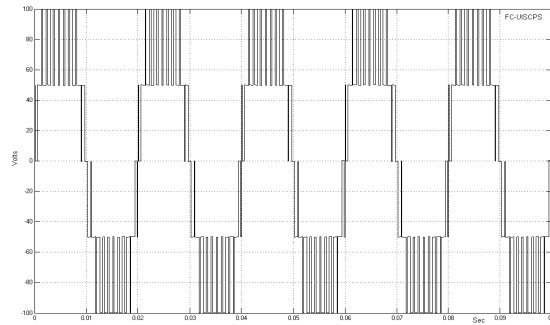


Fig. 18. Output Voltage with UISCPSPWM Strategy.

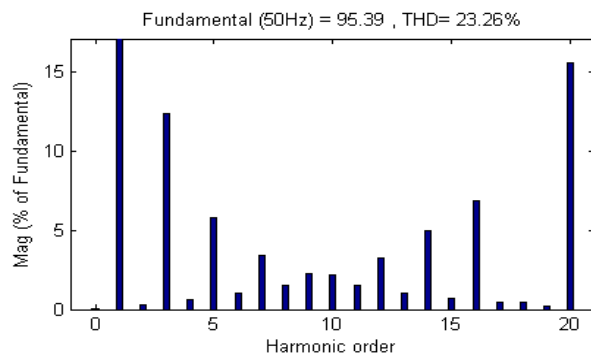


Fig. 19. FFT Plot of UISCPSPWM Strategy.

Table 2 . % THD for Different Modulation Indices.

| m_a | USH | UCO | UPS | UISC SH | UISCO | UISCPS |
|-------|-------|-------|-------|---------|-------|--------|
| 1.0 | 14.62 | 23.26 | 14.65 | 15.05 | 23.48 | 18.79 |
| 0.9 | 18.70 | 27.76 | 18.65 | 17.35 | 25.62 | 20.84 |
| 0.8 | 22.38 | 31.82 | 22.27 | 20.86 | 29.50 | 23.26 |
| 0.7 | 23.16 | 44.87 | 23.22 | 23.98 | 35.60 | 25.33 |
| 0.6 | 22.85 | 55.36 | 22.89 | 25.78 | 42.79 | 26.17 |
| 0.5 | - | 68.34 | - | - | 51.5 | - |

Table 3. % DF for Different Modulation Indices.

| m_a | USH | UCO | UPS | UISC SH | UISCO | UISCPS |
|-------|-------|------|-------|---------|-------|--------|
| 1.0 | 0.076 | 0.22 | 0.079 | 0.62 | 1.11 | 1.33 |
| 0.9 | 0.31 | 0.39 | 0.065 | 0.54 | 0.93 | 1.4 |
| 0.8 | 0.082 | 0.65 | 0.074 | 0.43 | 0.77 | 1.42 |
| 0.7 | 0.13 | 0.76 | 0.081 | 0.36 | 0.68 | 1.46 |
| 0.6 | 0.14 | 0.88 | 0.11 | 0.4 | 0.58 | 1.47 |
| 0.5 | - | 1 | - | - | 0.42 | - |

Table 4. V_{RMS} for Different Modulation Indices.

| m_a | USH | UCO | UPS | UISC SH | UISCO | UISCPS |
|-------|-------|-------|-------|---------|-------|--------|
| 1.0 | 70.61 | 72.63 | 70.68 | 74.66 | 77.67 | 76.95 |
| 0.9 | 63.5 | 66.49 | 63.65 | 69.28 | 73.67 | 72.28 |
| 0.8 | 56.36 | 59.48 | 56.49 | 63.42 | 68.73 | 67.45 |
| 0.7 | 49.25 | 50.68 | 49.37 | 56.79 | 62.4 | 62.5 |
| 0.6 | 42.14 | 41.96 | 42.33 | 48.87 | 55.7 | 57.28 |
| 0.5 | - | 33.24 | - | - | 48.61 | - |

5.2. Experimental Results

This section presents the results of experimental work carried out on chosen FCMLI using dSPACE DS1104 controller board which is based on the Texas Instruments TMS320F240 floating-point DSP. Real time implementation of these strategies using MATLAB – dSPACE/RTI requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/SIMULINK. The dSPACE system is an embedded or self contained system. The dSPACE system combines a data acquisition system with an independent processing system to implement digital control. It is specifically designed for the development of high-speed multivariable digital controllers. The dSPACE system can be plugged into a PCI slot of a PC. The gate signal generation block using different PWM strategies listed above is designed and developed using SIMULINK and downloaded to dSPACE / RTI. The results of the experimental study are shown in the form of the PWM outputs of chosen FCMLI. The PWM signals from the dSPACE are not capable of driving the MOSFETs. In order to strengthen the pulses a driver circuit is provided.

The results of the experimental study are shown in the form of the oscillograms of PWM outputs and harmonic spectrum of chosen MLI. Figures 20-25 show the experimental output voltage and corresponding harmonic spectra of

chosen FCMLI obtained using dSPACE/RTI with USHPWM, UCOPWM, UPSPWM, UISCSPWM, UISCOPWM and UISCPSPWM strategies respectively. PWM outputs shown for only one sample value of $m_a=0.8$. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 20 V. Figure 26 shows the entire hardware setup. The following parameter values are used for experimentation: $V_{dc}=20$ V, $R(\text{load})=100$ Ω , $f_c=1050$ Hz, $f_m=50$ Hz, $m_f=21$, $C1'=C2'=4700$ μF and $C3'=1000$ μF , $C4'=1500$ μF and $C5'=3000$ μF .

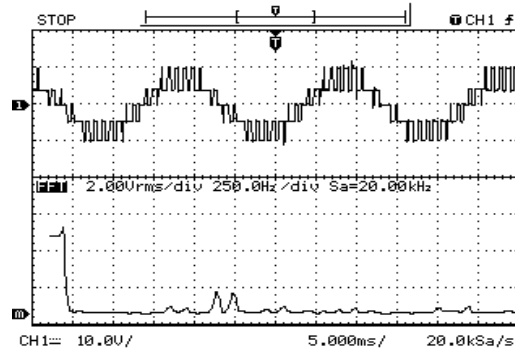


Fig. 20. Experimental Output Voltage with USHPWM Strategy.

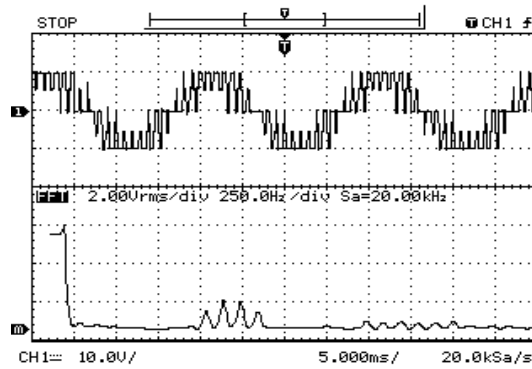


Fig. 21. Experimental Output Voltage with UCOWM Strategy.

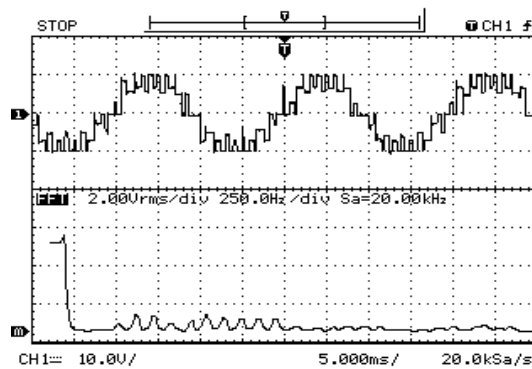


Fig. 22. Experimental Output Voltage with UPSPWM Strategy.

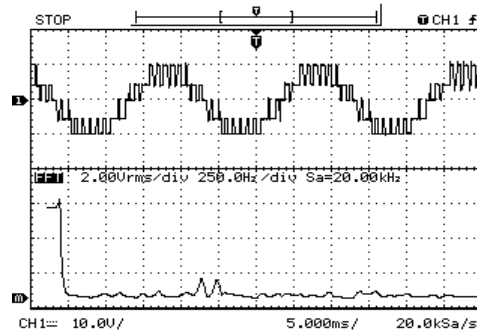


Fig. 23. Experimental Output Voltage with UISCSPWM Strategy.

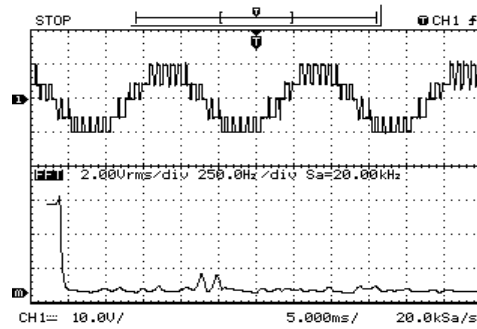


Fig. 24. Experimental Output Voltage with UISCOPWM Strategy.

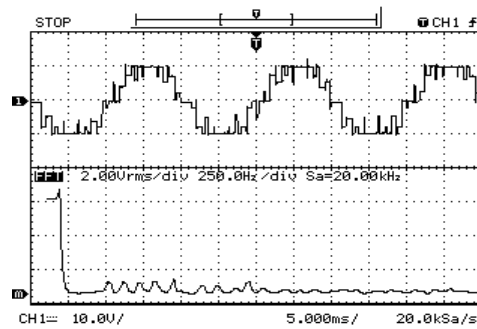


Fig. 25. Experimental Output Voltage with UISCPSPWM Strategy.

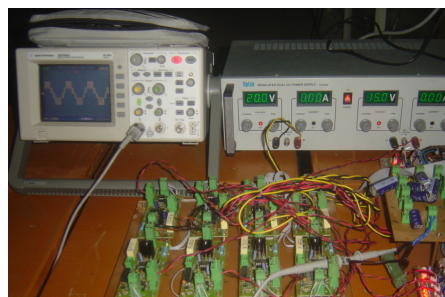


Fig. 26. Hardware Setup.

6. Conclusions

Various unipolar PWM strategies have been developed for different modulation indices ranging from 0.5-1 for the chosen single phase FCMLI. Various performance factors like (i) THD, DF, and harmonic spectra indicating purity of the output voltage (ii) V_{RMS} indicating the amount of DC bus utilization have been evaluated, presented and analysed. The USHPWM method provides lower THD than the other methods (Table 2). The PWM outputs of simulation and experimental results are closely matched with each other validating the strategies presented.

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