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SIMULATION AND DESIGNING OF THREE-STACK GaN HEMT POWER AMPLIFIER for 2-6 GHz BANDWIDTH

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Abstract

This paper illustrates a high power amplifier using GaN HEMT technology, desirable for broadband applications like Satellite, Radar, and Mobile Communications. A multi-drive technique employing three-stack GaN HEMT topology is used for the first time to design a broadband power amplifier having a bandwidth of 2-6 GHz. This technique enables us to get a higher supply voltage at the drain of the topmost HEMT, which allows the higher output power to be obtained. The simulation is done using AWR software for the UMS process of GH25_NHF_10. A complex inter-stage matching topology is used between the drain and the source of two consecutive stacked GaN HEMTs. Because of high output power, high power-added efficiency (PAE) as much as 35% could be achieved. The area occupied by the power amplifier is 5432.646×3784.753 micron. The saturated output power is achieved around 51 dBm along with a power gain of 14 dB.

Keywords: Broadband applications, GaN HEMT, Solid-state power amplifier (SSPA), Stacked HEMT, UMS process

1. Introduction

A microwave power amplifier is an electronic component, which is used at the transmitter end of the communication system, to convert DC power from the input to RF power at the load. The evolution of microwave power amplifiers is becoming more and more demanding in microwave applications, such as satellite payloads, keyless vehicle locks, electronic warfare, medical machines, microwave oven, Wi-Fi, RADARS, Garbage door openers, etc.

In the present time as the technology is growing fast in terms of high output power, small size, low cost, high efficiency, high linearity, large gain, etc., there is a need for this crucial module. The task for Power Amplifier designers of the next decade is to maintain high efficiency, high power, and good linearity across several frequency bands, modulation levels, and bandwidths [1-5].

There are different categories of amplification such as class A, B, C, D, E, F, S, and J, but each differs in terms of operation, efficiency, linearity, and output power capability. Normally, the output power from a single-stage power amplifier decreases as the operating frequency rises, resulting in a greater amount of power amplifiers needed for given output power. Scaling up the power distribution networks with a significant number of power amplifiers results in lower returns and produces a change in incremental output power performance.

Since we are designing the amplifier mainly in the frequency domain, the harmonic balance is the most appropriate one, in comparison to the time-domain method. This high-power amplifier design will also reduce size and weight, conserve electrical power and maintain a long service life without any loss [6, 7].

A Ku-Band microwave power amplifier using GaN HEMT technology has been demonstrated on SiC substrate. Because of the amplifier's potential for instability, an on-chip parallel RC network is employed at the transistor's gate, which has a minor impact on the transistor's output power. Furthermore, this network can be utilized to generate a frequency-dependent loss [8].

The high-power packaged amplifier has shown temperature dependency of gain and output power under continuous-wave operating conditions. It has used AlGaN/GaN HEMT technology having a full gate width of 11.52 mm. The manufactured device produced over 80W of output power at 9.5 GHz frequency and the channel temperature was reported to be 221℃ when the flange temperature was 36 ºC [9].

Virdee et al. [10] presented a harmonic processing technique to improve the efficiency of the power amplifier. At 2.35 to 2.55 GHz, the manufactured GaN HEMT power amplifier generated a nominal gain of 18 dB with an output power of 130W, a PAE of 64%, and a drain efficiency of 73% in continuous wave mode. To attain greater performance of high output power and high efficiency at 1.5 GHz, a new technique is reported to design a high-efficiency power amplifier using RF3931 GaN HEMT as an active device. This technique is governed by suppressing harmonic powers, the input and output matching circuit with transmission lines to increase the output power and efficiency [11].

GaN is a vigorous technology with remarkable reliability. It has made significant progress in the microwave electronics field over the past few years. When it is compared with GaAs and Si, GaN is found to have higher breakdown voltage, higher

electron mobility, higher power density, which can access better applications [8, 9]. Here, GaN on SiC is being used widely in comparison to other substrates like Si, Diamond, Sapphire, and GaAs, etc., because of their excellent thermal conductivity. Increasing power density in GaN technology makes power levels close to those of vacuum tube electron devices.

Recently reported statistics to display the success of GaN power amplifier with high power output density from S-band up to X-band. The main advantages of using this device for high power amplifiers are having low parasitic effects, withstanding high temperature, and high voltage [12]. Therefore, the value of these devices for power amplifier technologies is increasingly growing and hence the need for better design guidelines. Thus, a solid-state power amplifier using GaN is fast-growing technology with remarkably high reliability. Here a GaN HEMT stacked Power Amplifier study is presented with a special emphasis on their existing topologies.

Pornpromlikit et al. [13-16] reported a single-stage 3-stack FET power amplifier using the CMOS process. The circuit consists of a common source transistor and three stacked transistors, which are in series to add their output voltage swings in phase. They have used a resistive voltage divider circuit to separate the gate biasing of the bottom and stacking transistors to improve flat gain, avoid causing an early breakdown of top device, and compression of bottom one. This topology is also beneficial to implement on-chip input-output matching circuits to minimize body effect and parasitic capacitance effect, which arises due to the conventional approach. Load Pull simulation is used to find the values of inductors and capacitors for the input/output matching [17, 18].

The best possible inter-stage matching will solve the problem of phase differences by inserting inductors hence the performance of the power amplifier improves at high frequency [19]. By determining the optimal input matching network, tuning of stack transistors are possible which is used to achieve equal amplitude and phase in collector-emitter voltages. Efficiency can be increased by choosing this topology of stacked transistors on top of cascade transistors [20].

McRory et a. [21] and Wu et al. [22] used the transformers as input matching networks where the losses affect the power amplifier’s overall power gain and PAE but their impact on output saturated power and bandwidth is limited. One possible alternative for improving the output power and efficiency of wideband amplifiers is given by non-uniform distributed power amplifiers [23]. Impedance can be optimized at top of the stack by phase alignment to the artificial drain and gate T-lines. The architecture of the power amplifier is realized using dynamically biased stacked transistor cells, removing the need for an output-matching network. This topology is designed using two common source cells and two cascade cells to achieve high gain without stability and bandwidth concerns [24].

Agah et al. [25] proposed the concept of a stack FET power amplifier to combine the power without using passive power combining techniques. At millimetre-wave frequencies, it is difficult to achieve high efficiency and power. There is a requirement of adding extra tuning elements to obtain complex impedance for maximum performance. Three different approaches are presented for optimal intermediate node impedance that are shunt inductive tuning, shunt feedback tuning, and series inductive tuning [26-30].

This review is structured as follows. in Section 2, the stacking principle has been discussed and design trade-offs examined, with a demonstration of the three-stack power amplifier. The strategy of variations in stacking technique used by other scientists over the last two decades, for designing CMOS FET, GaAs mHEMT, and MESFET power amplifier at different frequencies, has been adopted here [31, 32].

To the best of our knowledge in GaN HEMT amplifier, this is the first stack-based design for high power broadband applications, which gives more than 14W output power. With a given power input, stacking several transistors help in reducing voltage swing on individual devices for better reliability and aging. Here a theoretical approach has been applied in the analysis of phase detuning at the intermediate nodes and its influence on efficiency and output power.

In Section 3, the design of three stack GaN HEMT power amplifiers have been discussed, with the help of a schematic diagram in AWR software. The input and output matching circuit has been used for maximizing the output power strength and performance by eliminating harmonic powers. Section 4 reveals the comparative study of the various references, with the present work, along with the results and discussion. Lastly, Section 5 presents the conclusion of the paper.

2. General Concept of FETs Stacking

The FET stacking circuit consists of a single cascode-like amplifier having a common-source input device along with additional common gate transistors (Fig. 1) connected in series with it. Ideally, the voltages at the output, i.e., at the drain electrodes of the FET devices get added at the drain (output) in phase as one goes up the stack so that maximum drain voltage will appear at the topmost FET device. For this operation to take place, a specified value of voltage swing should appear at the gates of the common-gate-FET devices in the stack, unlike a conventional cascade, which is with RF grounded gate.

As shown in Fig. 1, the external capacitances (C1, C2, C3, and C4) put in shunt with the gates of common gate FET devices of the cascode structure are forming voltage dividers with respect to gate-source capacitances of the respective FET devices. These voltage dividers circuits determine and control the voltage swing at the gates of common gate FETs. This leads to obtaining reduced drain-gate and drain-source swings, which is in contrast with traditional cascode structures and hence less stringent requirement of large signal for each common gate FET device.

Due to the presence of drain to source capacitance, there is a need for compensation, which is facilitated by series-shunt matching done between the drain of common source transistor and source of common gate transistor. The gate capacitances are also employed to protect the device from prematurely aging due to high DC supply voltage, which led to hot carrier injection.

This technique of FET stacking is an alternative to the passive power combining technique and contributes in major two ways (1) FET can be stacked to support high supply voltages. A high RF voltage swing can be obtained at the output, which increases output power and efficiency. (2) Load line impedance in this stacked FET approach, also increases for each additional FET, this allows better impedance matching at the output incurring low mismatch loss.

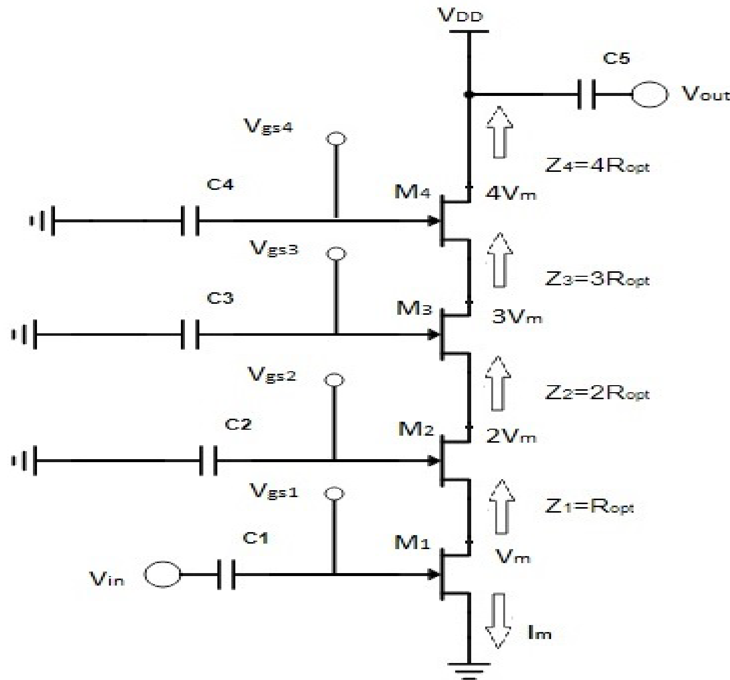

Fig. 1. Four stack FET Power amplifier schematic.

In designing of low-frequency circuit, where the operating frequency is very less in comparison to the transition frequency of the FET device. The output impedance of drain of transistors M_1, M_2, M_3, and M_4 are all approximately real and the FETs will share the same RF current I_m that will be generated in transistor 1. The capacitors values (C_1, C_2, C_3, and C_4) at the gate must be adjusted in such a way so that the drain impedances Z_1, Z_2, Z_3, and Z_4 are equal to the impedances R_{opt}, $2R_{opt}$, $3R_{opt}$, and $4R_{opt}$ as shown in Fig. 1.

The stacked FET device has been constrained to take up the linear operation and its output resistance and impedance due to gate to drain capacitance being large have been neglected. The impedance at the output of each FET device is given by Eqs. 1(a) and 1(b), and small-signal gain of these devices is also given by Eqs. 2(a) and 2(b), (3), (4) [28] from Fig. 2.

$$Z_{M-1} = \frac{(C_{gsM} + C_M + C_{gdM})(1 + g_{mM} Z_M + sC_{gsM} Z_M + sC_M Z_M)}{(g_{mM} + sC_{gsM})(C_{gsM} + C_M + sC_{gdM} C_M Z_M)} \qquad (1(a))$$

$$\approx \frac{1}{g_{mM}}\left(1 + \frac{C_{gsM}}{C_M}\right) \qquad f_o \ll f_T \qquad (1(b))$$

$$A_v = \frac{g_{m1} R_L}{\left(1 + \frac{sC_{gs2}}{g_{m2}}\right)\left(1 + \frac{sC_{gs3}}{g_{m3}}\right)} \qquad (2(a))$$

$$\approx g_{m1} R_L \qquad f_o \ll f_T \tag{2(b)}$$

$$C_M = \frac{C_{gs,M} + C_{gd,M}(1 + g_{m,M} R_{opt})}{(M-1) g_{m,M} R_{opt} - 1}, \; M = 2, 3, 4, \ldots, m \tag{3}$$

$$R_{opt} = \frac{V_1}{I_1} = \frac{2(V_{dd} - V_k)}{I_{\max}} = \left[\frac{1}{8} \frac{(2V_{dd} - V_k)^2}{P_{out}} \right] \tag{4}$$

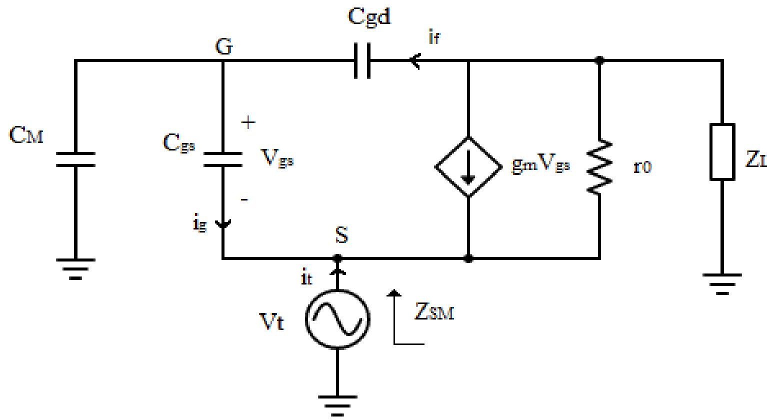

Fig. 2. Small signal equivalent circuit of FET.

The gates of all the FETs stacked devices are biased so that the DC and RF (V_{gs}, V_{gd}, and V_{ds}) voltages should bring down to their respective breakdown voltages. This should be despite supply voltage greater than the breakdown level of the FETs. For this purpose, the DC gate voltage (Eq. (5)) [29] of the stacked FET amplifier having M FETs is set to:

$$V_{G,M} = \left(\frac{M-1}{m}\right) V_{DD} + V_{GS,M-sat} \qquad M = 2, 3, 4, \ldots, \mathrm{m} \tag{5}$$

where, $V_{GS,\,M\text{-}sat}$ is the DC value of the M_{th} FET at the saturation power level.

Therefore, appropriate values of C_M, $V_{G,\,M}$, and R_{opt} will ensure the drain-source voltage to be less than the drain-source breakdown voltage. An additional restriction is required on the size of FETs, which ensures that the gate-drain voltage swing is less than the gate-drain breakdown voltage. The optimal value of gate-drain voltage (Eq. (6)) [29] is given below:

$$V_{gd,M} = -\frac{1 + g_{m,M} R_{opt}}{g_{m,M} R_{opt}} V_{opt} \qquad M = 1, 2, 3, 4, \ldots, m \tag{6}$$

Gate-drain voltage resulting from the smaller size of the transistor may be more than the gate-drain breakdown voltage of the transistor. The reduced gain is an acceptable trade-off viz. a viz. higher saturated output power and higher drain efficiency, in our stacked FET power amplifiers, especially when many transistors are connected in series. The appropriate adjustment of the DC gate voltages is a vital design factor for efficiency and reliable function. Additionally, for obtaining the

correct complex impedance between the transistor's elements, tuning is needed for maximizing performance. For this, three separate tuning circuits such as shunt L, shunt-series feedback, drain-source capacitor, and series inductance between two transistors, have been presented here, for getting appropriate complex node impedances [28]. Further, the above tuning methods have been used also to counteract the phase detuning of the device triggered by parasitic components.

3. Designing of Stacked GaN HEMT Power Amplifier

The design of microwave power amplifier has been implemented on the thick substrate of a thickness (H) = 100µm, having dielectric constant ($\in_r$) = 10.2, Tanδ = 0.0001, with conductor thickness (T) = 2µm. This substrate is having low channel resistance and low dissipation factor, which extends its usefulness to the Ku band and above.

An accurate nonlinear model of UMS foundry (UMS_GH25NHF_10) has been used having a gate length of 0.25 µm, f_t = 52 GHz (Fig. 3) which exhibits good performance. Application-specific design specifications are given in Table 1, which had led to the choice of this GaN HEMT transistor.

The class-A mode has been chosen in which input is a common source HEMT with three additionally attached stacked HEMT. The conjugate matching has been done at the input side to match with 50-ohm impedance along with the stability circuit as shown in Figs. 4 and 5. The input matching circuit is implemented with a pi network in terms of inductance, capacitance, transmission line, and resistance.

The stacked power amplifier is found to be better in terms of matching at the load side. This is due to the fact that when observed in a common source distributed amplifier the optimum load impedance is found to be less $Z_{L,tot}$ = $Z_{L,CS}$/T, as compared to a single common source transistor whereas in stacked FET the optimum load impedance for N transistors are N times the single common source transistor.

Similarly, the input impedance of the N stage common source distributed amplifier is $Z_{in,CS}$/N whereas, in three stacked HEMT, the input impedance is $Z_{in,CS}$/3 only. The circuit consists of a cascade-like transistor topology. The input is applied to a common source transistor stacked to three cascaded common gate transistors.

This configuration helps to increase the voltage handling of a power amplifier. The input impedance of common gate M_1 is determined. The capacitances of the gates are used to allow RF swings at the stacked transistors' gates. These capacitance values have been obtained from the optimum load impedance of the previous transistor to get maximum voltage swing and output power against each transistor. The voltage divider circuit, which is formed by the gate capacitors and gate-source capacitance C_{gs} has produced the in-phase voltage swings at both gate and drain.

Table 1. Design specifications.

Parameters	Specifications
Power Gain	14 dB
Bandwidth	2-6 GHz
Output Power	43 dBm
Small signal Gain dB[S21]	13.14 ± 0.5 dB
Return Loss	< -13 dB

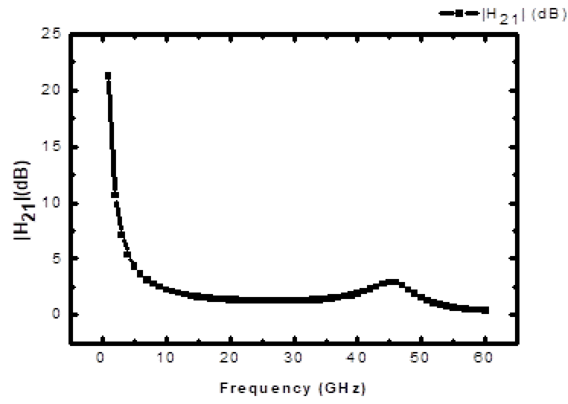

Fig. 3. Graph of f_T ($|H_{21}|$) of GaN HEMT (UMS) for frequency range of 1 to 60 GHz.

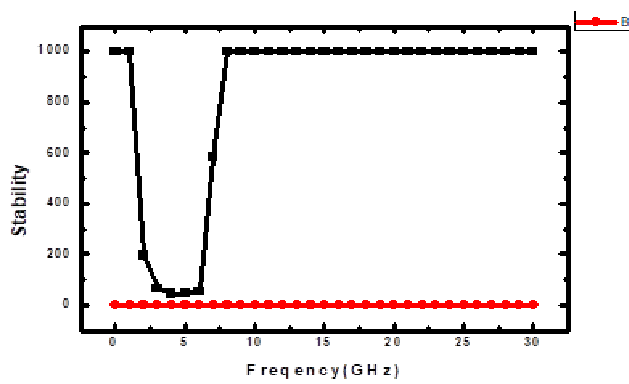

Fig. 4. Stability circuit of GaN HEMT (UMS device).

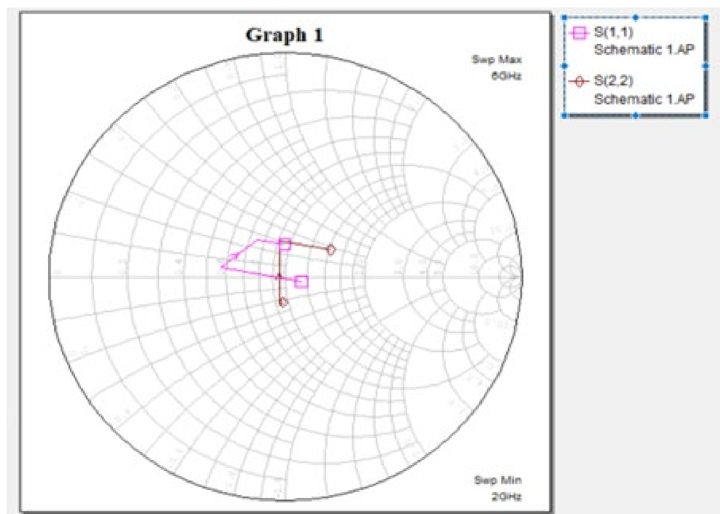

Fig. 5. Input/output matching for the three stack HEMT PA.

The concept of the addition of voltage at drain also applies in the stacking circuit using GaN HEMTs as active devices but at the drain of each GaN HEMTs, the impedance looking into the drain of the device is not real but is complex. So, between a source and drain of two consecutive stacked GaN HEMT devices, capacitive loading will come into the picture to match the drain and source impedances into optimal resistances, complex matching is required by employing the inductive cancellation of loading capacitances as shown in Fig. 6. By considering this figure admittance looking into the source of (k+1) stacked transistor can be derived by the given equation (Eq. (7)) [28]:

$$Y_{s,k+1} = \frac{1}{kR_{opt}} - \frac{sC_{ds,k+1}}{k} + \frac{sC_{gs,k+1}}{kg_{m,k+1}R_{opt}}, \qquad k=1, 2, 3,\ldots, K \tag{7}$$

The optimal impedance (Eq. (8)) at the drain of the HEMT

$$Y_{opt,k} = \frac{1}{kR_{opt}} - \frac{sC_{eqv,k}}{k}, \qquad k=1, 2, 3,\ldots\ldots\ldots, K \tag{8}$$

where $C_{eqv,k} = C_{ds,k} + kC_{dsub,k} + C_{gd,k}$, $\qquad k=1, 2, 3,\ldots\ldots\ldots, K$ (9)

From Eqs. (7) and (8), the impedance in terms of phase angle (Eq. (10)) is described by the (k+1)th transistor to the kth transistor is presented below:

$$\phi_{s,k+1} = \arctan(w(\frac{C_{gs,k+1}}{g_{m,k+1}} - C_{ds,k+1}R_{opt})) \tag{10}$$

Although the phase of optimal load (Eq. (11)) at kth drain is

$$\phi_{opt,k} = \arctan(-w(C_{eqv,k})R_{opt}) \tag{11}$$

Accordingly, to rotate the phase (Eq. (12)) of stacked admittance additional matching components are required

$$\phi_k = -\phi_{opt,k} + \phi_{s,k+1} \tag{12}$$

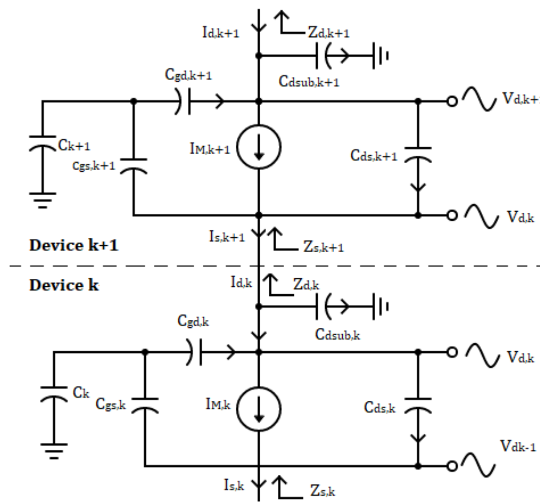

Fig. 6. Small signal model of stack HEMT Transistors in Simplified form.

For obtaining optimal performance, proper complex impedances between the transistors i.e., looking into the drain of lower GaN HEMT and source of upper GaN HEMT must be established by tuning the elements of the matching network. These elements consist of shunt-series inductors with the capacitor at the source of all stacked transistors (complex node matching). To achieve a wide bandwidth range number of sections of these matching elements have been used. The maximum phase alignment can be secured by obtaining the values of tuning elements with the help of the following equations (Eqs. (13) - (18) [28,29]:

$$\operatorname{Im}\left\{Y_{s,k+1}\right\}+\frac{1}{sL_k}=\operatorname{Im}\left\{Y_{opt,k}\right\} \quad (13)$$

$$\frac{1}{L_k}=\frac{w^2(C_{ds,k}-C_{ds,k+1})}{k}+\frac{w^2C_{gs,k+1}}{kg_{m,k+1}R_{opt}}+w^2\left(\frac{C_{gd,k}+kC_{dsub,k}}{k}\right),\ k=1,2,3,\ldots,K \quad (14)$$

$$Z_{opt,k}=kR_{opt}\,\frac{(1+sC_{eqv,k}R_{opt})}{1+(wC_{eqv,k}R_{opt})^2} \quad (15)$$

$$R^{\iota}_{opt,k}=\frac{R_{opt}}{1+(wC_{eqv,k}R_{opt})^2} \quad (16)$$

$$C^{\iota}_{k+1}=\frac{C_{gs,k+1}+C_{gd,k+1}(1+g_{m,k+1}R^{\iota}_{opt,k})}{kg_{m,k+1}} \quad (17)$$

$$L_k=kR^{\iota}_{opt,k}\,\frac{C_{gs,k+1}}{g_{m,k+1}}-kR^{\iota}_{opt,k}R^{\iota}_{opt,k}C_{ds,k+1}+kR^{\iota}_{opt,k}R_{opt}C_{eqv,k} \quad (18)$$

Equalization of voltage is done by using three methods such as by using a transformer, by using resistive feedback, and capacitive division. $(V_{gs}/V_{ds})_{CS} = (V_{gs}/V_{ds})_{CG}$ Similarly, current equalization is done by current correction using grounded capacitor at the source of each common gate HEMT, using drain to source capacitor at each common gate HEMT, and using drain of each transistor to the output port. To transfer maximum power from CS to CG HEMT the impedance looking into the drain of CS HEMT should be the complex conjugate of the impedance looking into the source terminal of CG HEMT.

4. Results and Discussion

In stacked HEMT configuration, power at the top of the HEMT will add up normally only when the voltage and current at the drain electrodes of the stacking HEMTs are aligned or having almost zero angles between them. This means there exists dominantly a resistive part at the drain electrodes of the HEMT. Looking into the HEMT model from the drain electrode side at the frequency of operation only complex impedance can be found, so to obtain V_{opt} corresponding to which we get aligned current and voltage waveform (Figs. 7 and 8) a matching network is required so that the reflections of power is minimized. The matching network is required to be attached to the right side of the drain electrode so that the complex part of the impedance looking into the drain is cancelled out by the complex part of the impedance looking into the matching circuit.

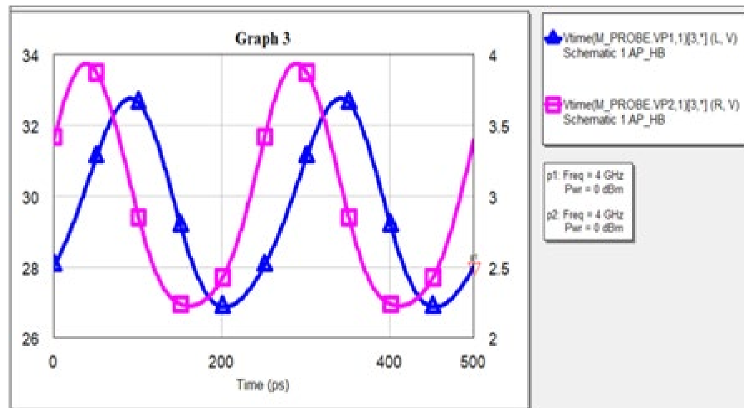

Fig. 7. Simulated voltage waveforms of three stack PA.

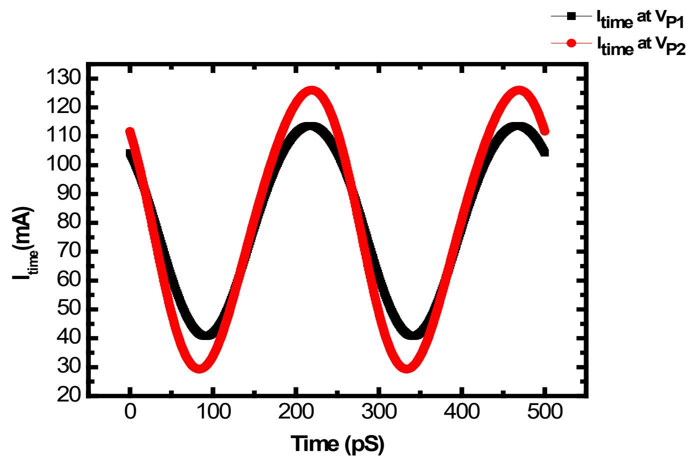

Fig. 8. Simulated current waveforms of three stack PA at 4 GHz when P_{in}=0 dBm.

As the input power is increased, distortion in the output voltage signal appears. When the voltage swings are made aligned with each other at the stacking GaN HEMTs drain electrodes, the distortion further increases due to the increase in output power. This is shown in Figs. 9 and 10 displaying voltage and current distorted waveforms. To reduce the distortion, a small relative phase between the voltage swings at the GaN HEMT stacking drains are introduced intentionally so that output power is slightly reduced (Figs. 7 and 8).

As shown in Fig. 11, input/output return loss is obtained higher than 13 dB from the 2 to 6 GHz range. Figure 12 depicts small signal and large signal gain as a function of frequency. UMS device of size 125x6 is characterized for P_{out} and PAE as shown in Figs. 13 and 14. For obtaining high power and high efficiency in the microwave power amplifier, the GaN HEMT's are driven into nonlinear region of operation, i.e., saturation region which causes the occurring of harmonic distortions as shown in Fig. 15.

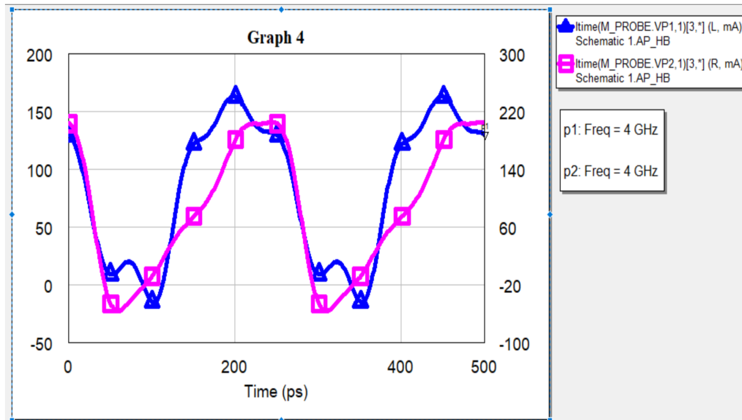

Fig. 9. Distorted current waveforms when output power is in saturation region.

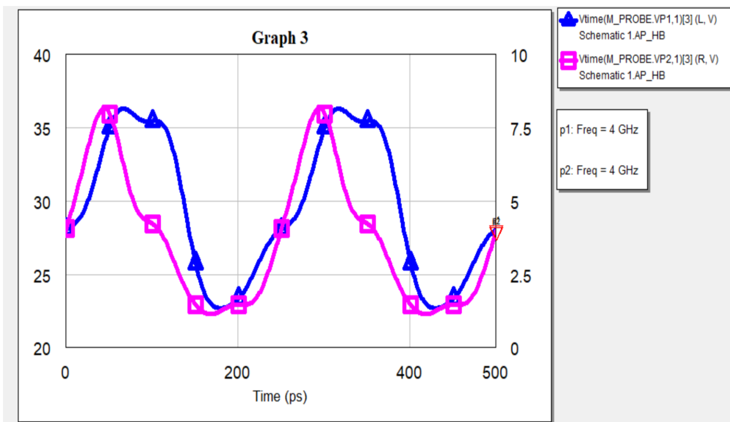

Fig. 10. Distorted voltage waveforms when output power is in saturation region.

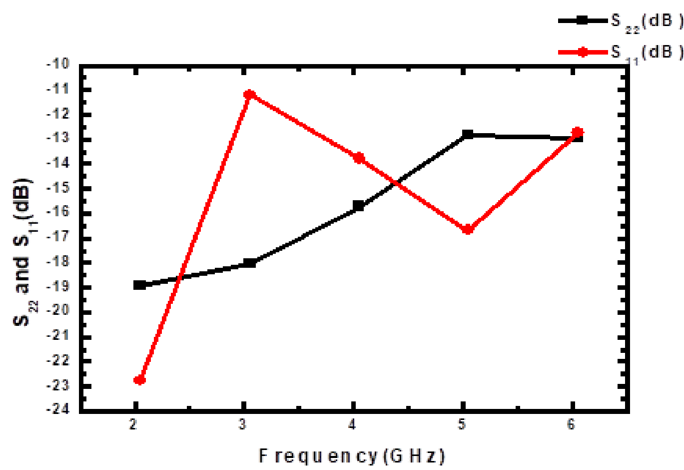

Fig. 11. Simulated S_{11} and S_{22} for three stack HEMT PA.

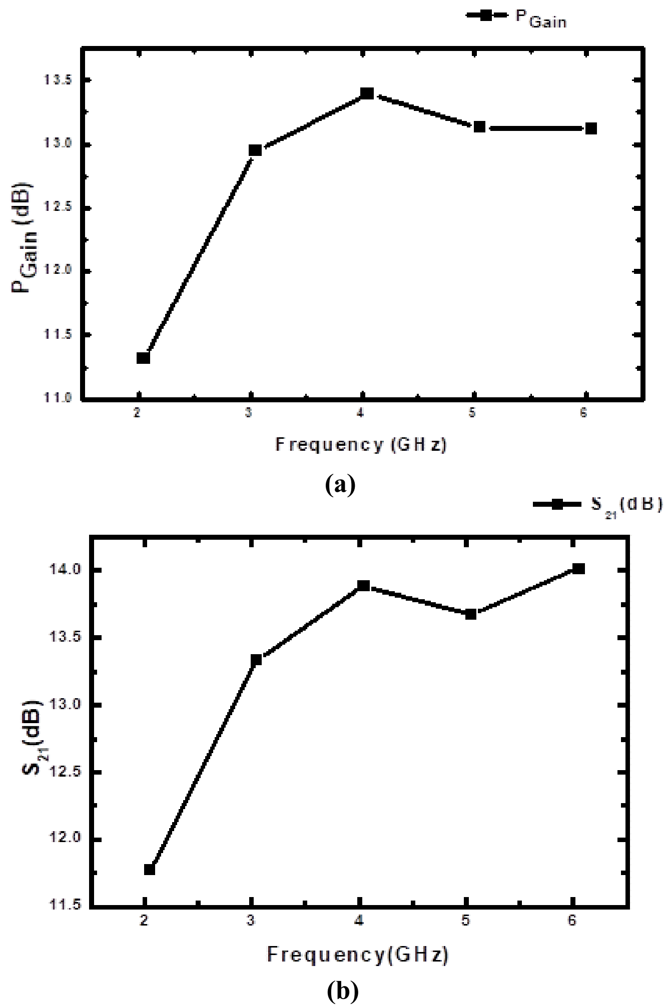

Fig. 12. (a) Large and (b) small signal gain of three stack power amplifier.

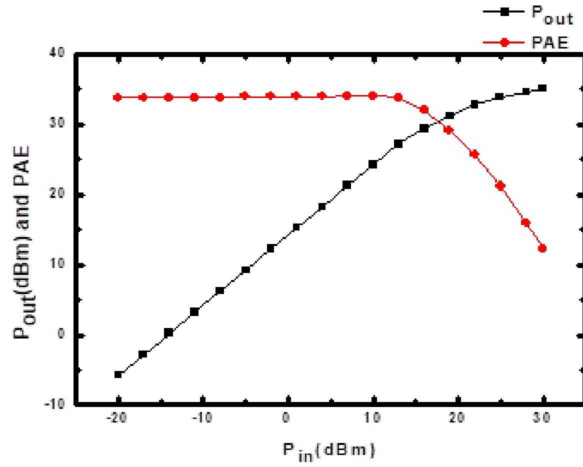

Fig. 13. P_{out} and PAE of the HEMT Device (UMS).

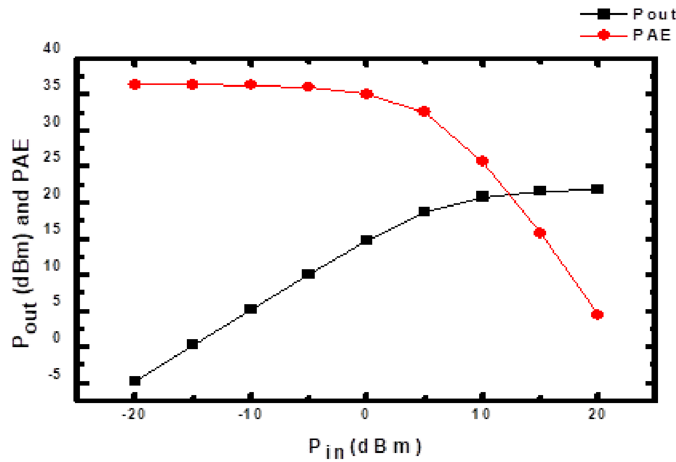

Fig. 14. P_{out} and PAE of the three-stack power amplifier.

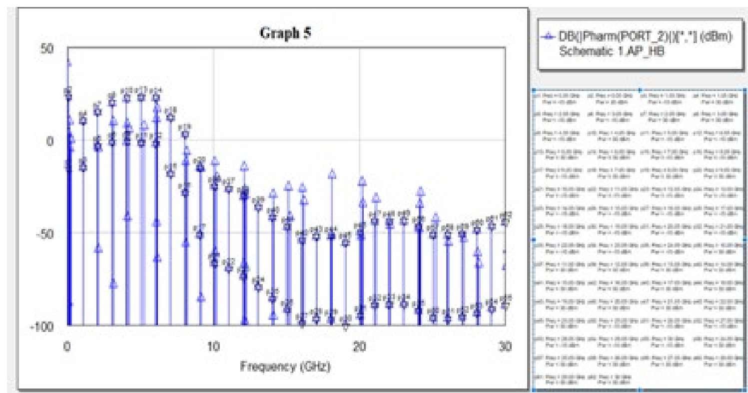

Fig. 15. Harmonic distortion of three-stack power amplifier.

As predicted P_{out} is initially increasing linearly with respect to P_{in} and then going into saturation or compression. There, it remains almost constant at the level of 35 dBm at P_{in} = 30 dBm. So PAE almost remains constant initially since both P_{out} and P_{in} are increasing almost linearly and P_{DC} being constant (Fig. 16). Later on, as P_{in} increases further, PAE drops down in the saturation/compression region since P_{out} stops increasing linearly with P_{in}.

Buffer amplifier follows the same pattern as that of GaN HEMT device for P_{out} and P_{in}. In stacking, topology voltages are adding as one goes up the stack. Hence, the P_{out} increases because of the increase in the voltage swing at the drain of each stacked GaN HEMT device whereas the current is almost equally distributed in the stacking GaN HEMTs. Therefore, output power for the stacked amplifier will show the same pattern as that of the buffer amplifier and the device.

Performance analysis of the complete circuit of stacked power amplifier design has been carried out separately and optimized. The layout of the schematic (Fig. 17) is generated. Table 2 summarizes the stacked power amplifier's performances whereas the presented one is compared with other published literature.

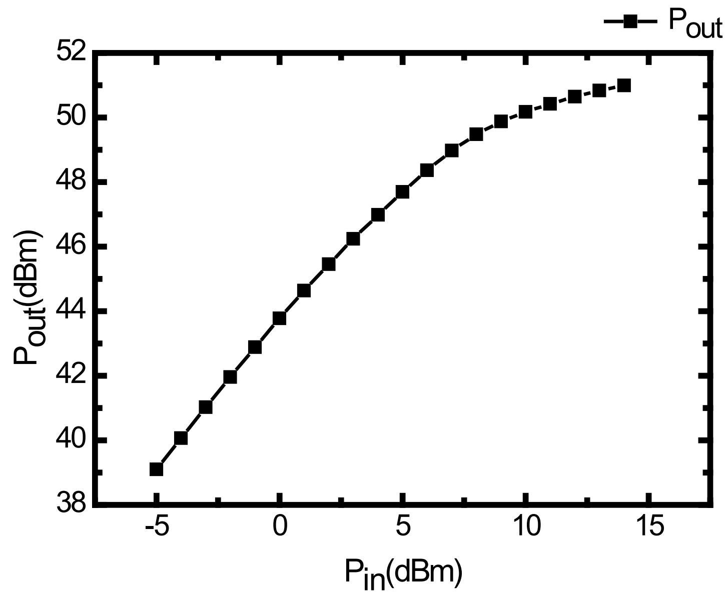

Fig. 16. P_{out} of the three-stack power amplifier (P$_{in}$ is applied as 0 dBm then the P_{out} is obtained as 43 dBm).

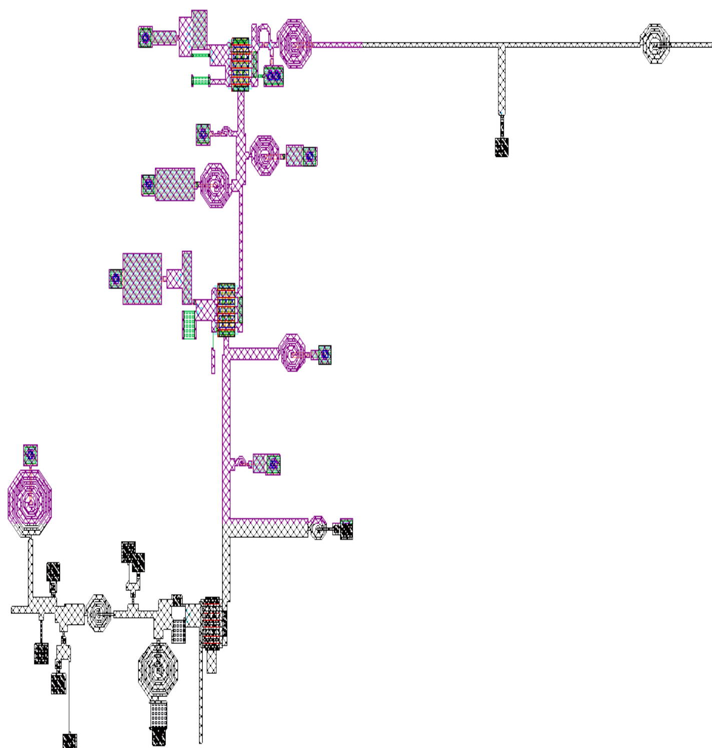

Fig. 17. Final Layout of the three-stack GaN HEMT PA.

Table 2. Comparative study of references.

S. No.	Class of operation	Frequency (GHz)	Power (dBm)	PAE (%)	Gain (dB)
1	CMOS, Class AB [25]	45	18.6-19.4	32-33.9	9.5
2	CMOS, Class A [30]	86-94	15.8	11	10.2
3	CMOS, Class A [29]	91	19.2	14	12.4
4	CMOS, Class A [27]	41-46	21.6-15.9	25.1-32.7	8.9-9.4
5	FET, Class AB [15]	1.9	33	47	13.2
6	CMOS, Class AB [16]	1.9	29.4-28.5	41.4-38.7	14.6
7	CMOS, Class A [14]	45	16.8-19	20-23	7.1-8
8	CMOS [23]	2-16	18.5-15	9-17	10
9	GaAs pHEMT [22]	4-10	35-37	25-32	13.5
10	FET, Class A [21]	0.9	30.2	35	NA
11	HBT [31]	1.6	12	23.5	32.6
12	mHEMT [17]	60	20	19	16
13	CMOS [27]	88-90	17.3	9	8
14	CMOS, Class A [24]	6-26	26.1	20.5	6
15	CMOS, Class E [13]	47.5	17.6	34.6	13
16	HBT, Class AB [32]	3.5	22	65	NA
17	CMOS [19]	24	17.5	20.5	12.2
18	HBT [18]	4.8 5.2 5.8	26 23.4 20	38 24 18	12 12 12
19	Bi CMOS [20]	2	27.3	34	23.8
20	CMOS [26]	57-85	18	20	12
This work	GaN HEMT, Class A	2-6	43	35	14

5. Conclusions

In this study, a single-stage three-stacked HEMT power amplifier has been designed for broadband applications. It has been shown that the gate resistance restricts the RF current swing in stacked FET power amplifiers. Hence, this limitation has been reduced in the proposed multi-drive stacked HEMT power amplifier. High power amplifiers, which have been facing several challenges, such as the output performance degradation attributed to parasitic effects, have been solved.

The proposed power amplifier was simulated using UMS PDK of 0.25µm process. The saturated output power of 40 dBm and PAE of 35% for a bandwidth of 2-6 GHz range is now successfully proved with a much-improved design than the earlier work, which also has used the same technique of FET as well as GaAs HEMT geometry. The return loss at output and input is found to be -13 and -13 dB over the entire range of operation.

The design presented is ideally suitable for both defence and commercial applications. To be confident about amplifier robustness, the design developed was verified, which indicated an outstanding RF performance viz. a viz. simulated and EM results.

Nomenclatures

A_v	Voltage Gain
C_1, C_2, C_3, C_4	Capacitances
C_{ds}	Drain-Source Capacitance
C_{gs}	Gate-Source Capacitance
C_{gd}	Gate-Drain Capacitance
C_{eqv}	Equivalent Capacitance
C_{dsub}	Dielectric Substrate Capacitance
ε_r	Relative Dielectric Constant
f_o	Operational Frequency
f_T	Transitional Frequency
g_m	Trans-conductance
I_m	Maximum Current
I_{max}	Maximum Current
L_k	Inductance at k^{th} value
P_{out}	Output Power
P_{in}	Input Power
P_{DC}	DC Power
R_{opt}	Optimum Resistance
R_L	Load Resistance
V_{dd}	Drain Voltage
V_k	Knee Voltage
V_{gs}	Gate-Source Voltage
V_{ds}	Drain-Source Voltage
V_{gd}	Gate-Drain Voltage
V_{opt}	Optimum Voltage
Y_s	Source Admittance
Y_{opt}	Optimum Admittance
Z_L	Load Impedance
Z_{in}	Input Impedance

Greek Symbols

φ_s	Source Phase
φ_{opt}	Optimum Phase
φ_k	Phase at k^{th} Value

Abbreviations

AWR	Applied Wave Research
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CS	Common Source
DC	Direct Current
EM	Electromagnetic
FET	Field Effect Transistor
GaN	Gallium Nitride
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Junction
HEMT	High Electron Mobility Transistor
MESFET	Metal Semiconductor Field Effect Transistor
mHEMT	Metamorphic High Electron Mobility Transistor
PA	Power Amplifier
PAE	Power Added Efficiency
PDK	Process Design Kit
RADAR	Radio, Detection and Ranging
RF	Radio Frequency
SSPA	Solid State Power Amplifier
T-Lines	Transmission Lines
UMS	United Monolithic Semiconductor
Wi-Fi	Wireless Fidelity

References

1. Chen, S.; Reese, E.; and Nguyen, T. (2012). A compact 70-Watt power amplifier MMIC utilizing S-band GaN on SiC HEMT process. 2012 *IEEE Compound Semiconductor Integrated Circuit Symposium* (*CSICS*), La Jolla, CA, USA, 1-4.
2. Dhanya, H.R.; Hu, W.; Ahmed, A.; Nawaz, H.; and Waseem, M. (2019). High efficiency GaN HEMT class F power amplifier for S-band telemetry application. *Proceedings of* 2019 *Photonics & Electromagnetics Research Symposium - Fall* (*PIERS - Fall*), *Xiamen*, *China*, 3283-3288.
3. Kikuchi, K.; Nishihara, M.; Yamamoto, H.; and Mizuno, S. (2015). An X-band 300-watt class high power GaN HEMT amplifier for radar applications. *SEI Technical Review* (*Info-Communication*), 40-44.
4. Maassen, D.; Rautschke, F.; Ohnimus, F.; Schenk, L.; Dalisda, U.; and Boeck. G. (2017). 70 W GaN-HEMT Ku-band power amplifier in MIC technology. *IEEE Transactions on Microwave Theory and Techniques*, 65(4), 1272-1283.
5. Maekawa, A.; Nagahara, M.; Yamamoto, T.; and Sano, S. (2006). A 100W high-efficiency GaN HEMT amplifier for S-band wireless system. *Proceedings of* 2005 *European Microwave Conference*, Paris, France, 2-5.
6. Nakatani, K.; and Ishizaki, T. (2015). A 2.4 GHz band 100W GaN HEMT high efficiency power amplifier for microwave heating. *Journal of Electromagnetic Engineering and Science*, 15(2), 82-88.
7. Zhou, X.Y.; Chan, W.S.; Zheng, S.Y.; Feng, W.; Liu, H.-Y.; Cheng, K.-K.M.; Liu, H.-Y.; and Ho, D. (2019). A mixed topology for broadband high-efficiency

Doherty power amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 67(3), 1050-1064.

8. Qin, G.; Xiaojuan, C.; Weijun, L.; Tingting, Y., Lei, P.; and Xinyu, L. (2011). A Ku-band high power density AlGaN / GaN HEMT monolithic power amplifier. *Journal of Semiconductors*, 32(8), 085001, 1-4.
9. Takagi, K.; Masuda, K.; Kashiwabara, Y.; Sakurai, H.; Matsushita, K.; Takatsuka, S.; Kawasaki, H.; Takada, Y.; and Tsuda, K. (2006). X-band AlGaN / GaN HEMT with over 80W output power. *Proceedings of* 2006 *IEEE Compound Semiconductor Integrated Circuit Symposium*, San Antonio, TX, USA, 265-268.
10. Virdee, A.; Virdee, B.; and Ahmed, K. (2017). High power GaN amplifier for high efficiency applications. *ARMMS April Conference*, Oxfordshire, USA, 1-4.
11. Wang, Y.; and Wang, P. (2011). A high-efficiency power amplifier using GaN HEMTs. Proceedings of 2011 *International Conference on Electronics, Communications and Control* (*ICECC*), Ningbo, China, 1815-1817.
12. Zhang, H.; Gao, H.; and Li, G.P. (2005). Broad-band power amplifier with a novel tunable output-matching network. *IEEE Transactions on Microwave Theory and Techniques*, 53(11), 3606-3614.
13. Chakrabarti, A.; and Krishnaswamy, H. (2014). High-power high-efficiency class-E-Like stacked mmwave PAs in SOI and bulk CMOS: Theory and implementation. *IEEE Transactions on Microwave Theory and Techniques*, 62(8), 1686-1704.
14. Pornpromlikit, S.; Dabag, H.-T.; Hanafi, B.; Kim, J.; Larson, L.E.; Buckwalter, J.F.; and Asbeck, P.M. (2011). A Q-band amplifier implemented with stacked 45nm CMOS FETs. *Proceedings of* 2011 *IEEE Compound Semiconductor Integrated Circuit Symposium* (*CSICS*), Waikoloa, HI, USA, 1-4.
15. Pornpromlikit, S.; Jeong, J.; Presti, C.D.; Scuderi, A.; and Asbeck, P.M. (2009). A 33dBm 1.9 GHz silicon on insulator CMOS stacked FET power amplifier. *Proceedings of* 2009 *IEEE MTT-S International Microwave Symposium Digest*, Boston, MA, USA, 533-536.
16. Pornpromlikit, S.; Jeong, J.; Presti, C.D.; Scuderi, A.; and Asbeck, P.M. (2010). A watt-level stacked-FET linear power amplifier in silicon-on-insulator CMOS. *IEEE Transactions on Microwave Theory and Techniques*, 58(1), 57-64.
17. Kim, J.; Koh, Y.; Lee, S.; Jeong, J.; Seo, K.; and Kwon, Y. (2011). A 60 GHz broadband stacked FET power amplifier using 130 nm metamorphic HEMTs. *IEEE Microwave and Wireless Component Letters*, 21(6), 323-325.
18. Lei, M.-F.; Tsai, Z.-M.; Lin, K.-Y.; and Wang, H. (2007). Design and analysis of stacked power amplifier in series input and series-output configuration. *IEEE Transactions on Microwave Theory and Techniques*, 55(12). 2802-2812.
19. Chang, J.; Kim, K.; Lee, S.; and Nam, S. (2011). 24 GHz stacked power amplifier with optimum inter-stage matching using 0.13µm CMOS process. *Proceedings of* 2011 3*rd International Asia-Pacific Conference on Synthetic Aperture Radar* (*APSAR*), Seoul, South Korea. 885-887.
20. Fritsche, D.; Wolf, R.; and Ellinger, F. (2012). Analysis and design of a stacked power amplifier with very high bandwidth. *IEEE Transactions on Microwave Theory and Techniques*, 60(10), 3223-3231.

21. McRory, J.G.; Rabjohn, G.G.; and Johnston, R.H. (1999). Transformer coupled stacked FET power amplifiers. *IEEE Journal of Solid-State Circuits*, 34(2), 157-161.
22. Wu, H.; Liao, X.; Wang, C.; Chen, Y.; Hua, Y.; Hu, L.; Lv, J.; and Tong, W. (2017). A 4-10 GHz fully-integrated stacked GaAs pHEMT power amplifier. *Proceedings of* 2017 *IEEE MTT-S International Microwave Symposium* (*IMS*), Honolulu, HI, USA, 24-26.
23. Tarar, M.M.; Beucher, T.; Qayyum, S.; and Negra, R. (2017). Efficient 2-16 GHz flat-gain stacked distributed power amplifier in 0.13µm CMOS using uniform distributed topology. *Proceedings of* 2017 *IEEE MTT-S International Microwave Symposium* (*IMS*), Honolulu, HI, USA, 27-30.
24. Chen, J.-H.; Helmi, S.R.; Azadegan, R.; Aryanfar, F.; and Mohammadi, S. (2013). A broadband stacked power amplifier in 45-nm CMOS SOI technology. *IEEE Journal of Solid-state Circuits*, 48(11), 2775-2784.
25. Agah, A.; Dabag, H.; Hanafi, B.; Asbeck, P.; Larson, L.; and Buckwalter, J. (2012). A 34% PAE, 18.6dBm 42-45GHz stacked power amplifier in 45nm SOI CMOS. *Proceedings of* 2012 *IEEE Radio Frequency Integrated Circuits Symposium*, Montreal, QC, Canada, 57-60.
26. Ning, K.; and Buckwalter, J.F. (2018). An 18dBm, 57 to 85-GHz, 4-stack FET power amplifier in 45-nm SOI CMOS. *Proceedings of* 2018 *IEEE/MTT-S International Microwave Symposium – IMS*, *Philadelphia*, *PA*, *USA*, 1453-1456.
27. Jayamon, J.; Agah, A.; Hanafi, B.; Dabag, H.; Buckwalter, J.; and Asbeck, P. (2013). A W-band stacked FET power amplifier with 17 dBm Psat in 45-nm SOI CMOS. *Proceedings of* 2013 *IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications*, Austin, TX, USA, 256-258.
28. Dabag, H.-T.; Hanafi, B.; Golcuk, F.; Agah, A.; Buckwalter, J.F.; and Asbeck, P.M. (2013). Analysis and design of stacked-FET milli-meter wave power amplifier. *IEEE Transactions on Microwave Theory and Techniques*, 61(4), 1543-1556.
29. Agah, A.; Jayamon, J.A.; Asbeck, P.M.; Larson, L.E.; and Buckwalter, J.F. (2014). Multi-drive stacked-FET power amplifiers at 90 GHz in 45 nm SOI CMOS. *IEEE Journal of Solid-State Circuits*, 49(5), 1148-1157.
30. Agah, A.; Jayamon, J.A.; Asbeck, P.M.; Buckwalter, J.F.; and Larson, L.E. (2013). A 11% PAE, 15.8dBm two-stage 90-GHz stacked-FET power amplifier in 45-nm SOI CMOS. *Proceedings of* 2013 *IEEE MTT-S International Microwave Symposium Digest* (*MTT*), Seattle, WA, USA, 13-15.
31. Luong, M.D.; Ishikawa, R.; Takayama, Y.; and Honjo, K. (2016). Microwave characteristics of an independently biased 3-stack InGaP/GaAs HBT configuration. *IEEE Transactions on Circuits and Systems*, 64(5). 1140-1151.
32. Nguyen, H.H.; Luong, D.M.; and Bach, G.D. (2019). A novel independently biased 3-stack GaN HEMT configuration for efficient design of microwave amplifiers. *Applied Sciences*. 9(7), 1510, 1-16.