ANALYSIS OF SHORT CHANNEL EFFECTS IN MULTIPLE-GATE \((n, 0)\) CARBON NANOTUBE FETS

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Abstract

The Carbon NanoTube Field Effect Transistor (CNTFET) is a decent alternative to nanometre scaling of device limitations. In this research work, Double-Gate (DG) CNTFET and Tri-Gate (TG) CNTFET have been simulated using the three-dimensional Poisson and Schrodinger solvers by Non-Equilibrium Green’s Function (NEGF) and influence of the short channel effects on DG-CNTFET and TG-CNTFET have been analysed. First, the authors have analysed the effects of carbon nanotube diameter \((d_{CNT} \sim 2 \text{ nm}-4 \text{ nm})\) and the gate contact length \((L_g \sim 5 \text{ nm}-25 \text{ nm})\) variations on Field-effect mobility \((\mu_{FE})\), Conductance, Subthreshold-Swing \((SS)\), DIBL, and \((I_{ON}/I_{OFF})\) current ratio of DG-CNTFET and TG-CNTFET. The results show that the increase in \(d_{CNT}\) increases the \(I_{ON}\) and \(\mu_{FE}\). Further, the comparison of gate voltage with channel capacitance has been made at different oxide thicknesses in both the DG and TG structures. The DG-CNTFET can achieve a high \(I_{ON}/I_{OFF}\) ratio. The simulation results report that the double-gate device offers promising \(SS\) value and the \(DIBL\), which improves with an increase in channel length and diameter of CNT.

Keywords: Carbon nanotube, CNTFETs, Multigate structures, Nanotechnology, NEGF, Short-channel effects, VLSI.
1. Introduction

The conventional MOSFETs are approaching the limits due to strict adherence to the short channel effects, and exhibit poor performances at nanometer scaling of the device. The concurrent miniaturization of electronic devices has led the semiconductor industry to step forward in technological progression. However, the integrated circuits, which follow Moore [1] law, in which, have become so smaller that scaling of the conventional MOSFET has become much complicated. The device performance and fabrication suffer from adverse short channel effects when it is subjected to further down-scaling. In situation, adopting newer material, techniques, or structures have only been the solution to a certain extent of the scalability. In recent years, many researchers have paid attention towards exploring other channel material in devices for seeking improvements, particularly in nanoscale regime. Subsequently, carbon nanotube (CNT) transistors [2], silicon nanowire transistors [3], Cylindrical surrounding double-gate [4], FinFETs [5] and graphene-nano-ribbon transistors originated for resolving the scaling issues of conventional transistors.

Although many challenges are accompanying with the scaling, yet the technological developments are consistent. Thus, the researchers have been looking for finding the improvements in carrier transport of the device channel region. Carbon nanotubes (CNTs) are capable of realizing the high mobility of the channel. Because of their superior electronic properties, they are amongst the preferable choice for use in channel material in FETs [6] and becoming increasingly popular these days in several applications [7].

The CNTFETs have undergone many structural changes for achieving performance improvement since its introduction in 1998. After the invention of nanotubes by Iijima [8], CNTFETs have prolonged substantial progress in terms of modelling of the devices, which explored what the physical dimension of the transistors must abide by specific rules [9-15] to keep the Drain Induced Barrier Lowering (DIBL) up to an acceptable level [16]. Besides, this has been reported that the transistors are more efficient when it has multiple gates for producing independent potential, which provide more control over the gate.

In this work, authors present the impact of short-channel effects on different multiple gate structure in CNTFETs of Double-Gate (DG) and Triple-Gate (TG) CNTFET using simulation by three-dimensional Poisson and Schrodinger solvers within the non-equilibrium green function [17-19]. In which, first the authors have analysed the effects of carbon nanotube diameter ($d_{CNT} \sim 2 \text{ nm} - 4 \text{ nm}$) and the gate length variation ($L_g \sim 5 \text{ nm} - 25 \text{ nm}$) of the double-gate structure in terms of Field-effect mobility ($\mu_{FE}$), Conductance ($G$), Subthreshold-Swing ($SS$), DIBL and $(I_{ON}/I_{OFF})$ current ratio parameters. Later on, the achieved results of TG-CNTFETs are compared with the electrical characteristics of DG-CNTFET.

This paper is organized as follows. The dimensional description of the DG and TG CNTFET is given in Section 2. Section 3 describes the simulation methodology of the proposed device. Section 4 provides the results of the simulation and discuss the obtained result. Finally, Section 5 presents the conclusion and future scope of the work.
2. Structural description

The CNTFETs have been introduced as one of the sustainable transistors in the ultra-low scales, which maintains high performance. The CNTFETs differ from MOSFETs because of carbon nanotubes (CNTs) as a channel instead of Silicon. This CNT channel makes it possible to deliver higher current density and transport considerable current carrier mobility compared to the bulk Silicon. Carbon nanotubes, usually, are of two types (i) Multi-Wall (MW) or (ii) a Single-Wall (SW).

The SWNT are structured from one-atom-layer of graphite known as Graphene, formed by enfolding the sheet into a unified cylinder. Figure 1 shows the Multi-wall and single-wall carbon nanotube structures. A single-wall CNT (SWCNT) has one cylinder, makes the manufacturing of tube simple; therefore, they are prevalent. In addition, the easy fabrication process of SWCNTs makes them suitable. The tube length of the SWNT structure is much larger in comparison to the diameter of the tube.

The schematic of double-gate CNTFET and Tri-gate CNTFET is shown in Figs. 2 and 3, respectively. DG CNTFETs have two gates on either side surrounding the CNT channel. The lengths \( L_{ch} \), \( L_{D} \), and \( L_{S} \) correspond to the channel, drain to channel interface, and source to channel interface, respectively, and \( t_{ox1} \) and \( t_{ox2} \) are the oxide thicknesses of gate terminals 1 and 2. In contrary, the TG-CNTFET has top-metal electrode covering three sides of the structure as shown in Fig. 3.

If it does not follow, it acts as a semiconductor. The diameter of the CNT can be calculated from Eq. (1) [20].

\[
d_{\text{CNT}} = a_o \frac{a_{cc}}{\pi} \sqrt{n^2 + m^2 + mn} \tag{1}
\]

where \( a_o = a_{cc} \cdot 3^{1/2} \) is the length of the basis vector, and \( a_{cc} \approx 1.42 \) A is the nearest neighbour C-C bonding distance.

![Fig. 1. Multi-wall and single-wall carbon nanotube structure.](image)
3. Simulation Method

Based on Dargar and Srivastava [20], Guo et al. [21], Data [22, 23] and Lake et al. [24], the methodology has been accomplished from the solution of Poisson-Schrodinger equation at the open boundary with NEGF for geometrical and device physics measurements.

The electron-hole concentrations are calculated by solving the Schrodinger equation and Eq. (2) represents Green’s function [22, 23],

\[
G(\epsilon) = [\epsilon I - H - \Sigma_S - \Sigma_D]^{-1}
\]  

(2)

where \( \epsilon \), \( I \), and \( H \) are the energy, unitary matrix, and the Hamiltonian of the tube, respectively and \( \Sigma_S \) and \( \Sigma_D \) are the drain and source self-energy matrix.

If there are \( m \) number of carbon atoms in the nanotube, then the Hamiltonian would be \( m \times m \) and as indicated in Eq. (3), irrespective to the term of \( \Sigma_{scat} \) connected to the electrons scatter, comprehensive ballistic for simulating the device behaviour is taken into account. The entire array of self-energy matrix \( \Sigma_S \) becomes 0 except the array (1,1), given as Eq. (3) [24],

\[
\Sigma_S(1,1) = \frac{(\epsilon - \epsilon_i)^2 + r^2 + b^2_{in}}{2(\epsilon - \epsilon_i)} - \frac{\sqrt{[(\epsilon - \epsilon_i)^2 + r^2 + b^2_{in}]^2 - 4(\epsilon - \epsilon_i)^2 r^2}}{2(\epsilon - \epsilon_i)}
\]  

(3)
Without the loss of generalization, the DG-CNTFET and TG-CNTFET in a coaxial gate geometry are depicted in Figs. 2 and 3 for the DG-CNTFET 25 nm channel length are distributed in three portions. The one of either channel has control of gate surrounding the prime gate, which controls the centre part and responsible for switching ON and OFF the CNT channel. Same gate length in each part is assumed, i.e., 15 nm, to generalize the expression. The prime and polar gates are idealistically inaccessible to each other and the separation distance is neglected. Eq. (4) displays drain current derived from Landauer formula [25].

\[
I_d = \frac{2Q v_F}{\hbar} \int_{-\infty}^{+\infty} (f(e-e_{FD}) - f(e-e_{FS}))T(e)de
\]  

(4)

where \( I_d, \hbar, \) and \( f \) represents Drain current, Planck’s constant, and the Fermi-function, respectively, and \( e_{FS} \) and \( e_{FD} \) are the Fermi levels in Source and the Drain, respectively. The Transmission Coefficient \( T(e) \) refers to the probability of the carriers reaching from one contact to the other. The transmission coefficient \( T(e) \) in the Landauer formula is obtained by merging \( T_{center}, T_{left}, \) and \( T_{right} \) as given in Eq. (5).

\[
T(e) = \frac{T_{left} * T_{right} * T_{center}}{T_{left} * T_{right} + T_{left} * T_{center} + T_{right} * T_{center} - 2T_{left} * T_{right} * T_{center}}
\]

(5)

where \( T_{center} \) is transmission coefficient that denotes whether a carrier has adequate energy to flow above the barrier created by the primary gate at the channel’s centre, and \( T_{left} \) and \( T_{right} \) are the transmission coefficient at the source and drain, it corresponds to the probability if a carrier has enough energy to enter in the channel. \( T_{center} \) has only thermionic conduction, however, \( T_{left} \) and \( T_{right} \) are assumed to conduct due to both thermionic and tunnelling. Svizhenko et al. [26] mentioned that the tunnelling probability of \( T_{left} \) and \( T_{right} \) are assessed as shown in Eq. (6) using the WKB approach.

\[
T_{left/right} = \exp \left[ -2 \int_{z_{initial}}^{z_{final}} k_z(z)dz \right]
\]

(6)

where \( z_{initial} \) and \( z_{final} \) are the classical bending points and \( k_z \) refers to parallel momentum, which is determined by the \( \epsilon-k \) bonding of CNT [27].

The transmission coefficient variation with respect to the classical bending points in the \( z \)-direction of the TG-CNTFET and DG-CNTFET channels are displayed in Fig. 4. In this work, both Shockley-Read-Hall and CVT models have been consolidated as physical models of MOS-type transistors.

NEWTON and GUMMEL program select models are utilised for calculation. For obtaining drain current and \( V_{GS} \) curve, each step bias point and swept bias points are comprehended, and resulting log file is saved (.log extension) as a solution. The outputs (.logfile) have been loaded and sloped to perform variation in gate voltage.

The simulation altogether should self-consistent with the Poisson rule. The coaxial-gate CNTFET gives theoretically superior gate-control of the channel. Heavily doped Source-Drain, CNTs, and the gate control the channel conductivity similar to a Si-MOSFET.
The transistor characteristics are extensively influenced by quantum transport and electrostatics. Hence, the iteration between the NEGF and Poisson equation is performed. In short, the steps are as follows. First, the Poisson equation has been solved by the simulator to obtain the electrostatic potential in the CNT channel for a given charge density. Then the potential profile has been computed and input to the NEGF equation. The process provides an improved approximation of charge densities. The Poisson and the NEGF transport calculates reiteration till the self-consistency is obtained and result in the current for potential profiles.

**Fig. 4. Transmission coefficients of DG-CNTFET and TG-CNTFET.**

### 4. Results and discussion

In this work, authors have used, zigzag CNT, which has a diameter of 1 nm placed in SiO$_2$. An intrinsic part of the nanotube of variable length $L$ acts as a channel with end terminals at both the side are doped with $n$-type dopants. These two ends of length $L_S = L_D = 5$ nm are the source and the drain. Using the electronic simulator, the DG-CNTFET is simulated each time keeping $d_{CNT} = 2$ nm for the values of $L_g = 5$ nm, 15 nm, 20 nm, and 25 nm, respectively. It is noteworthy in Fig. 5, which the field-effect mobility ($\mu_{FE}$) increases at a decrease in gate length as the channel becomes narrower at reduced gate length and offers higher drift to the charge carriers.

**Fig. 5. Field-effect mobility vs. charge density at different $L_g$.**
Figure 6 shows that the $\mu_{FE}$ also increases with increase in CNT diameter, however, it is opposed by charge carriers, i.e., as the charge density increases, the field-effect mobility also increases gradually in comparison to the initial charge density. The effect of charge density variation on the device conductance at various gate-lengths is shown in Fig. 7.

The comparison of conductance at different gate length shows that the initial charge densities do not affect the conductance significantly, however, further increases carrier charge density continually. High conductance can be seen at the smallest gate length, yet it does not follow the linearity at increasing gate lengths.

Similarly, the impact on the conductance w.r.t. increasing carrier concentration at the different CNT diameters are shown in Fig. 8. Increased CNT diameter provide large channel area and offer higher conductance at $d_{CNT} \sim 4$ nm in comparison to the $d_{CNT} \sim 2$ nm. The two critical measures of short channel effects (SCEs) in semiconductor devices are Drain-Induced-Barrier-Lowering (DIBL) and Subthreshold Swing (SS). Figure 9 depicts the transfer characteristics of DG-CNTFET of gate length $L_g \sim 15$ nm with oxide thickness 1 nm at drain voltage $V_d = 0.1$ V and $V_d = 0.5$ V, respectively as obtained from simulation results. In the same way, the transfer characteristics of the TG-CNTFET with a gate length $L_g \sim 15$ nm and oxide thickness of 1 nm at drain voltage $V_d = 0.1$ V and $V_d = 0.5$ V, are depicted in Fig. 10.

![Fig. 6. Field-effect mobility vs. charge density at different $d_{CNT}$.](image1)

![Fig. 7. Conductance vs. charge density at different $L_g$.](image2)

![Fig. 8. Conductance vs. charge density at different $d_{CNT}$.](image3)

![Fig. 9. Transfer characteristics of DG-CNTFET.](image4)
The Subthreshold-Swing (SS), which is the rate of increment in the current below its threshold at an applied gate voltage, is stated as the mV of the voltage required for the increase of drain current in decibel, given as Eq. (7) [15, 28].

$$SS = \frac{dV_G}{d(\log_{10} I_D)}$$  \hspace{1cm} (7)

For a MOSFET, Subthreshold slope is given as \((k_B T/q)\log I_D\). For analysing the device performance, SS and \(I_{ON}/I_{OFF}\) parameters have been extracted from the I-V characteristics of both the devices. Figure 11 shows the comparison of Subthreshold Swing oscillation of DG-CNTFET and TG-CNTFET.

Figure 12 represents the comparison of \(I_{ON}/I_{OFF}\) current-ratio computed from simulation results of both the device, where the nearly equal ON-OFF current ratio is obtained at \(L_g \sim 22\) nm. Comparatively, it has been observed that TG-CNTFET upholds a wide range of gate length (14 nm-26 nm) during which, higher \(I_{ON}/I_{OFF}\) is obtained. Further, the simulation is performed by varying the oxide thickness of the gate to \(t_{ox1} \sim 0.5\) nm, 0.8 nm, 1.2 nm and 2 nm to know the quantum capacitance variation with the gate voltage applied.

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**Fig. 10.** Transfer characteristics of TG-CNTFET.

**Fig. 11.** SS oscillation of TG and DG-CNTFET at various \(L_g\).

**Fig. 12.** \(I_{ON}/I_{OFF}\) for TG and DG-CNTFET.
The channel field does not only depend on the gate potential, however, it also affected by the length of the source to drain regions and drain-source voltage. An ultra-scaled CNTFET has the value of DIBL [15, 28], as shown Eq. (8).

\[
V_T \frac{1}{V_{d=0.1V} - V_T} \frac{1}{V_{d=0.5V}} \quad 0.5 - 0.1
\]

(8)

The computed value of the DIBL for the simulated DG-CNTFET structure is 43.37 mV/V, while 63.19 mV/V is obtained for TG-CNTFET. The lower DIBL has been achieved in the DG-CNTFET makes the structure superior to overshoot SCEs. The Quantum Capacitance \( C_Q \) is related to the channel material. As the density of the state is finite in a semiconductor quantum well, the Fermi level jump above conduction band, which increases quantum well charges. Figure 13 corresponds to the quantum capacitance variation at different thicknesses of DG-CNTFET.

The value of capacitance reduces with the increasing gate oxide thickness, though it affects only after the threshold. The effect of gate oxide thickness on the \( C_Q-V_g \) for TG-CNTFET is demonstrated in Fig. 14. The Fermi level requires energy to drive, which depends on quantum capacitance, \( C_Q \) causes the Fermi level diffusion in the conduction band. Hence, it is noteworthy in Fig. 14 that the increasing thickness causes the capacitance to reduce above the gate voltage 1 V.

![Fig. 13. C-Vg characteristics of DG-CNTFET at different tox.](image1)

![Fig. 14. C-Vg characteristics of TG-CNTFET at different tox.](image2)

5. Conclusions

In this paper, the electrical behaviour and impact of the short-channel effects in single-wall carbon nanotube have been analysed. The authors have designed and simulated Double-Gate (DG) and Tri-Gate (TG) structures of CNTFET. First, we have considered the effects of carbon nanotube diameter (dCNT - 2 nm-4 nm) and the gate contact length variations \( L_g \sim 5 \text{ nm}-25 \text{ nm} \) in a double-gate structure.

After that, electrical characteristics in terms of Field-effect mobility \( (\mu_{FE}) \), Conductance (G), Subthreshold-Swing (SS), Drain Induced barrier lowering (DIBL), and ON-OFF current ratio \( (I_{ON}/I_{OFF}) \) of DG-CNTFET and TG-CNTFET are compared. In addition, the Quantum capacitance \( C_Q \) versus \( V_g \) at various thickness values \( L_{ox} \sim 0.5 \text{ nm}, 0.8 \text{ nm}, 1.2 \text{ nm}, \) and 2 nm have been obtained for DG-CNTFET and TG-CNTFET. The analysis of results shows that an increase in

$d_{CNT}$ increases the on current ($I_{ON}$) and Field-effect mobility ($\mu_{FE} \sim 1.4 \times 10^3$ cm$^2$/V-s). In the simulation results, high mobility from DG-CNTFET has been achieved.

The work further considered the comparison of gate voltage versus channel capacitance at different oxide thickness in both the device structures. DG-CNTFET can achieve a large $I_{ON}/I_{OFF}$ ratio. The results also demonstrate that the double-gate structure offers better $SS$ oscillation and low DIBL (43.37 mV/V) at increasing channel length and CNT diameter. These results provide detail insights of CNTFET performance and serve as a guide through future CNTFET device design and fabrication. In conclusion, DG-CNTFET offers better performance than TG-CNTFET. It is a better device configuration for low power and higher drain current applications. Beyond the superiority in SCEs mitigation, of CNTFETs performance in circuit applications would be analysed in the future work.

### Nomenclatures

- $d_{CNT}$: Carbon nanotube diameter, m
- $G$: Transconductance, S
- $h$: Planck’s constant, J.s
- $I_{ON}/I_{OFF}$: Current ON-OFF ratio
- $L_D$: Drain to channel interface length, nm
- $L_g$: Gate contact length, nm
- $L_S$: Source to channel interface length, nm
- $n,m$: Chirality vector
- $T$: Transmission coefficient
- $t_{ox}$: Gate oxide thickness, nm
- $V_T$: Threshold voltage

### Greek Symbols

- $\epsilon_{FS,FD}$: Fermi energy in Source and Drain, eV
- $\mu_{FE}$: Field-effect mobility, cm$^2$/V-s
- $\Sigma_S, \Sigma_D$: Source, drain self-energy matrix

### Abbreviations

- CNT: Carbon Nano Tube
- DG: Double Gate
- DIBL: Drain Induced Barrier Lowering
- NEGF: Non-Equilibrium Green’s Function
- SS: Subthreshold Swing
- TG: Triple Gate
- WKB: Wentzel Kramers Brillouin approximation

### References


