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SIMULATION AND PERFORMANCE EVALUATION OF NON-ORTHOGONAL IDMA SYSTEM FOR FUTURE WIRELESS NETWORKS

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Abstract

Multiple access techniques nowadays are considered a hot topic for research for the Fifth-Generation (5G) systems. However, with orthogonal multiple access, it is not possible to achieve the sum capacity of multi-user communications. Non-Orthogonal Multiple Access (NOMA) is imagined to be a serious solution for 5G wireless networks. Recently, a new non-orthogonal multiple access technology has been suggested, which is called Interleave Division Multiple Access (IDMA), where the number of users are greater than the spreading length and user load could be greater than one. IDMA is a promising method to improve spectral efficiency and has attracted much interest from both industrial and academic fields in recent years. In this paper, the performance of the IDMA system is studied by constructing different theory-based exact simulators. The effect of different system parameters such as modulation schemes and channel coding/spreading conditions are considered, where flat fading channels are assumed. The contribution of this paper lies on designing low-cost Chip-by-Chip (CBC) iterative receivers; that is the Chip-by-Chip Successive Interference Canceller (CBCSIC), and the CHIP by Chip Parallel Interference Canceller (CBCPIC) to achieve high system throughput. The system design has been achieved using SIMULINK. The simulation results show that the IDMA scheme is advantageous in terms of both spectral efficiency and bit error rate performance; a high throughput up to 6 bits/chip has been achieved, which make IDMA a promising candidate for 5G wireless networks. In addition, the numerical results show that the CBCSIC receiver manifests better performance compared with the CBCPIC receiver.

Keywords: IDMA; Multiple access interference; Iterative receiver; NOMA.

1. Introduction

For many years, the Code Division Multiple Access (CDMA) technique and due to its own capabilities to cope with asynchronous nature of multimedia data traffic, it had been nominated to support multimedia services in mobile radio communications. Compared with conventional access techniques such as Time Division Multiple Access (TDMA) and frequency division multiple access (FDMA); CDMA is used to provide higher capacity, and to combat the hostile channel frequency selectivity. However, despite its widespread prevalence and its efficiency, CDMA performance is mainly restricted by multiple access interference (MAI) and inter-symbol interference (ISI) problems [1].

Moher [2] mentioned that it is well known that the interleaving process is usually used in CDMA to overcome the problem of burst errors; however, the idea of utilizing such an interleaving process to separate users in CDMA systems have been first suggested. Bruck et al. [3] and Tarable et al. [4], revealed that by assigning different interleaving patterns to different users in a CDMA system, a significant performance improvement can be achieved. Mahadevappa et al. [5] and Frenger et al. [6] have suggested the philosophy of chip-level interleaving for CDMA. Based on such a philosophy, Schoeneich and Hoeher [7], Hoeher and Schoeneich [8] and Ping et al. [9] and Liu et al. [10] have proposed the philosophy of interleave division multiple access, where the term IDMA has been coined by Ping et al. [11] for the first time.

Recently, IDMA is suggested for 5G wireless communication systems, which uses interleaving pattern as users separation. The IDMA is a special case of CDMA. In contrast to the Conventional Multiple Access (CDMA), which uses specific code signature as user separation, the signals of users in the IDMA system are separated by user-specific interleavers for each user [12, 13]. In IDMA, the entire bandwidth is allocated to a single user achieving very high capacity. However, the IDMA requires an iterative process to suppress the MAI problem. The IDMA principle is not limited to multiple access, it can be utilised in many other applications such as coded modulation for high throughput single user transmission, relay and adhoc transmission and Multiple Input Multiple Output (MIMO) systems [9, 14, 15].

In this paper, the performance of the IDMA system is investigated by constructing different theory-based exact simulators. These simulators have been designed to cover different system parameters such as modulation schemes and channel coding/spreading conditions. In addition, two methods of achieving low-cost Chip-by-Chip (CBC) iterative receiver are considered; that is the Chip-by-Chip Successive Interference Canceller (CBCSIC), and the Chip-by-Chip Parallel Interference Canceller (CBCPIC). This paper is organised as follows: after the introduction, Section 2 considers the theory behind the IDMA system where the iterative receiver algorithm is also introduced. In Section 3, we discuss the construction of the IDMA system simulator. The numerical results are discussed in Section 4. Finally, in Section 5, the conclusions are drawn.

2. Structure of IDMA transmitter and receiver

2.1. Mathematical modelling of IDMA transmitter

A general block diagram of the IDMA uplink transmitter is shown in Fig. 1. One can note that the information data $\{d_k(m), m = 1, 2, .., M\}$ is firstly encoded by certain FEC code say {$FEC_k(m)$, m=1, 2, .., M}, where M represents the frame size of the data. The FEC code is generally composed of convolutional code concatenated with repetition code. Then, a user-specific interleaver is used to discriminate among different uplink IDMA users, resulting in a sequence {$y_k(m)$, m=1, 2, …, M} that are usually called "chips" [9, 16, 17]. For this, the name Interleave Division Multiple Access systems has been coined [18, 19]. Thereafter, the sequence $y_k(m)$ is multiplied by the corresponding coefficient (h_k) resulting in the sequence $z_k(m)$. According to Ping et al. [20], it is worth mentioning that h_k represents a coefficient which account for both flat fading channel effects along with the power control. For the sake of simplicity, we assume real values of h_k; however, the results can be easily generalised to complex channels. Then, the sequence $z_k(m)$ is transmitted over flat fading a channel, where it will suffer from the interference of other active users.

By assuming $n(m)$ as samples of a zero-mean AWGN with variance $\sigma^2 = N_0/2$ [21], the received signal can be written as:

$$s(m) = \sum_{k=1}^{K} h_k y_k\,(m) + \ n(m) \ \ m = 1, 2, .., M. \tag{1}$$

It is worth mentioning here that h_k is considered to be known previously by the receiver.

2.2. Mathematical modelling of IDMA receiver

The IDMA receiver consists of the Elementary Signal Estimator (ESE) along with a bank of decoders. The receiving process depends on two constraints, the FEC code constraint and the multiple access constraints as shown in Fig. 1.

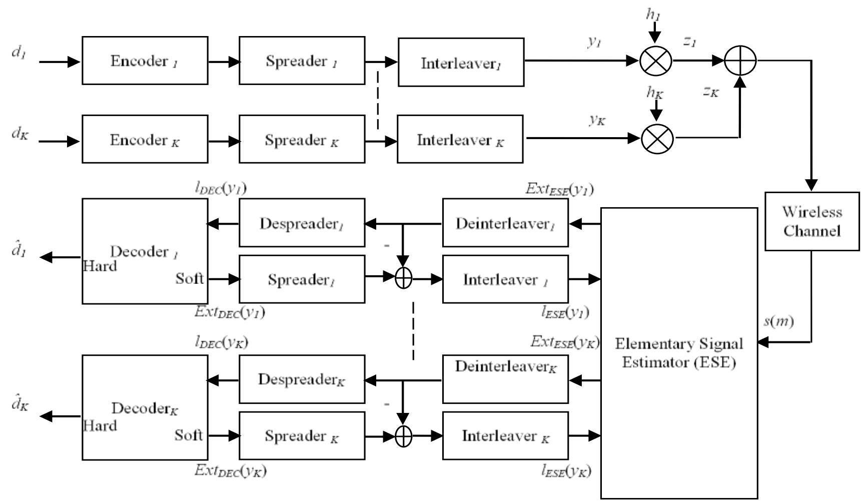

Fig. 1. Block diagram of IDMA system.

The decoders are based on a posteriori probability decoding algorithm (APP) which will not be explained here for the sake of simplicity. However, the receiver operation is achieved by combining the outcomes obtained from the ESE along with the outcomes obtained from the DEC via an iterative process. A related point to consider is that the receiver employs the log-likelihood principle, which gives the Log-Likelihood Ratio (LLR) about certain random variable [9, 17].

According to studies by Ping et al. [9], the ESE receiver has two inputs; $s(m)$ which represents the received signal and a bank of feedback inputs represented by $\tilde{l}(y_k\,(m))$ which expresses the log-likelihood ratios about $y_k(m)$:

$$\tilde{l}_{ESE}(y_k(m)) = log\left(\frac{Pr(y_k(m)=+1)}{Pr(y_k(m)=-1)}\right), \forall k, m \tag{2}$$

where $Pr(y_k(m) = +1)$ is the probability of $y_k(m)$ having the value +1, and $Pr(y_k(m) = -1)$ is the probability of $y_k(m)$ having the value -1. Also, the ESE has a bank of K outputs represented by $Ext_{ESE}(y_k(m))$, as shown in Fig. 1.

Following the outputs of the ESE, one can observe that they are deinterleaved giving $\tilde{l}_{DEC}(y_k(m))$ that are then used as inputs to the corresponding decoders. It is clear that each decoder has two outputs, the hard decision output and the soft decision output. The soft decision output is used to update the ESE receiver with a newer log-likelihood ratio about $y_k(m)$ via a feedback process. The feedback process comprises a reinterleaving operation giving $\tilde{l}_{ESE}(y_k(m))$ as new intrinsic information about $y_k(m)$ to be provided to the ESE input. This operation is repeated several times to assist the receiver endeavours to converge to the target BER.

2.3. Description of ESE receiver

The basic function of the ESE receiver is to give rough estimates about the $y_k(m)$. Ping et al. [9, 17] mentioned that now, under the assumption of BPSK modulation, the log-likelihood ratio about $y_k(m)$ can be given by follows:

$$log\ likelihood\ ratio\ about\ y_k(m) = log\left(\frac{Pr(y_k(m) = +1|s(m), h)}{Pr(y_k(m) = -1|s(m), h)}\right) \tag{3}$$

where the numerator represents the probability of $y_k(m)$ being equal to +1 given the received signal $s(m)$ and h_k as known. The denominator represents the probability of $y_k(m)$ being equal to -1 given $s(m)$ and h_k as known. Ping et al. [17] mentioned, using *Bayes* theorem, Eq. (3) can be rewritten as follows:

$$log\left(\frac{Pr(y_k(m) = +1|s(m), h)}{Pr(y_k(m) = -1|s(m), h)}\right) = log\left(\frac{p(s(m)|y_k(m)=+1,h)}{p(s(m)|y_k(m)=-1,h)}\right) + log\left(\frac{Pr(y_k(m)=+1)}{Pr(y_k(m)=-1)}\right) \tag{4}$$

where the first term represents the extrinsic log-likelihood ratio $Ext_{ESE}(y_k(m))$ about the chip $y_k(m)$ given h_k as the channel observation, while the second term $\tilde{l}_{ESE}(y_k(m))$ supports the ESE with a priori information about the other chips.

By the same way, the decoder obtains a priori information denoted as $\tilde{l}_{DEC}(y_k(m))$ from the ESE output, which supports the decoder a posteriori output about $y_k(m)$ given the code constraint (C). The $Ext_{DEC}(y_k(m))$ is usually called the decoder soft output which, after reinterleaving, is fed back to the ESE as an updated information about $y_k(m)$ denoted as $\tilde{l}_{ESE}(y_k(m))$.

Ping et al. [17] stated that depending on the fed back signal $\tilde{l}_{ESE}\left(y_k(m)\right)$, the ESE receiver make an initial estimation on $y_k(m)$ (i.e., $E\left(y_k(m)\right)$).

$$E\left(y_k(m)\right) = \frac{exp\left(\tilde{l}_{ESE}(y_k(m))\right)-1}{exp\left(\tilde{l}_{ESE}(y_k(m))\right)+1} = tanh\left(\frac{\tilde{l}_{ESE}(y_k(m))}{2}\right) \tag{5}$$

Also, based on studies by Ping et al. [17], the ESE receiver calculates the variance of $y_k(m)$:

$$Var\left(y_k(m)\right) = 1 - \left(E\left(y_k(m)\right)\right)^2 \tag{6}$$

The ESE receiver then exploits the results obtained from equations 5 and 6 to make new extrinsic information about $y_k(m)$ which is denoted as $Ext_{ESE}\left(y_k(m)\right)$.

Ping et al. [17] suggested that now, to find $Ext_{ESE}\left(y_k(m)\right)$, firstly we can rewrite Eq. (1) as follows:

$$s(m) = h_k y_k(m) + \xi_k(m) \tag{7}$$

where $h_k y_k(m)$ is the signal of the desired user, and

$$\xi_k(m) \equiv s(m) - h_k y_k(m) = \sum_{\substack{k'=1 \\ k' \neq k}}^{K} h_{k'} y_{k'} + n(m) \tag{8}$$

The distortion (including both interference and additive noise) contained in $s(m)$ with respect to $y_k(m)$. Now, assuming a large number of active users, the central limit theorem can be applied to $\xi_k(m)$. According to Ping et al. [9], hence, $\xi_k(m)$ can be approximated as a Gaussian variable, and $s(m)$ can be characterized by a conditional Gaussian probability density function as follows:

$$p\left((s(m)|y_k(m) = \pm 1)\right) = \frac{1}{\sqrt{2\pi Var\left(\xi_k(m)\right)}} exp\left(-\frac{\left(s(m)-\left(\pm h_k + E\left(\xi_k(m)\right)\right)\right)^2}{2Var\left(\xi_k(m)\right)}\right) \tag{9}$$

where;

$$E\left(\xi_k(j)\right) = \sum_{\substack{k'=1 \\ k' \neq k}}^{K} h_{k'} E\left(y_{k'}(m)\right) \tag{10}$$

$$Var\left(\xi_k(j)\right) = \sum_{\substack{k'=1 \\ k' \neq k}}^{K} |h_{k'}|^2 Var\left(y_{k'}(m)\right) + \sigma^2 \sum_{\substack{k'=1 \\ k' \neq k}}^{K} h_{k'} E\left(y_{k'}(m)\right) \tag{11}$$

Also, based on studies by Ping et al. [17], $E(\cdot)$ is the mean function and $Var(\cdot)$ is the variance function. Now, by applying the Gaussian approximation to Eq. (7), the $Ext_{ESE}\left(y_k(m)\right)$ can be calculated as follows:

$$Ext_{ESE}\left(y_k(m)\right) = log\frac{exp\left(-\frac{\left(s(m)-E\left(\xi_k(m)\right)-h_k\right)^2}{2Var\left(\xi_k(m)\right)}\right)}{\sqrt{2\pi Var\left(\xi_k(m)\right)}} - log\frac{exp\left(-\frac{\left(s(m)-E\left(\xi_k(m)\right)+h_k\right)^2}{2Var\left(\xi_k(m)\right)}\right)}{\sqrt{2\pi Var\left(\xi_k(m)\right)}} = 2h_k \,.\frac{s(m) - E\left(\xi_k(m)\right)}{Var\left(\xi_k(m)\right)} \tag{12}$$

Therefore, the output of the ESE receiver can be represented by Eq. (12).

To sum up, the operation of the iterative receiver can be represented by a mathematical algorithm. So, in the following section, the iterative receiver algorithm for BPSK mapping with single path channel will be discussed in details.

2.4. Algorithm for BPSK modulation over flat fading channel

ESE operations:

Step 1. Estimation of interference mean and variance

Initialization: $\tilde{l}_{ESE}(y_k(m)) = 0, \forall m, k.$ (13)

$$E(y_k(m)) = tanh(\tilde{l}_{ESE}(y_k(m))/2), \forall k, m. \quad (14)$$

$$Var(y_k(m)) = 1 - \left(E(y_k(m))\right)^2, \forall k, m. \quad (15)$$

$$E(s(m)) = \sum_{k'=1}^{K} h_{k'} E(y_{k'}(m)), \forall m \quad (16)$$

$$Var(s(m)) = \sum_{k'=1}^{K} |h_{k'}|^2 Var(y_{k'}(m)) + \sigma^2, \ \forall m \quad (17)$$

Step 2. Finding the extrinsic LLR

$$Ext_{ESE}(y_k(m)) = 2h_k \cdot \frac{s(m) - E(s(m)) + h_k E(y_k(m))}{Var(s(m)) - |h_k|^2 Var(y_k(m))}, \forall k, m \quad (18)$$

Decoder operations:

The APP decoding in DECs is carried out to create $Ext_{DEC}(y_k(m))$ and update $\tilde{l}_{ESE}(y_k(m))$ then return to Eq. (14) for the next iteration.

The chip-by-chip detection algorithm can be implemented either by a parallel scheme (CBCPIC), discussed above, where the APP decoding and the processes (14)-(16) are performed at the same time for all users. Or by a serial scheme (CBCSIC), where the APP decoding and the processes (14)-(16) are performed user by user. With the CBCSIC (serial detection algorithm), after the user's APP decoding is carried out, the means and variances in (5) are updated partially.

It is worth mentioning that the complexity of the former algorithm is very low and independent of the total number of users (K). This is due to the fact that the normalized computational cost in (14)-(16) (excluding the APP decoding of C) is only several multiplications and additions, and $tanh(x)$ function per chip per user per iteration. A related point to mention is that the iterative receiver algorithms for QPSK will not be discussed here to avoid redundancy.

3. Designing IDMA system simulator

As we mentioned earlier, in this paper we aim at achieving the exact simulator for the promising IDMA wireless communication system. In this section, we discuss the simulator for IDMA system. It is worth to mention that we have used MATLAB program for this purpose. The main blocks of the system have been designed corresponding to that in Fig. 1.

The Simulink model that we have built for the transmitter and the receiver of IDMA system with K simultaneous users is shown in Fig. 2.

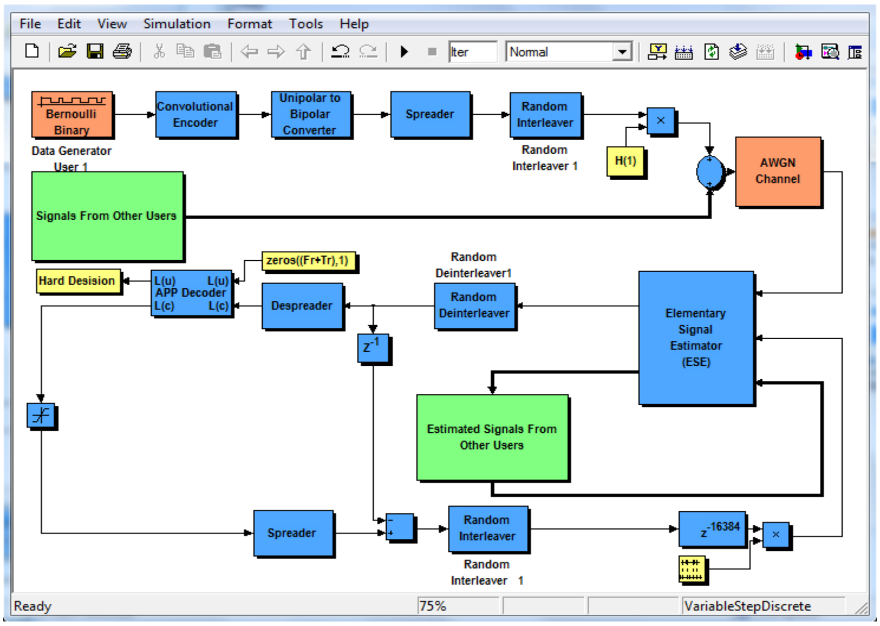

Fig. 2. Simulink block diagram of IDMA system.

The main blocks that we have used are listed below:

For the transmitter side:

- Data generator: The first stage of the simulator is to generate a random data sequence by using the Bernoulli Binary random generator.
- Encoder: Each user data are first encoded with a Forward-Error-Correcting (FEC) code. FEC code consists of convolutional code followed by repetition code. A convolutional encoder of rate 1/2 is used [22].
- Random interleaver: The interleaver is used to permute the input data and rearrange it using random pattern.

Then the symbols are multiplied by h_k, where h_k accounts for the combined effect of both flat fading channel and the power control for the user-k.

For the receiver side:

- Elementary Signal Estimator (ESE): The ESE subsystem is composed of several functional blocks that are working jointly to achieve the ESE algorithm. Figure 3 shows the internal blocks for the ESE subsystem.
- Random deinterleaver: This block is used to restore ordering or rearrange the elements of its input vector using a random permutation. By this process, the original ordering of data sequence can be retrieved.
- Despreader: It is exactly the inverse operation of the spreader on the transmitter side.
- APP Decoder: APP decoder aims at recovering messages that are encoded using a convolutional encoder. It performs a posteriori probability (APP) decoding of a convolutional code.

Respreading and reinterleaving are applied in the feedback loop of the receiver to achieve the iterative process. During the iterative process, ESE and DECs exchange extrinsic information about the input signal. This operation carried out many times until it reaches a predetermined iteration number.

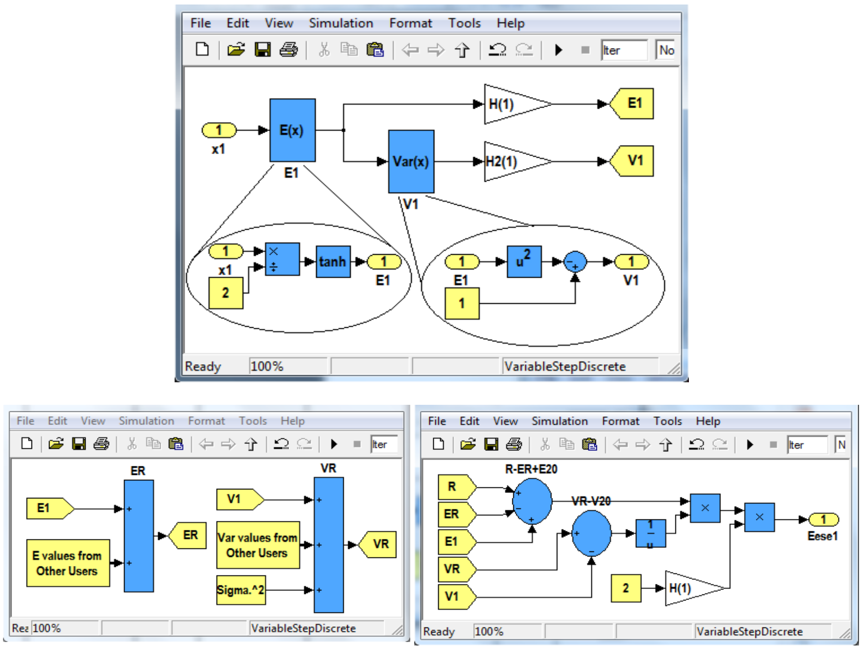

Fig. 3. Elementary signal estimator of the algorithm *I:* (a) Mean and variance calculations of the desired user, (b) Mean and variance calculations of all users and (c) Extrinsic LLR calculation of the desired user.

4. Numerical results

Based on the ESE algorithm, this section presents the simulation results to evaluate the performance of IDMA system. Firstly, let us focus our attention to examine the throughput efficiency of the uncoded IDMA system. The information bits for each user are divided into frames, each frame length equals to 1024 bits. The information bits are encoded by a spreading sequence [+1, -1, +1, -1,… ,-1] with length equal to 16 and permuted by random interleaver to generate the chip-level sequence. The interleaving process is accomplished in a way of keeping the different interleavers random and independent. QPSK mapping is applied. Also, each user has a rate of R=1/16 information bits per symbol.

The overall bandwidth efficiency is one of the important parameters for evaluating the performance of communication systems; it is usually measured by the total system throughput $K\times R$. Table 1 demonstrates the power distribution among users for QPSK mapping, where the flat fading channel effect is already taken into account. This distribution is utilised to achieve minimum total transmitted power [20]. Knowing that the system throughput is represented by $K\times R$, hence, for K = 16, 32 and 48 the corresponding throughputs are 2, 4 and 6 bits/chip. We can see from Table 1 that for throughput = 2 bits/chip, the same power allocation is applied, while for higher system throughput, however, unequal power allocation is necessary for good performance.

Figure 4 demonstrates the desired user signal variations throughout the various stages of the IDMA system at the first iteration, where one can observe that the signal waveforms obey each stage function.

Table 1. Relative power allocation among users for uncoded IDMA system.

	(Number of users) x (power level (h_k^2) in dB)	Throughput (bit/chip)
***K*=16**	16×0.	2
***K*=32**	15 ×0, 1×3.311, 4×3.725, 3×4.139, 1×6.623, 4×7.037, 4×7.451.	4
***K*=48**	15×0, 3×3.311, 3×4.139, 3×4.553, 2×6.623, 2×7.037, 3×7.451,1×9.52, 3× 9.934, 3×10.348, 1×10.762, 4×13.246, 5×13.659.	6

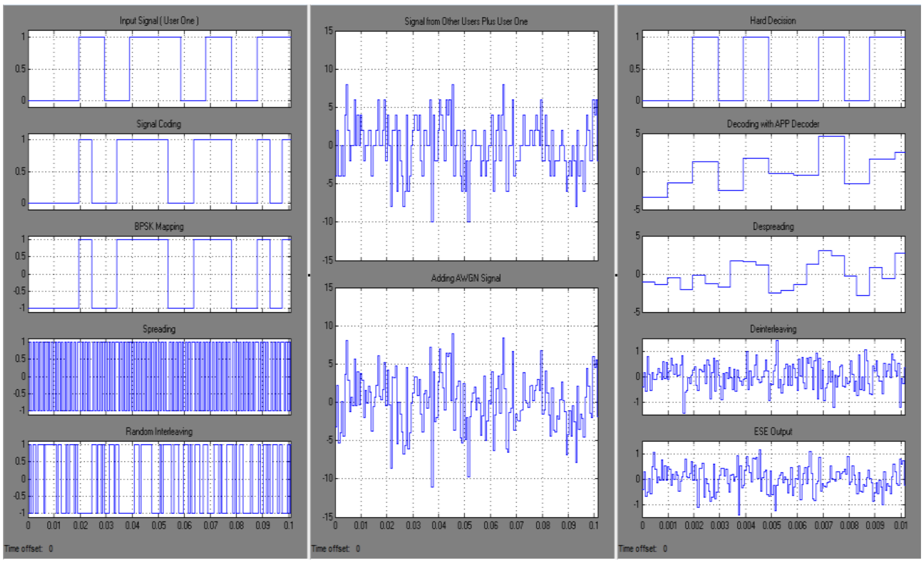

Fig. 4. Signal flow of IDMA system at first iteration.

Henceforth, QPSK mapping is used over flat fading channel; unless otherwise stated. The performance of the uncoded IDMA system is depicted in Fig. 5 for different numbers of active users. The performance of single-user is also plotted for reference. The number of iterations that are used to obtain the results for *K*=32, and for *K* = 48; are 6 and 15, respectively. It is clear that even with such high throughputs, the IDMA system can achieve a Bit Error Rate (BER) of 10^{-4} but at the expense of the increase in E_b/N_o.

The system BER versus the number of iterations for different values of E_b/N_o and for *K* = 48 is illustrated in Fig. 6. It is clear that for a certain number of iterations, increasing E_b/N_o decreases the probability of receiving error bits, especially at a large number of iterations.

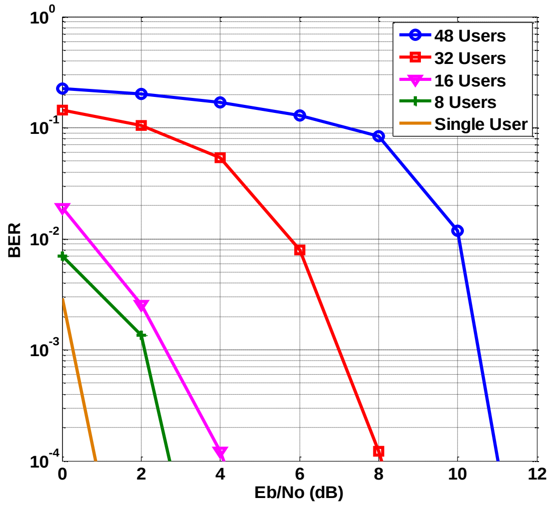

Fig. 5. Performance of uncoded IDMA system for different numbers of users in wireless channel.

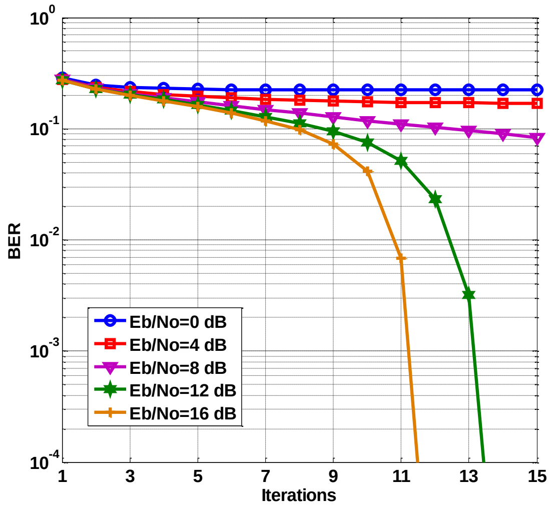

Fig. 6. Performance of IDMA system for different values of E_b/N_o.

Also, Fig. 7 shows the performance of coded IDMA system for different mapping schemes. A rate 1/2 convolutional code with generator polynomials $(5, 3)_8$ is used followed by a rate 1/8 spreading code, iterations number = 4, and the number of users is marked in the figure. From the figure, one can observe that the system performance is improved by using QPSK mapping compared with BPSK mapping [23].

Figure 8 shows the system BER performance with the number of iterations for different spreading code lengths. The number of active users equal to 8 and E_b/N_o equals to 10 dB. As expected, it can be seen that when the spreading length is getting large, the performance is becoming better.

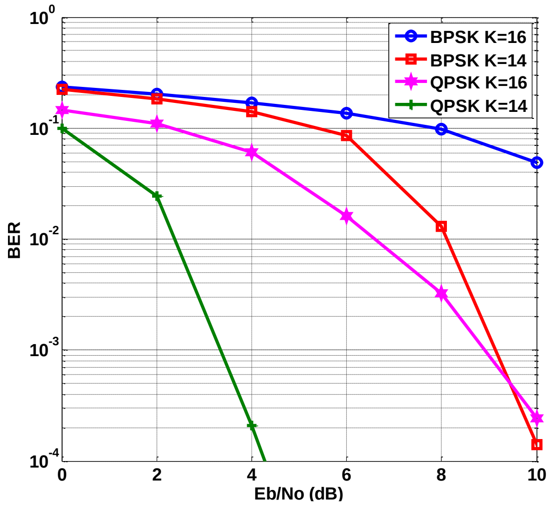

Fig. 7. Performance of coded IDMA system for different mapping schemes

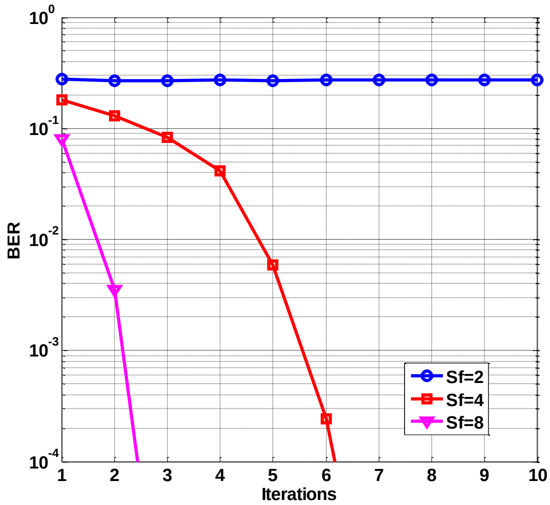

Fig. 8. Performance of IDMA system for different spreading lengths.

In Fig. 9, the coded IDMA manifests better performance than uncoded IDMA, which is consistent with the fact that the efficiency will be improved as code rate *R* goes lower than 1 [16].

From Fig. 10, it can be seen that CBCSIC needs fewer iterations for users detection than the CBCPIC but on the account of delay. Iteration gains can be obtained with CBCSIC even at the sixth iteration, which is enough to achieve a BER lower than 10^{-4} with $K = 16$. However, CBCPIC can also reach this limit but after much more iterations. From the figure, one can observe that the SINR evolves from its minimum value, which is equal to $\frac{P}{(K-1)P+\sigma^2}$ till it reaches its maximum value, where $P = h_k^2$. However, the maximum SINR occurs when all interferences are cancelled out by the iterative receiver, so the maximum SINR is equal to $\frac{P}{\sigma^2}$.

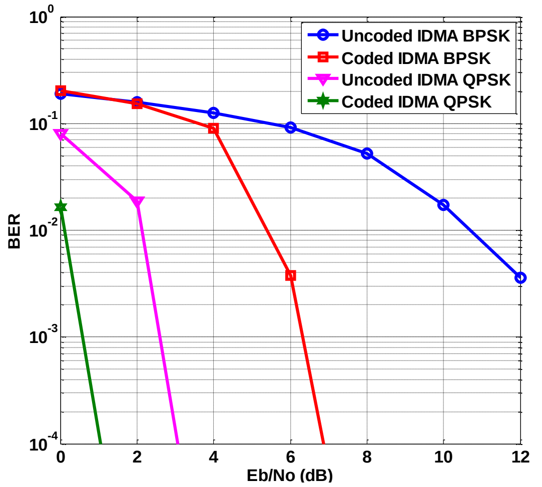

Fig. 9. Performance comparison between coded IDMA and uncoded IDMA systems.

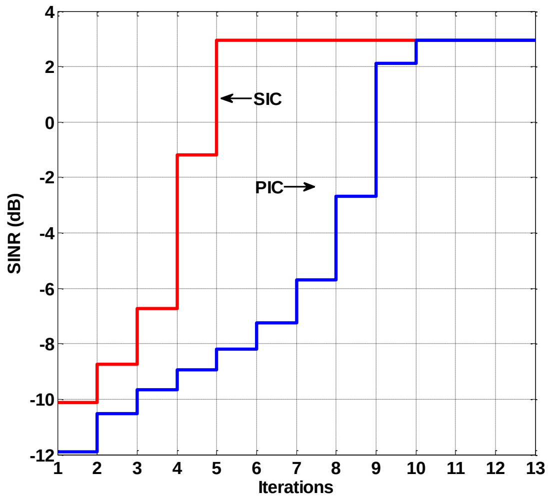

Fig. 10. SINR evolution for parallel and serial iterative receivers.

Visual results

It may be suitable here to give an example of image transmission instead of random data transmission to make the results more vital. So, for the sake of further verification for the IDMA system performance; especially the ability of the designed iterative receiver to discriminate among various active users, each user is allowed to transmit certain image as shown in Fig. 11.

It is visually clear that the images detection is improved by the iteration progress. Furthermore, we can numerically notice the SINR evolution along with the BER reduction, which is shown beneath each corresponding image.

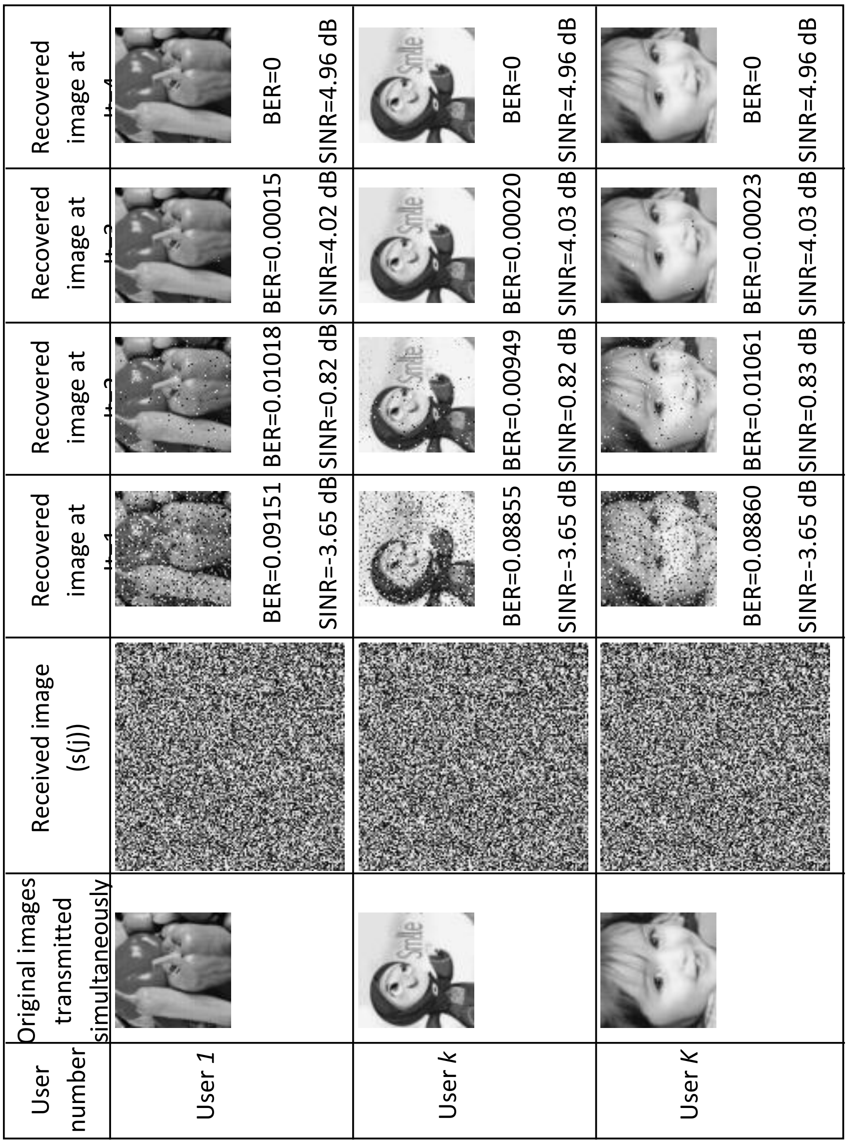

Fig. 11. Performance of IDMA system via visual demonstration.

5. Conclusions

This paper aims at building a simulator for the new multiple access scheme, that is the IDMA. In this concluding section, the main findings of our investigations are summarised. From the simulation results, it can be concluded that the IDMA system can achieve throughput up to 6 bits/chip with BER of 10^{-6}. Furthermore, the simulation results demonstrate that the power distribution among active users has a significant effect on the iterative receiver performance. Consequently, proper power distribution can improve system throughput. Therefore, a study on IDMA power control optimization can be considered for future work. In addition, our work can be extended to account for the effect of selective fading channel by incorporating the Orthogonal Frequency Division Multiplexing (OFDM) scheme resulting in the OFDM–IDMA architecture.

Nomenclatures

d_k	Information data
E	Mean value
E_b/N_o	Normalized Signal to noise ratio value
Ext_{ESE}	Extrinsic information from ESE
Ext_{ESE}	Extrinsic information from DEC
FEC	Encoded data
h_k	Channel coefficient
l_{DEC}	Intrinsic information to DEC
l_{ESE}	Intrinsic information to ESE
K	Number of users
M	Frame size
P	Power of the signal
R	Rate of system
S	Received signal
Var	Variance value
y_k	Transmitted signal

Greek Symbols

ξ	Distortion signal
π	Pi value
σ^2	Variance of AWGN

Abbreviations

5G	Fifth-Generation
APP	A Posteriori Probability
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPSK	Binary Phase Shift Keying
CBC	Chip-By-Chip
CDMA	Code Division Multiple Access
DEC	Decoder
ESE	Elementary Signal Estimator
FDMA	Frequency Division Multiple Access
FEC	Forward Error Correcting
IDMA	Interleave Division Multiple Access
ISI	Inter-Symbol Interference
LLR	Log-Likelihood Ratio
MAI	Multiple Access Interference
NOMA	Non-Orthogonal Multiple Access
PIC	Parallel Interference Canceller
QPSK	Quadrature Phase Shift Keying
SIC	Successive Interference Canceller
SINR	Signal to Noise and Interference Ratio
TDMA	Time Division Multiple Access

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