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HIGH-RESOLUTION TIME TO DIGITAL CONVERTER IN 0.13 μM CMOS PROCESS FOR RFID PHASE LOCKED LOOP

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Abstract

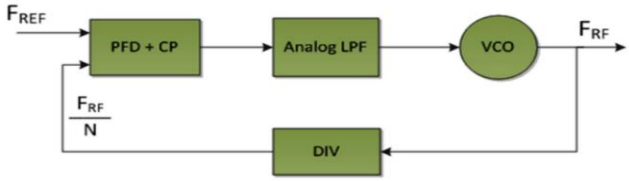
Time to Digital Converter (TDC) has become an attractive replacement of the traditional phase/frequency detector and charge pump with the appearance of digitally intensive All-Digital Phase-Locked-Loop (ADPLL) in deep submicron Complementary Metal-Oxide Semiconductor (CMOS). The performance of Radio Frequency Identification (RFID) ADPLL is limited by the TDC time resolution because it contributes to the in-band phase noise. The available TDC design consumes more power and also difficult to implement in ADPLL because of its complex circuitry. In this article, a simple TDC architecture, based on modified current starved delay element and D flip-flop, has been proposed for RFID ADPLL, which is implemented and tested in TSMC 0.13 μm CMOS process. The proposed TDC circuit achieves 1.31 ps resolution and consumes an average power of 0.061 μW only with 1.8 V power supply. The designed TDC will be suitable to be used in ADPLL frequency synthesizer for RFID applications, high-speed data transmission, automotive solutions etc.

Keywords: All-digital phase-locked loop (ADPLL), CMOS, Delay-line TDC (DL-TDC), TDC.

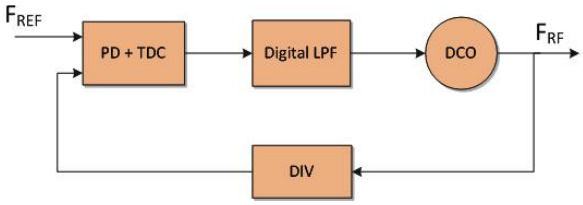
1. Introduction

Since the last decade, the use of RFID has increased extensively in different applications such as a security system, health care and transportation [1, 2]. Nowadays the applications of RFID technology in warehousing have gained a great amount of attention because of its challenging and dynamic environment. The overall performance of the RFID applications greatly depends on the PLL part where TDC contributes significantly [2, 3]. In order to get high performance in RFID applications, the analogue CPPLL is replaced by the ADPLL [3]. Basically, A CPPLL can be visualised as an electronic circuit consisting of a variable frequency oscillator, a phase detector, charge pump, a loop filter and a frequency divider circuit as shown in Fig. 1. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the reference periodic signal and adjusts the oscillator to keep the phases matched through the charge pump and loop filter.

The output frequency, after suitable frequency division by frequency divider, is feedback toward the input of the phase detector, which forms a loop. Consequently, along with synchronizing signals, a phase-locked loop can track an input frequency, or it can create a frequency that is a multiple of the input frequency. On the other hand, in a conventional ADPLL, TDC and digital Phase Detector (PD) replace the PFD and the Charge Pump (CP). Besides, a Digitally Controlled Oscillator (DCO) replaces the conventional VCO and digital low pass filter replace the analogue low-pass filter as shown in Fig. 1. When the locking is aided loop bandwidth of ADPLL can be dynamically reformed. The faster lock time, better phase noise, as well as low signal noise performance, can be achieved at that condition [4]. Moreover, ADPLL can perform direct frequency modulation creating modulated RF. The traditional TDC design required a high cost and suffers from circuit complexity. Therefore, the digital TDC architecture should be design carefully in order to achieve better compared to an analogue PLL. Therefore, it has become challenging for the chip designer to design a highly efficient TDC in order to get high performance of the RFID applications.



(a) Basic block diagram of CPPLL.



(b) Basic block diagram of ADPLL.

Fig. 1. Basic block diagram of CPPLL and ADPLL.

The TDC has been expanded for phase measurement in ADPLLs [5-7]. ADPLL-based clock, data recovery, and frequency synthesiser are being used in many communication applications such as computer, radio, television, cellular phones, and RFID applications [8-10]. TDC is considered as one of the key functional blocks in ADPLL [10]. The quality of the carrier signal in ADPLL is limited by the linearity, conversion range and resolution of the TDC [11-13].

There are several design schemes of CMOS TDC. Delay-line based TDC is the simplest, fully digital, low power and compact structure of TDC compare to other architectures [14]. However, time resolution provided by the inverter or the buffer time delay is inadequate by the CMOS technology. Vernier delay line and 2D vernier ring structure can measure interval up to sub-gate delay resolution [15, 16]. This structure consists of two long delay lines, which lead to a random mismatch of the buffer delay, raise area occupancy, and power consumption. The Gated-Ring-Oscillators (GRO) structure can improve the linearity performance of reducing the quantization noise and produce a wide range of TDC with small area occupancy. But it consumes high power because its resolution is proportionally related to the GRO frequency [17]. The combination of Vernier and GRO TDC can improve time resolution, conversion rate, and power consumption [18]. The GRO internal state could fluctuate during the off-state due to leakages, which create high noise. Implementing 2-step Time Amplifier (TA), high-resolution TDC with lower power consumption and area occupancy can be obtained [19]. The Cyclic and Pulse Train TA TDC achieves high resolution, fast conversion rate and high linearity [20, 21] but suffer from high circuit complexity. It can provide higher gain, which is robust to PVT because it does not depend on cross-coupled logic. But these structures still suffer from an insufficient input linear range and inaccurate gain due to its cross-coupled structure. Pipeline TDC also achieves reasonable resolution, good linearity and high conversion rate [22] but this scheme is complex and difficult to be developed.

Even though there are various types of CMOS TDC architectures available, designers tend to use the simplest and easily integrable TDC schemes [23, 24]. Delay-line based TDC and inverter delay-line based TDC schemes are preferred because of their simple circuit architecture and high resolution. TDC resolution is defined as the minimum unit of the time measurement. It is dependent on the circuit characteristics and noise performance. The time resolution is the significant parameter that contributes to the in-band phase noise of ADPLL [25]. The TDC requires a fast delay to get low in-band phase noise. Therefore, the main challenge faced by the designers is to design a high-resolution TDC with simple TDC architecture. To address these issues, a simple TDC based on delay-line scheme implemented in TSMC 0.13 μm CMOS process is proposed in this article.

2. Methodology

The block diagram of the conventional delay line TDC (DL-TDC) is depicted in Fig 2. It describes that the delay signals are produced by the start signal ripples along a delay chain. The outputs of the delay elements are linked to either latches or flip-flops and sample the state of the delay-line on the rising edge of the stop signal. All delay stages need to be passed by the start signal. Among them successfully passed delay stage provides high value and failed to pass delay stage provides low values in the output of the sampling element. The time resolution of DL-TDC depends on the delay element in the chain [14].

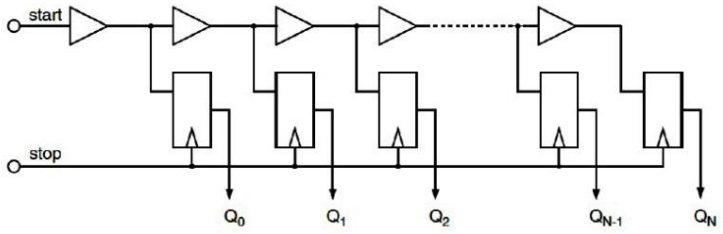


Fig. 2. Conventional delay-line TDC [21].

2.1. *D* flip-flop

In order to store information, flip-flops and latches are used as the basic memory where *D* flip-flops are used to sample the state of the delay line. The flip-flop provides better timing control in tricky timings in view that signal on the input pin is captured at the moment when the flip-flop is clocked and consequent changes in the information are disregarded until the next clock event. The D flip-flop can be interpreted as a delay-line or zero order preserve. The *D* flip-flop is designed with the aid of the NAND gate and inverter.

Figure 3 shows the 2-input NAND gate implemented in the D flip-flop circuit. This gate is made in CMOS process by utilizing an NMOS Pull-Down Network (PDN) at the bottom of a PMOS pull-up network (PUN). With the PUN charging capacitances, the gate act as an inverter while the discharging is performed by the PDN system. From VDD to the output a current path is created, causing Q heads to VDD when I or D is turned off. When both A and B are high, there will be another current path towards the ground, permitting Q discharging to zero.

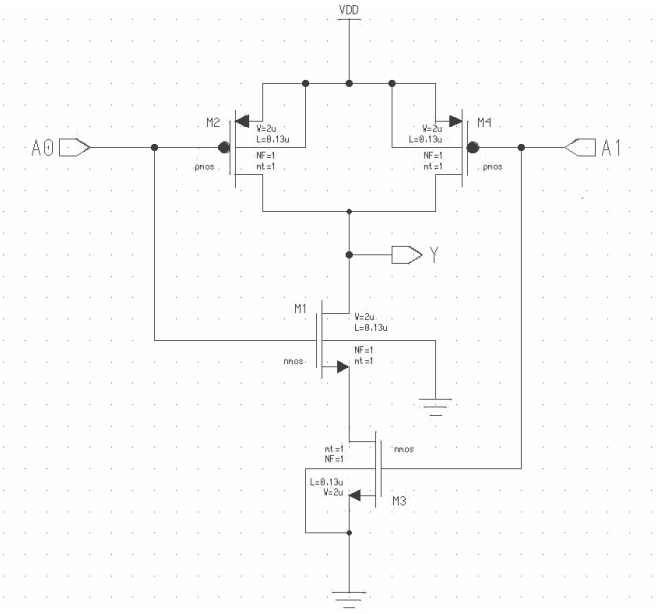


Fig. 3. Two input NAND gate schematic.

2.2. Current starved delay element

There are a few techniques to execute delay elements. Among them, the variable transistor process, shunt capacitor manner and current starved technique are considered the most popular methods for coming up with variable delay cells. In this TDC design, current starved delay element has been chosen because of its simple circuit architecture and a vast range of delay regulations. The designed current starved delay element is presented in Fig. 4.

The current starved delay element composes of two basic inverters between the output and input. The inverters are consisting of M2, M3, M4 and M5. For the first inverter, the charging and discharging currents are controlled by the bias voltage of the transistors M1 and M3 and the delay in the delay element can be adjusted by charging and discharging currents.

The advantage of this delay element is that rising and falling edge of the input signal can be controlled. With the aid of increasing/diminishing the operative on-resistance of M1 and M3, the circuit delay can be extended/diminished.

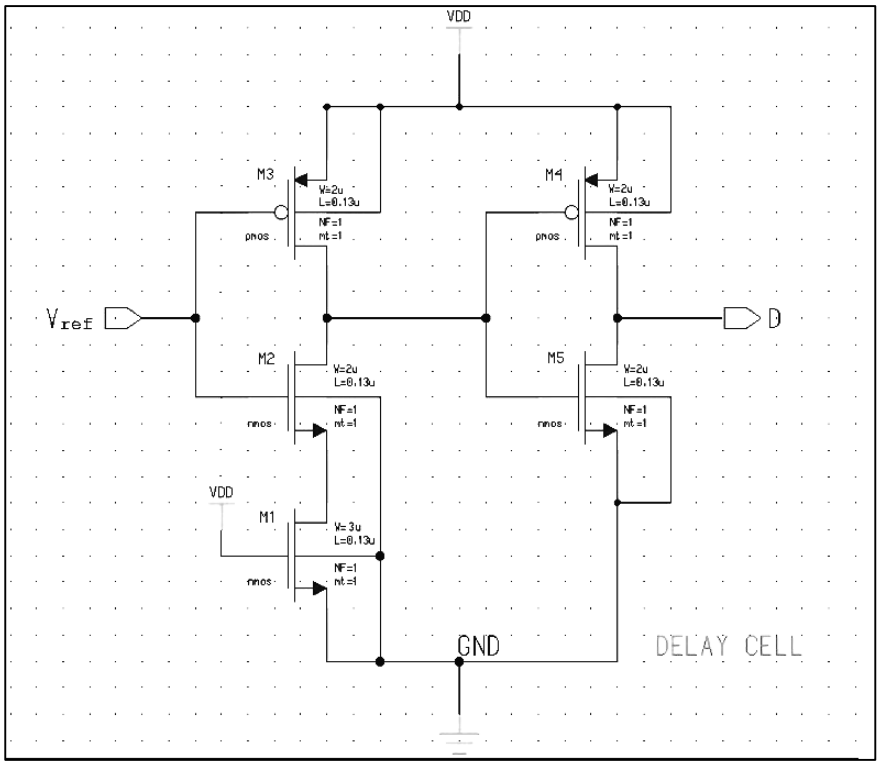


Fig. 4. Designed current starved delay circuit.

2.3. Proposed TDC

Currently, the attention of researchers is not only in the area and delay performance, but also focused on the power dissipation [20]. The low power dissipation has been taken into consideration during the TDC design. Figure 5 describes the proposed

delay-line TDC, which is consists of current starved delay elements and D flip-flop. It integrates 6D-flip-flops and 6 delay elements for 6b output.

The delay time for the designed circuit can be controlled by adjusting the width of the transistor. The relationship between the time delay and the width or transistor are optimised in the proposed circuit because the time resolution of DL-TDC depends on the delay time for the delay circuit. The delay circuit should be as fast as it can be in order to produce the highest resolution TDC.

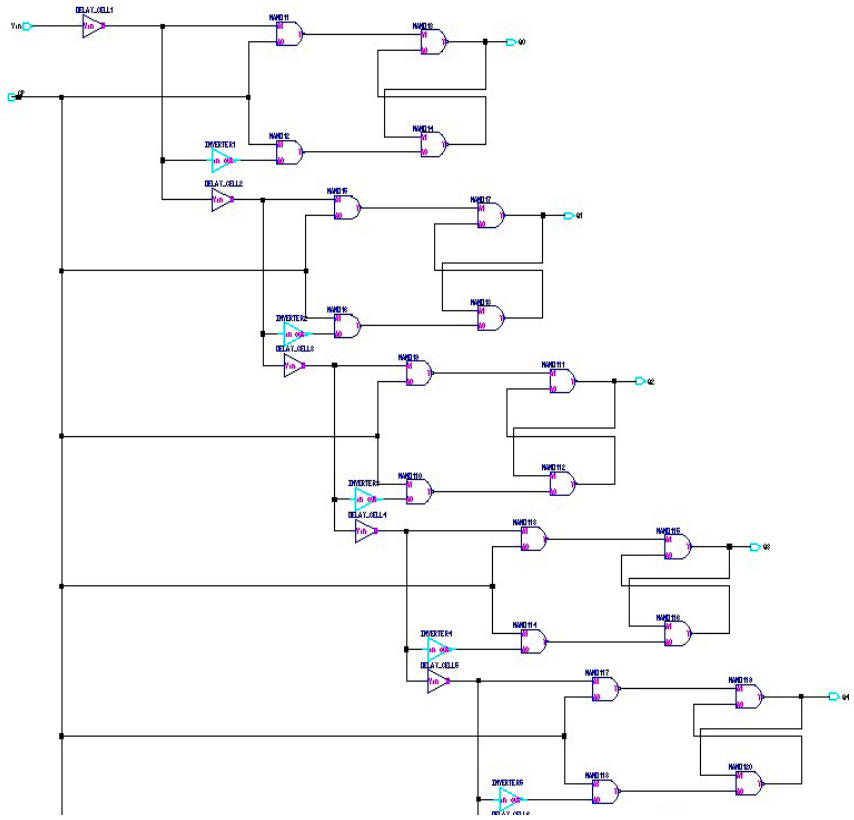


Fig. 5. Proposed TDC architecture (gate level).

Because of the thermal impacts, the TDC error contains a number of parameters: quantisation, linearity, and randomness. In the ADPLL-based frequency synthesiser, the quality of the carrier signal such as the spurious power level, the phase noise, and the output jitter determines the performance of the synthesiser. The noise level at the lower frequencies is defined by the TDC quantisation noise. By Eq. (1) the quantization noise can be measured where Δt res refers to TDC resolution [25], TDCO stands for the time of digitally controlled oscillator (DCO) frequency and the f_{ref} is the reference frequency. The output frequency and the reference frequency remain steady within the time domain, which causes noise.

$$L = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{res}}{T_{DCO}}\right)\frac{1}{f_{ref}} \tag{1}$$

The proposed TDC is designed in TSMC 0.13 μm CMOS process and simulated by EDA tools in the Mentor Graphics environment.

3. Results and Discussion

3.1. Current starved delay element

The time resolution of delay-line TDC is determined by the delay of one delay element and the width of transistor M1 plays a great role to achieve the smallest delay time. The simulation was done by varying the width of transistor M1 value from 0.6 μm to 3 μm keeping the other parameters unchanged. Figure 6 shows the significant impact of the delay time with respect to the variable width of transistor M1. It shows that by increasing the width of transistor M1, the delay will be lower and vice versa. It is because of the fact that larger M1 allows faster charging and discharging current, which responsible for less delay.

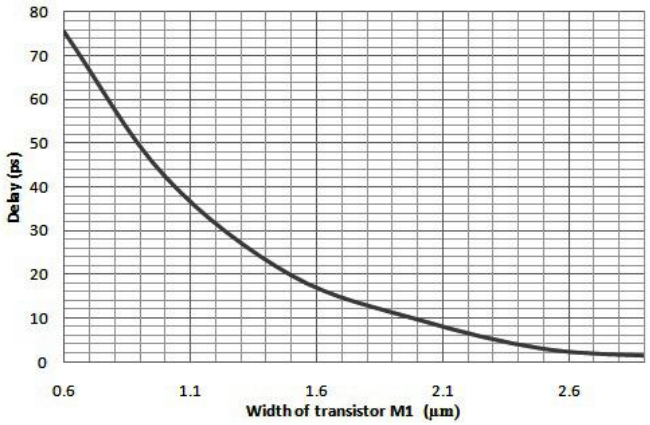


Fig. 6. Delay time versus width of transistor M1.

3.2. Simulation results of TDC

The charging and discharging currents of transistors M2 and M3 are controlled by transistor M1 in the current starved delay circuit. By increasing the effective resistance of controlling transistor M1, the circuit delay can be decreased. When the delay time is decreased, the unit time measurement for TDC also reduces. The M1 transistor is then set to 3 μm since it can provide better resolution to the proposed TDC. Figure 7 shows the simulation waveforms of the proposed TDC. It shows the voltage and current waveforms and respective delays for the desired nodes. This is explained with the help of Fig. 8, which presents the time resolution of the proposed TDC.

From Fig. 8, it can see that the designed TDC achieves 1.31 ps time delay implementing the proposed current starved delay circuit. Moreover, with 26 MHz reference frequency and 2 GHz DCO frequency, the proposed TDC achieved -120.678 dBc/Hz in-band noise. Figure 9 shows the layout of the proposed TDC. The layout is designed using the 3 μm width of transistor M1 in the proposed current starved delay elements. The layout consists of 3 main blocks, which are the

designed current starved delay element, inverter, and NAND gate. The complete layout of the TDC covers only 0.0015 mm^2 area.

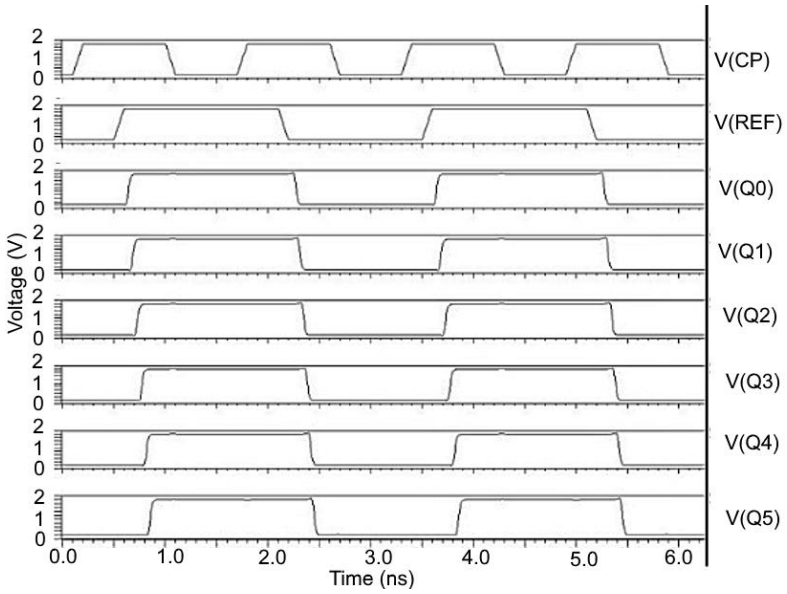


Fig. 7. Output (voltage, current and respective delays for desired nodes) of proposed TDC.

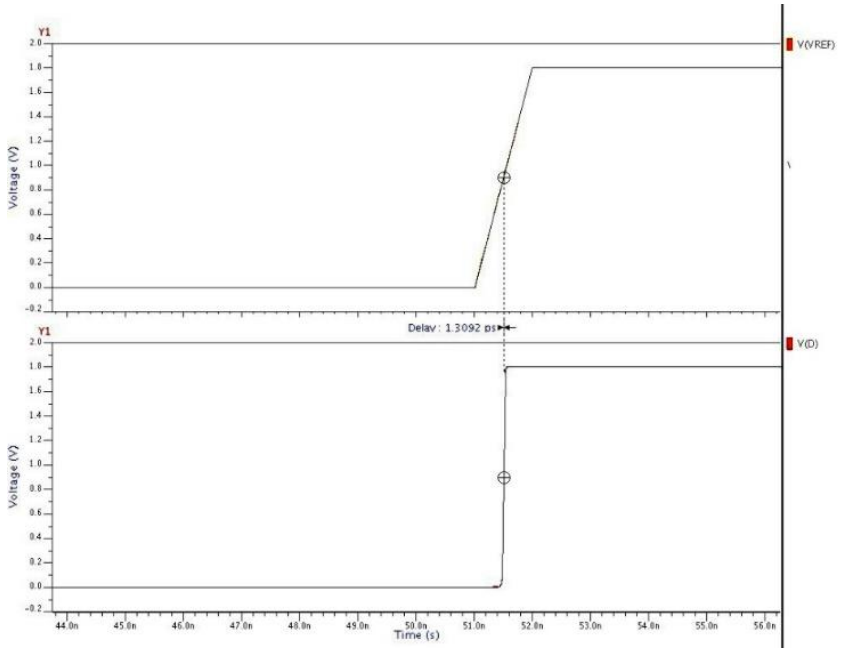


Fig. 8. Time delay of proposed TDC.

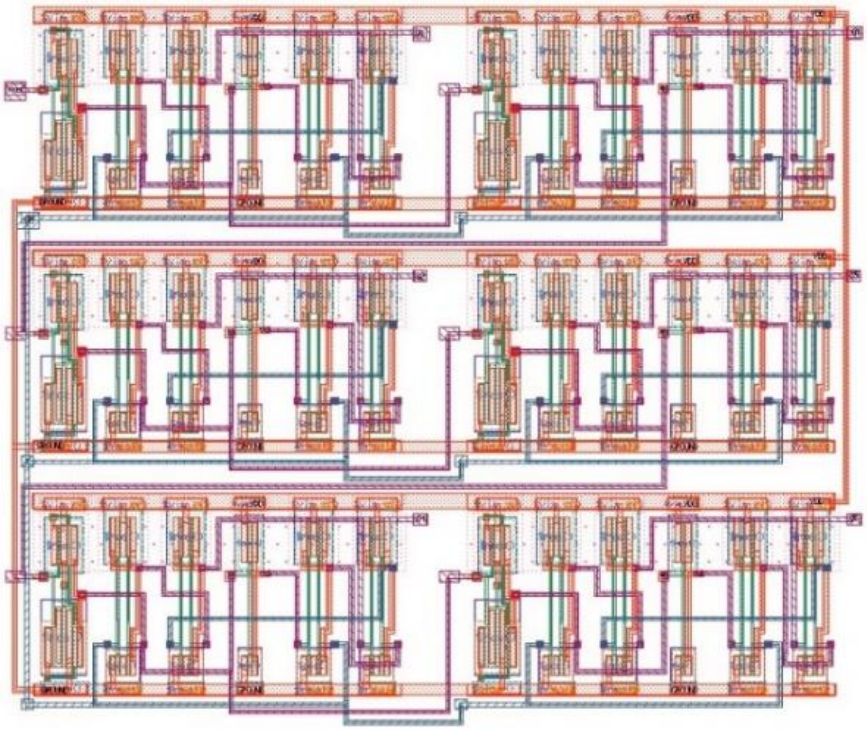


Fig. 9. Time delay of proposed TDC.

3.3. Performance comparison of TDC

The performance comparisons among the proposed TDC circuit and other existing circuits in terms of the design scheme, CMOS process, resolution, power consumption and area are summarised in Table 1.

Table 1 shows the results of different performance parameters of TDC that have been conducted by the different researchers. Table 1 shows that the maximum resolution of 7.3 ps occurs [26]. The channel length modulation effect, the mismatch between PMOS and NMOS causes this high resolution. Andersson et al. [27] suggested architecture also suffers from a high resolution of 5.7 because of the finite output impedance of the current and transistors high cut-off frequency. Dehghani et al. [28] achieved the considerable power consumption and resolution at the same time. As proposed by Lu et al. [29], the recently reported TDC managed to achieve a good resolution of 2.2 ps and less power consumption compared to [18, 21] implementing two 3-stage Gated-Ring-Oscillators (GROs) in the X/Y Vernier branches. Therefore, compared to all, mentioned in Table 1, it can be concluded that the proposed TDC achieves the best resolution of 1.31 ps.

The result indicates that the proposed delay-line TDC resolution depends on the current starved delay element where the fastest delay is achieved. Moreover, the achieved power dissipation of 0.061 mW in this research is much lower compared to others covering die of only 0.0015 mm^2. The reduced chip size is achieved because of less number of transistors used in the current starved delay

circuit that results in low cost. Thus, from this comparison, it is evident that the designed TDC circuit in this research marks a significant improvement in terms of resolution, power dissipation and the chip size of TDC circuits.

Table 1. Performance comparison of proposed TDC design.

Previous research	TDC scheme	CMOS process [nm]	Resolution [ps]	Power dissipation [mW]	Area [mm^2]
Lu et al. [18] 2012	Vernier GRO	90	3.20	3.6	0.0027
Kim et al. [21] 2013	Pulse TA	130	3.75	3.6	0.020
Kim et al. [22] 2013	Pipeline	130	1.76	-	-
Andersson et al. [27] 2014	Delay line and delay latches	65	5.7	1.75	3.96
Dehghani et al. [28] 2015	Vernier delay line	65	4.5	0.098	0.04
Cheng et al. [26] 2016	Vernier ring oscillator	130	7.3	1.2	0.03
Lu et al. [29] 2016	GRO	90	2.2	2.3	0.06
Roy et al. [5] 2017	Ring oscillator	65	6.9	0.16	0.0017
This work	Delay-line	130	1.31	0.061	0.0015

4. Conclusion

A low-power and high-resolution TDC suitable for RFID ADPLL designed and simulated in TSMC 0.13 μm CMOS process is presented in this article. The TDC with the proposed current starved delay element achieves 1.31 ps resolution executing simple delay line based TDC scheme. It consumes the lowest power of 0.00006 mW and compact layout area of 0.0015 mm^2 only. In addition, the proposed design only contributes -120.678 dBc/Hz to the ADPLL in-band phase noise, thus, makes it more suitable for ADPLL frequency synthesiser.

Nomenclatures

fref	Reference frequency

Greek Symbols

Δt	TDC resolution
π	Angle of attack, deg.

Abbreviations

ADPLL	All-digital phase-locked-loop
CMOS	Complementary metal-oxide semiconductor
CP	Charge pump
DCO	Digitally controlled oscillator
DL-TDC	Delay line TDC
GRO	Gated-ring-oscillators
PD	Phase detector
PDN	Pull-down network
PUN	Pull-up network
RFID	Radio frequency identification

TA	Time amplifier
TDC	Time to digital converter
VCO	Voltage controlled oscillator

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