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DESIGN OF CONDITIONAL PULSE ENHANCEMENT FLIP-FLOP EMBEDDED WITH CLOCK GATING AND SIGNAL FEED-THROUGH MECHANISM

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Abstract

In this paper, a new power efficient and high-speed Pulsed-Triggered Flip-Flop (P-FF) in implicit style with clock gating, Conditional Pulse Enhancement and Signal Feed-Through (CGCPESFTFF) is proposed. This new design is presented for the pulsed D-FF in the CMOS 90-nm technology. Three important features are embedded in this flip-flop architecture. Firstly, the enhancement in width and height of triggering pulses during specific conditions gives a solution for the longest discharging path problem in existing P-FFs. Secondly, the clock gating concept reduces unwanted switching activities at sleep/idle mode of operation and thereby reducing dynamic power consumption. Thirdly, a modified signal feed-through mechanism, which directly samples the input to output by using an nMOS pass transistor is introduced. The proposed design achieves better speed and power performance by successfully solving the longest discharging path problem and unwanted switching activities. The post-layout simulation results in Cadence software based on CMOS 90-nm technology shows that the proposed design features less power dissipation, reduced Data-to-*Q* delay and better Power Delay Performance (PDP) when compared with conventional P-FFs. The proposed design is having the advantage of 43.35% in power and 40.74% in speed when compared with conventional P-FFs. The proposed P-FF is implemented in Xilinx FPGA.

Keywords: Clock gating, High-speed, Implicit, Low power, Pulse flip-flop.

1. Introduction

Flip-Flops are the widely used fundamental storage element in all types of digital structures. It is also approximate that above 25% of the total system power is consumed by the clock system [1]. Thus, a major part of the area and power consumption of the total system is contributed by the FFs. In low power and high-speed applications, P-FF exhibits better performance than conventional master-slave FF designs. Kawaguchi and Sakurai [2] mentioned that the single latch structure design of P-FFs made them more popular than conservative master-slave and transmission gate-based FF designs in low power and high-speed applications.

Pulse generator and latches are the two basic parts in the structure of a P-FF design. The trigger pulses are generated by the pulse generator at any edges of clock signals or at both edges of clock signals. The latch structure performs the latching or sampling of the input data into the output based on the generation trigger pulses. Depending upon the triggering pulse generation mechanism, P-FFs are classified as a single and double edge triggered types.

Based on the connection of pulse generation logic and latch, P-FFs are classified as implicit and explicit types [3]. In implicit case, the pulse generator is inbuilt in the latch structure and in explicit it is external to the latch structure. It is estimated that power efficiency is more for implicit P-FFs than explicit types. It is due to the fact that control of discharging the path takes place in implicit P-FF but in the explicit P-FF physical generation of the pulses needed [4]. However, explicit P-FF has an advantage of sharing of pulse generator among neighbouring latches. Both implicit and explicit P-FFs face the longest discharging path problem in a latch structure. According to Elsharkasy et al. [5], this increases the size of the transistors used at the pulse generator to enlarge the width and height of triggering pulses for the sufficient capturing of data.

A lot of wastage in power consumption takes place due to the unnecessary switching activity in a P-FF. Using various technologies such as conditional discharging [6], conditional data mapping [7], conditional capturing [8, 9], error masking [10], power gating [11], and clock gating [12-15], unwanted switching activities can be avoided and thus, the power consumption can be reduced [16].

In this paper, low power and high-speed P-FF is presented,which has an implicit style of operation. This structure solves the unwanted switching activities at sleep/idle mode of operation and the longest discharging path problem in the latch. The remaining part of the paper is organized as follows: Section 2 describes two conventional P-FF designs. It includes Signal Feed-Through FF (SFTFF) and Conditional Pulse Enhancement FF (CPEFF). Section 3 describes the proposed implicit P-FF design. Section 4 compares the P-FFs and presents the results after simulation. The paper concluded in Section 5.

2. Conventional Pulse Flip-Flop Designs

The operations of two P-FFs are discussed in this section. It includes (i) Signal Feed-Through FF (SFTFF), and (ii) Conditional Pulse Enhancement FF (CPEFF).

2.1. Signal feed-through flip-flop

The circuit diagram of explicit pulsed Signal Feed-Through Flip-Flop (SFTFF) is shown in Fig. 1. Explicit pulse generation unit consists of inverters $I1$, $I2$, $I3$, $I4$,

and NAND gate. The true single-phase clock latch structure of this explicit P-FF is embedded with pseudo-nMOS logic and signal feed-through technique [17, 18].

In this P-FF, an *N*-type pass transistor *N*4 driven by clock pulse is used for direct feed-through of input to output. The pass transistor *N*4 provides the path for discharging of the output node *Q* and provides additional driving power to output node *Q* during LOW to HIGH transitions of input data. The requirement of direct driving power from the input to output causes glitches in input data and this result in input skew problems.

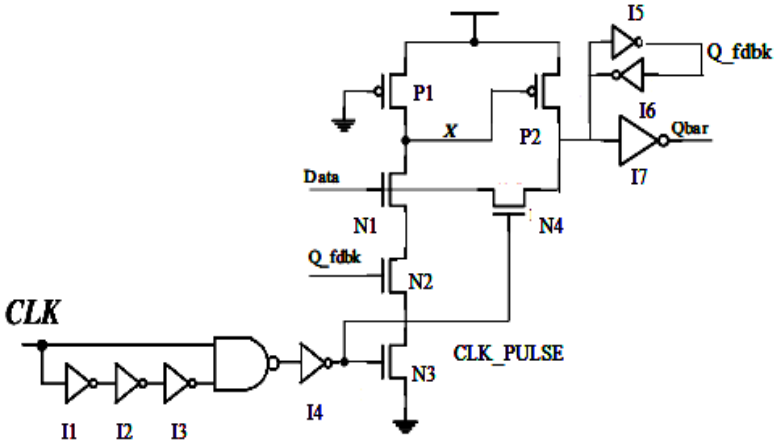

Fig. 1. Circuit diagram of SFTFF.

2.2. Conditional pulse enhancement flip-flop

Based on studies by Hwang et al. [19], the Conditional Pulse Enhancement Flip-Flop (CPEFF) shown in Fig. 2 overcomes the drawbacks of SCCERFF design. In CPEFF, transistors *N*2 and *N*3 form a two-input AND gate of N-type Pass-Transistor Logic (PTL) style. An additional pMOS transistor *P*3 is used for enhancing the width and height of triggering pulses when the input data makes a LOW transition to HIGH.

The speciality of *N*-type PTL is that it transmits only weak ones, that is if VDD is the input then VDD-Vtn is the output. The value of pulse signal is zero at node *Z* in most of the time other than transition edges of clock signals, because of these two complementary inputs of the AND gate. When the clock signal falls to a LOW value then the pulse at node *Z* reaches a temporary floating state. Both transistors *N*2 and *N*3 are turned ON at the rising edges of the clock signal. This passes a weak logic high value (VDD-Vtn) to node *Z*, which causes turning ON of transistor *N*1 by a time period inserted by the delay of inverter *I*1.

In CPEFF, the conditional enhancement in the width and height of triggering signals at node *Z* occurs when the output *Q* of the *FF* is subjected to a transform from LOW to HIGH value. The formation of the longest discharging path occurs when both the data and inverted output Qbar are HIGH. Transistor *P*3 is used to increase the speed of discharge. Turning ON of transistor *P*3 is not possible until the node *X* is discharged to LOW (Vtp) value. An additional boost in the value of

triggering pulse at node *Z* from VDD-Vtn to VDD occurred when pMOS transistor *P*3 turns ON. Subsequent to the rising edge of the clock signal, the delay of inverter *I*1 changes the value of triggering pulse at node *Z* reverse to zero through nMOS transistor *N*3. This will have turned OFF the discharging path. The CPEFF is having better performance in power and speed than those conventional P-FFs schemes with pulse width control issue. In this flip-flop also, unwanted switching activities take place on sleep/idle mode of operation. This will increase the total power consumption and thus degrades the performance.

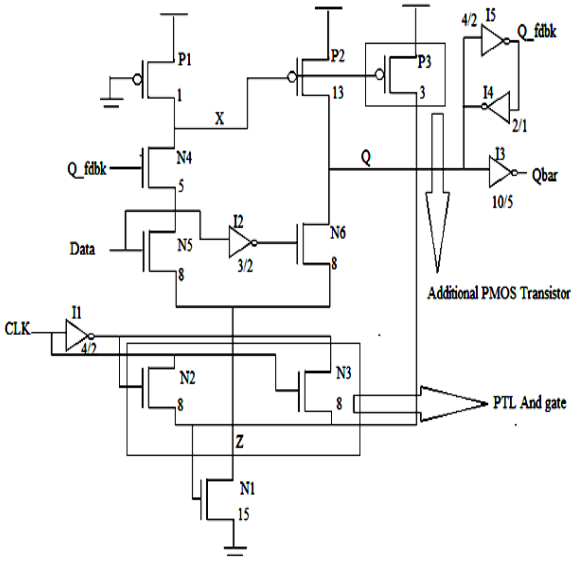

Fig. 2. Circuit diagram of CPEFF.

3. Proposed Pulse Flip-Flop Design

The application of clock gating technique, which aims in the further reduction of clock power in sleep/idle mode of operation is proposed here. The power exerted by the logic gates in connection with the clock and, the power of the remaining part of the flip-flop circuit are the two components of power dissipation inside flip-flops. A flip-flop mainly functions in the active and sleep/idle mode of operation. It is estimated that during the active mode clock must be working and all the switching activities must be at this mode and during sleep/idle mode the clock must be inactive and there will be no switching activities. However, unfortunately, the clock remains active during sleep/idle mode and unwanted switching activities take place, this will increase the power consumption.

Clock gating concept is specially designed for low power applications. This concept solves unwanted switching activities at sleep/idle mode of operation with an additional NOR gate. In this technique, there is a separation in the power exerted by the clock circuit and a remaining circuit. The power consumption of both the clock and the remaining circuit in sleep/idle mode can be reduced by disabling the clock circuit. The proposed clock gating technique can be implemented by disabling the inverter gates present in the pulse generation logic of the conventional

P-FF. This can be achieved by replacing the inverter *I*1 present in CPEFF with a NOR gate as shown in Fig. 3.

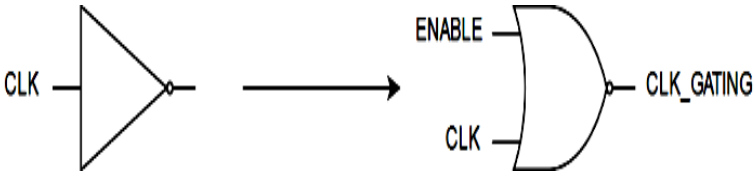

Fig. 3. Clock gating concept.

The circuit diagram of the proposed CGCPESFTFF is shown in Fig. 4. This design is embedded with three important features. The unwanted switching activities in the sleep/idle mode of operations can be overcome by using clock gating concept. The speed of the discharging path can be improved by the conditional enhancement in the width and height of triggering pulses. The speed of latching of input data into the output can be increased by the signal feed-through concept. The embedding of these three features makes the proposed P-FF, more speed and power efficient.

In CGCPESFTFF, the transistors *N*2 and *N*3 form a two-input AND gate of N-type pass-transistor logic style. An additional pMOS transistor *P*3 is used for enhancing the width and height of triggering pulses when the input data makes a LOW transition to HIGH. The nMOS transistor *N*6 controlled by triggering pulse is used for directly sampling the input data to output. The CLK and ENABLE are the two input signals of the NOR gate. In the active mode, NOR gate behaves like an inverter due to its LOW ENABLE input and the flip-flop operate in the normal fashion. All switching activities take place at this mode of operation. In the sleep/idle state, the internal clock is disabled by setting the output of the NOR gate to zero due to its HIGH ENABLE input signal.

The nMOS transistor *N*1 present in the pull-down path is turned off and prevents any data evaluation. This results in saving of clock power by disabling the internal clock. The use of smaller transistors in the NOR gate and also reduced short-circuit power dissipate on the logic gates associated with the clock are the two features of clock gating. Thus, the clock gating circuit does not bring in any power overhead in the total system. The larger stack of transistors in the NOR gate reduces its short circuit power when compared with NOT gate.

In the proposed P-FF, when both input data and inverted output Qbar are HIGH then the internal node *X* must discharge through the three nMOS transistors *N*4, *N*5, and *N*1. This is the longest discharging path. This causes the turning ON of pMOS transistors *P*2 and *P*3. An additional boost in the value of triggering pulse at node *Z* from VDD-Vtn to VDD occurred when pMOS transistor *P*3 turns ON. Thus, an enhancement in the width and height of triggering pulses at node *Z* takes place when the output *Q* of the *FF* is changed from LOW to the HIGH value. The generated pulse is taller, which enhance the discharging strength of transistor *N*1. After the rising edge of the clock signal, the delay of inverter *I*1 drives the value of triggering pulse at node *Z* reverse to zero through nMOS transistor *N*3. This will have turned OFF the discharging path.

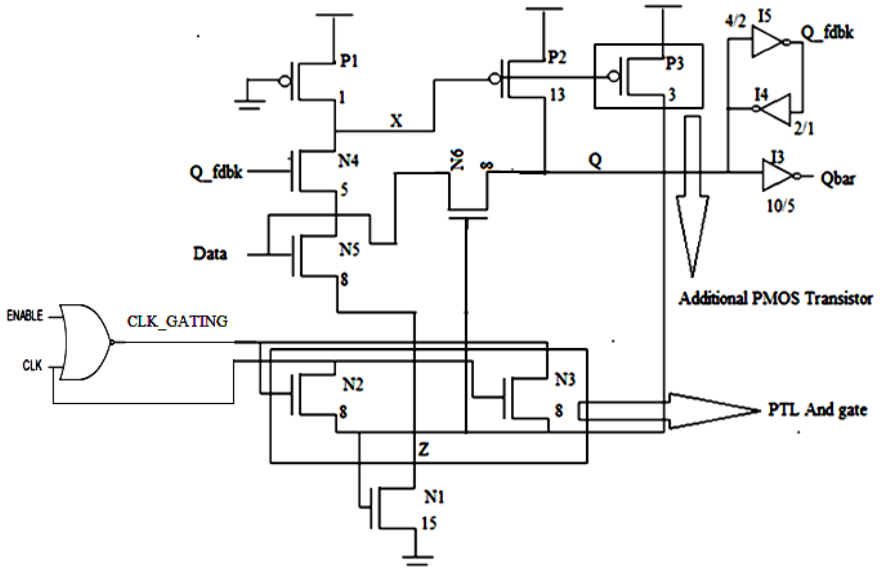

Fig. 4. Circuit diagram of proposed P-FF.

In the proposed design, a weak pull-up gated ground pMOS transistor *P*1 is used in the first stage of true single phase clock latch. This gives to a pseudo-nMOS logic style design and the saving of charge keeper circuit for the internal node X can take place. This will reduce the load capacitance of node *X*.

An nMOS pass transistor *N*6 controlled by trigger pulse generated from pulse generation logic is included so that input data can directly drive the node *Q*. A pMOS transistor *P*2 facilitates auxiliary signal driving from input data to output *Q*. The quick charging of this node shortens the data transition delay from input to output.

The total power consumption is the combination of dynamic, static and short circuit powers and is given in the Eq. (1) [20].

$$P = P_{dynamic} + P_{static} + P_{short-circuit}\,(1) \quad (1)$$

In Eq. (1), $P_{dynamic}$ is the dynamic power consumption, also known as switching power. Dynamic power depends on several factors, including the frequency of operation (f), a square of the supply voltage (V^2), activity factor (α) and Clock Load Capacitance (C_L) [20] as shown in the Eq. (2).

$$i.e., P_{dynamic} = \alpha C_L V^2 f(2) \quad (2)$$

In CGCPESFTFF, the clock is inactive during the sleep/idle mode of operation and this will reduce unwanted switching activities. The reduction of unwanted switching activities leads to dynamic power saving. Thus, the embedding of the clock gating concept, conditional pulse enhancement scheme and signal feed-through mechanism makes the proposed CGCPEFF with better performance in power than conventional P-FFs. The proposed clock-gating concept is not applicable for the flip-flops, which do not use an inverter in the clock path.

4. Experimental Results and Discussions

The proposed and conventional P-FFs are simulated in CMOS 90 nm technology with the power supply of 1.5 V and temperature of 298 K. Cadence software is the simulation tool used to implement the various P-FF designs. The simulation waveform of proposed P-FF is shown in Fig. 5.

The proposed P-FF acts like a single edge triggered *FF* design. The output *Q* is changed according to the data applied at the input during the rising edges of clock signals. In the proposed P-FF, three techniques (Conditional pulse enhancement, clock gating, and signal feed-through) are embedded. Conditional pulse enhancement of the proposed P-FF is shown in Fig. 6. When output *Q* makes a transition from LOW to HIGH value, the width and height of triggering pulses increase from 0.78 nS to 1.2 nS and 800 mV to 1.14 V respectively. From the simulation results, it is clear that the pulse width and height is enhanced upon 35% and 29.82% respectively when compared with normal condition. This happens due to the additional voltage supplied by pMOS transistor *P*3.

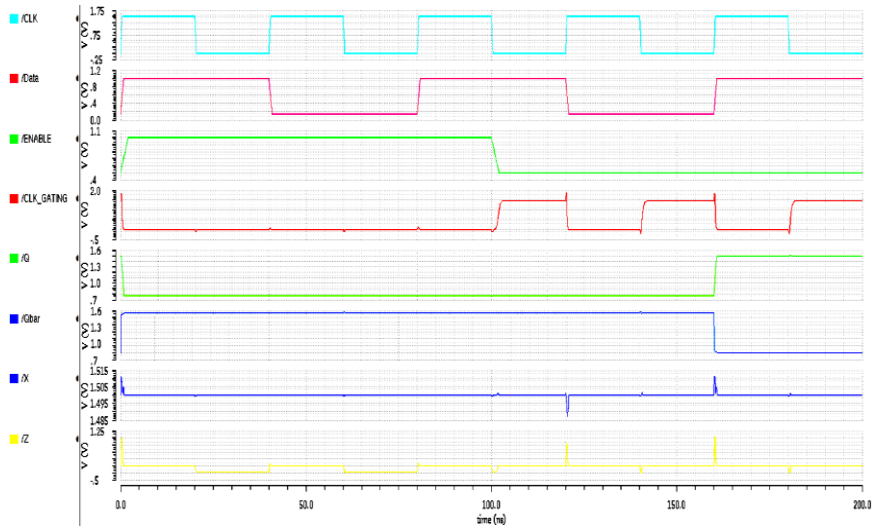

Fig. 5. Simulation waveform of proposed P-FF.

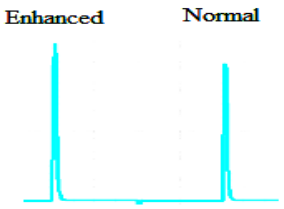

Fig. 6. Conditional pulse enhancement in proposed P-FF.

From the simulation waveform of proposed P-FF, it is clear that the clock gating divides the flip-flop operation into active and sleep/idle mode. When the ENABLE signal is HIGH, no CLK_GATING signal is formed and as a result, there are no transitions at the output node *Q*. At this time flip-flop is in sleep/idle mode and

simulation results gives the average power consumption at this mode is 845.26 nW. During LOW ENABLE, the CLK_GATING signal is formed as the inverted value of the clock signal and input data is sampled to the output *Q* at rising edges of the clock signal. Now the flip-flop is in active mode and average power consumption at this mode is 65.02 μW. The waveform of the clock gating concept is shown in Fig. 7. Due to the embedding of three power reduction techniques, the proposed P-FF reduces the average power consumption to 40.54 μW. The power waveform of proposed P-FF is shown in Fig. 8. Thus, the introduction of the clock-gating concept and signal feed-through mechanism in CPEFF make advantage of 43.35% in power and 40.74% in speed.

The total layout area of the proposed P-FF is 304.71 μm^2 and is shown in Fig. 9. The functional verification of proposed P-FF is done by implementing it in Xilinx FPGA. The implementation of the proposed P-FF in FPGA is shown in Fig. 10.

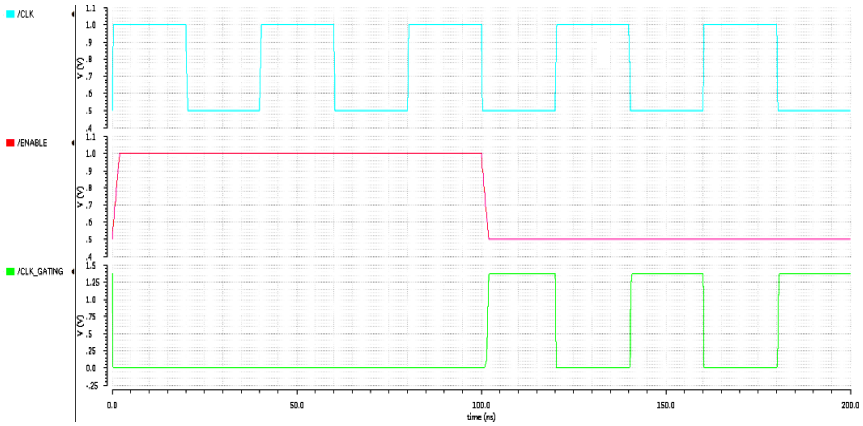

Fig. 7. Waveform of clock gating concept.

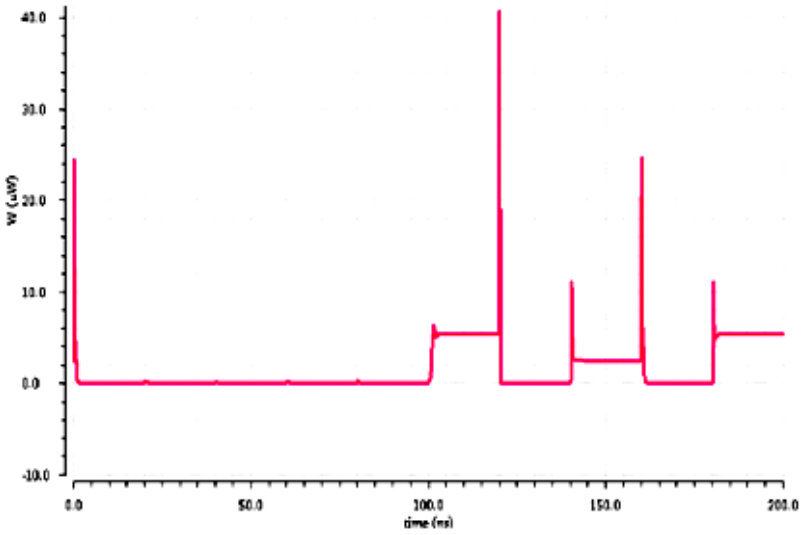

Fig. 8. Power waveform of proposed P-FF.

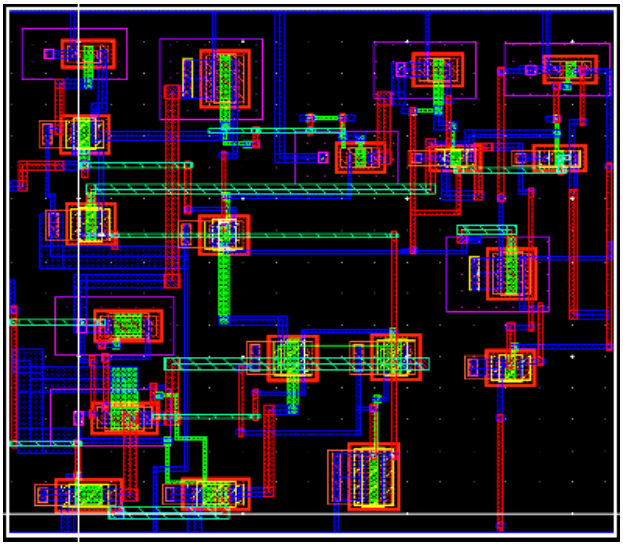

Fig. 9. Layout of proposed P-FF.

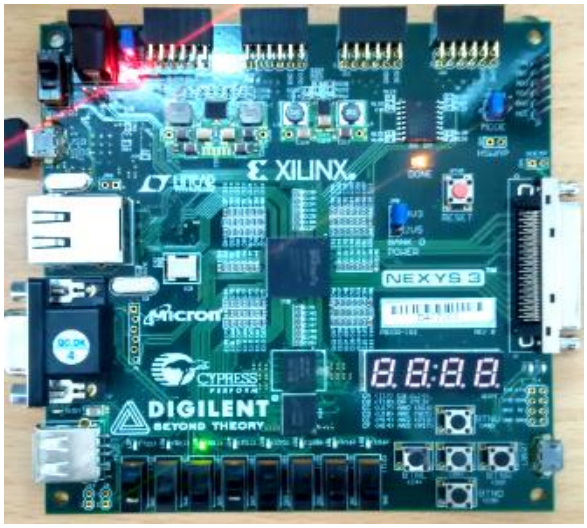

Fig. 10. Implementation of proposed P-FF in Xilinx FPGA.

Comparison with existing pulse flip-flops

To assess the performance of the proposed P-FF, post layout simulation of other designs is done under similar conditions. Table 1 shows the comparison of various performance parameters of proposed FF with other conventional designs. It includes transistor count, average power consumption, minimum Data to Q delay, minimum CLK to *Q* delay, setup time, hold time, power-delay product performance and the layout area. The simulation result shows that due to the embedding of conditional pulse enhancement technique, clock gating concept and signal feed-through mechanism, the proposed P-FF have better performance in power, speed and power-delay product than conservative P-FF.

In the proposed design, the clock is inactive during the sleep/idle mode of operation and this will reduce unwanted switching activities. The reduction in unwanted switching activities leads to dynamic power saving. The direct coupling of input to output and the conditional pulse enhancement scheme increases the speed of latching of data without increasing the delay of inverters and the width of transistors used at the pulse generator.

Figure 11 shows the power comparison of proposed P-FF with SFTFF and CPEFF. The power consumption of the proposed design outperforms the conventional explicit SFTFF by a margin of 62.32%. The proposed design is having the advantage of 43.35% in power consumption when compared with conventional implicit CPEFF. The proposed P-FF is having the advantage of speed in the latching of input data to output *Q* is 40.74% and 34.58% when compared with CPE and SFT flip-flops respectively.

The proposed design is having a negative setup time. Due to negative setup time, the proposed design is having a slightly larger hold time requirement. Figure 12 shows the data-to-*Q* delay comparison of proposed P-FF with SFTFF and CPEFF. The layout area of the proposed CGCPESFTFF is 6.69% smaller than CPEFF. Among the compared P-FFs, proposed P-FF is having the best power-delay product performance due to its reduced power consumption and increased speed of operation.

Table 1. Observation of design parameters.

P-FFs	SFTFF [17]	CPEFF [19]	Proposed
Number of transistors	24	19	19
Power consumption (μW)	107.59	71.57	40.54
Data-to-Q delay (pS)	300	331.24	196.26
CLK-to-Q delay (pS)	129.36	142.83	84.61
Setup time (pS)	-235.6	-122.6	-72.6
Hold-time (pS)	330.2	262.8	155.6
Power-delay product (fJ)	32.27	23.70	7.95
Layout area (μm^2)	398.87	326.59	304.71

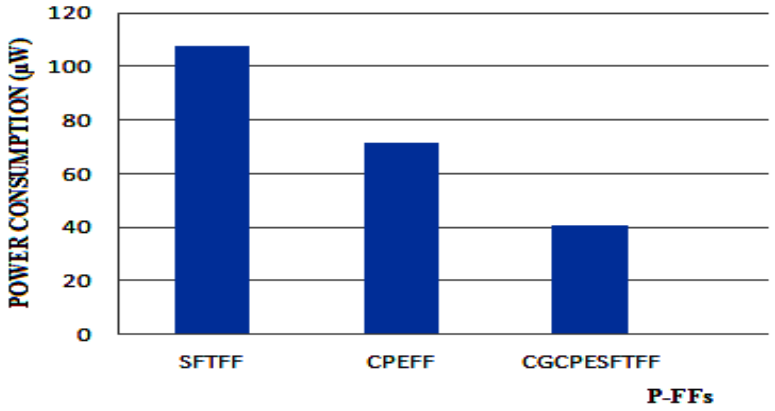

Fig. 11. Comparison of power consumption in P-FFs.

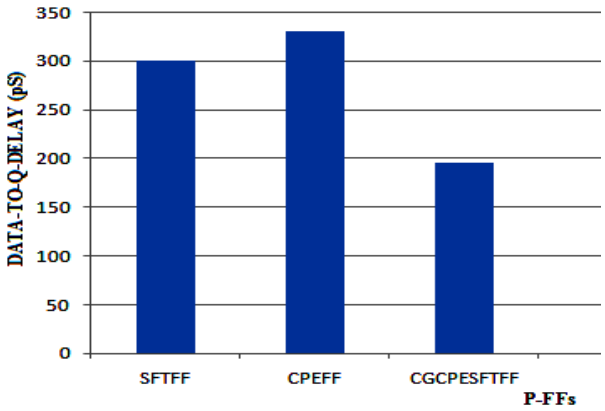

Fig. 12. Comparison of data-to-Q delay in P-FFs.

5. Conclusions

In this paper, a novel low power and high-speed implicit P-FF is presented with three key features. The first feature is the conditional enhancement in the width and height of triggering pulse when output changes from LOW to the HIGH value using an additional pMOS transistor. The second feature is the clock gating concept, which reduces unwanted switching activities at sleep/idle mode, using NOR gate-based clock gating signal generation. The third feature is the direct sampling of input data to output using nMOS pass transistor controlled by trigger pulses. The conditional enhancement in triggering pulse reduces the longest discharging path problem, clock gating concept reduces dynamic power consumption and signal feed-through mechanism increases the speed of operation by direct coupling of input to output. Cadence post-layout simulation results indicate that the proposed P-FF design is having the best performance in power, speed, and Power Delay Product (PDP).

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Nomenclatures

C_L	Clock load capacitance, F
F	Frequency of operation, H
V^2	Square of supply voltage, V

Greek Symbols

α	Activity factor

Abbreviations

CGCPEFF	Clock Gated Conditional Pulse Enhancement Flip-Flop
CPEFF	Conditional Pulse Enhancement Flip-Flop

FF	Flip-Flop
FPGA	Field Programmable Gate Array
P-FF	Pulse Flip-Flop
SFTFF	Signal Feed-Through Flip-Flop

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