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A HYBRID T-TYPE MULTILEVEL INVERTER WITH A NOVEL MODULATION STRATEGY FOR ISOLATED SUPPLY ELECTRIC SYSTEMS

JEBY THOMAS JACOB[1,*], D. KIRUBAKARAN[2]

[1]Sathyabama University, Chennai, India
[2]HoD-EEE Dept. St. Joseph's Institute of Technology, Chennai, India
*Corresponding Author: thomasjebyj@gmail.com

Abstract

Proliferation of multilevel inverters during the last decade focusses mainly on medium and high-power applications. The necessity for low power high efficiency Multilevel Inverters (MLI) were contented by T-Type topologies. This paper proposes a hybrid multilevel inverter topology suitable for isolated supply electric systems. The proposed system is a congregation of T-type and Active Neutral Point Clamped (ANPC) converter modules powered from isolated battery sources. The topology is designed to operate as a boost rectifier also for charging its battery system. A multi input fuzzy controller is employed to optimize the utilization of battery sources powering the system. A distinct Variable Frequency Overlapped Carrier (VFOC) level shifted modulation strategy based on sinusoidal pulse width modulation is developed for efficient switching. VFOC modulation technique aims at reduction in higher order harmonics and minimization of switching losses. Inherent voltage balancing between floating capacitor is another topological peculiarity of the proposed system. Analysis confirms phenomenal reduction in total harmonic distortion compared to its conventional counterparts. Performance and reliability of the proposed MLI is verified for different modulation indices and various kinds of loads. Reliability and effectiveness of the proposed system has been investigated with a simulation model and hardware prototype.

Keywords: ANPC converters, Carrier based modulation technique, Hybrid multilevel inverters, Total harmonic distortion, T-Type inverters.

1. Introduction

Multilevel inverters (MLI) are developed as a result of the fifty-year-old investigations led by researchers to realize a new category [1] of inverter topology with higher nominal power handling capability using existing limited power devices. MLI's present obvious advantage over two level conventional converters such as superior output wave shape quality, lower harmonic distortion and less power loss. Multilevel inverters are basically divided into three main categories viz., Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB).

Complexity of these conventional multilevel inverters increases with the number of levels due to its proportional increment in number of semiconductor devices and driver circuits. This increased number of discrete components affects the reliability of the system also. Each topology possesses its own particular advantages along with some drawbacks. Consequently, a new category [2] of multilevel inverters were introduced named as Hybrid Multilevel Inverter. Hybrid topologies are generally developed to satisfy specific applications by overcoming the shortcomings posed by conventional MLI's. Hybrid topologies are also listed under symmetric and asymmetric structures. Symmetric topologies are based on similar dc voltage sources and have the advantage of modularity [3]. In contrary asymmetric topologies has a more complex design with dissimilar dc sources. But a smaller number of switching devices can be counted as an advantage.

Major types of hybrid topologies introduced in the industry are H-bridge Neutral Point Clamped, Active Neutral Point Clamped (ANPC), Nested Neutral Point Clamped, T- Type Nested Neutral Point Clamped converters. Among the above, the most popular active neutral point converters are developed to generate higher number of voltage levels overcoming unbalanced thermal stresses of power semiconductor devices [4, 5]. ANPC's combine the flexibility of a FC and an NPC. They are also employed in application where minimum THD level are to be maintained. In order to achieve higher voltage levels in ANPC's the number of flying capacitors also has to be increased. The voltage imbalance between dc-link capacitors are the major challenge confronted in any ANPC topology. Higher switching frequency operation of the converter is a mandatory requirement to control the capacitor voltage imbalance [6]. Popular ANPC's design used in the commercial sector are the 3-level and 5-level topology [7-10] as shown in Fig. 1. In this, the clamping switches are replaced with clamping diodes to balance the loss distribution between the switches by creating a path for the neutral current.

This arrangement in other way aids for the inherent capacitor voltage balancing also. All the above-discussed topologies of multilevel inverters are employed in medium or high-power applications. The need for a low power high efficiency multilevel topology was answered by the T- type inverters [11] as shown in Fig. 2.

T type inverters are another class of MLI's discussed in the literature [11], this topology of multilevel inverters own the advantages of low conduction losses and high efficiency

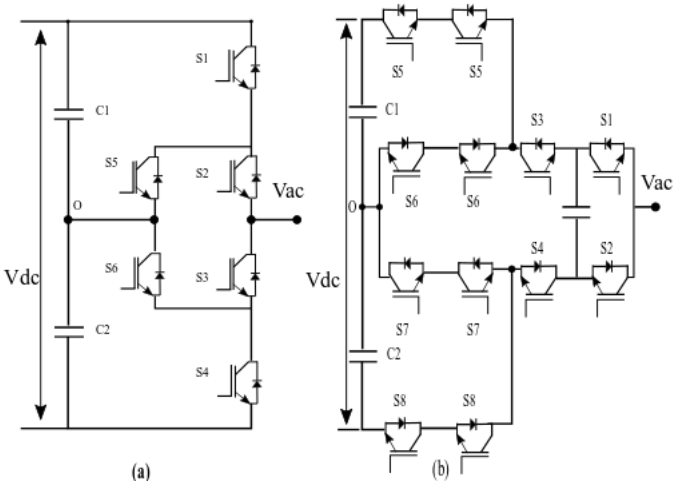


Fig. 1. (a) Three level-ANPC, (b) Five level- ANPC.

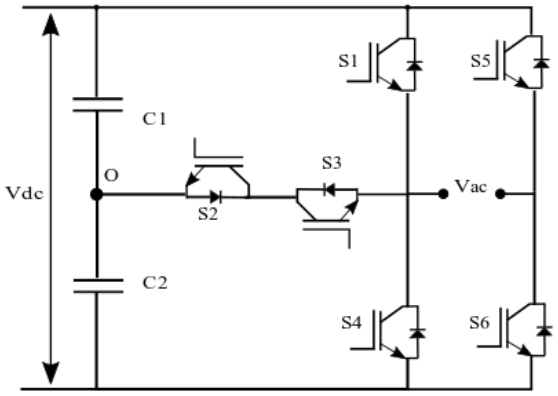


Fig. 2. T-Type three-level MLI.

They are a simple reduced switch topology structure derived from NPC. A T-bridge is basically formed by two conventional and one bidirectional device per phase. The authors claim to have achieved a switch count reduction up to 37.5% compared to conventional topologies with number of voltage levels [11]. Aly et al. [12] discussed a five level T-type multilevel structure with a new PWM method to balance the power losses in power switches. A better lifetime expectancy for power switches are claimed through redundant switching operation of the circuit.

Yu et al. [13] explained that a reduced switch count seven level T- type MLI is reported with multicarrier modulation technique, but the scheme poses serious drawback with high THD in line voltages. Valderrama et al. [14], Xu et al. [15] and Vemuganti et al. [16] reported for another T-type five level asymmetrical converter. The topology is built on an H-bridge configuration, where the bidirectional switches are connected to the central point of the DC-link as shown in Fig. 3.

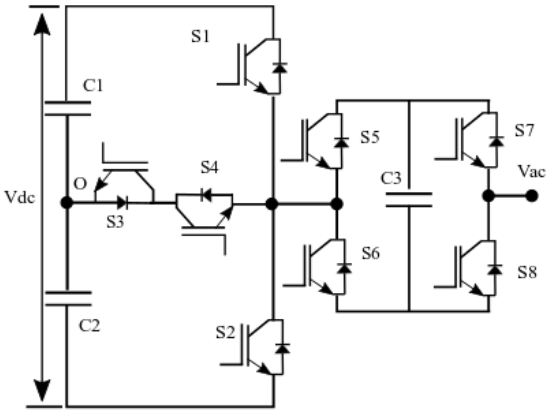


Fig. 3. Seven level-T-type MLI.

The work emphasizes on the reduction of leakage current present in the system according the European standards Analysis of the system shows that Linear modulation index is achieved only up to 0.48. Also, the investigation lacks discussions pertaining to, THD variation with respect to modulation index. He at al. [17] and Narendrababu et al. [18], discussed the T-type five level MLI with level shifted opposite phase disposed carrier modulation technique. The modulation technique utilizes single frequency equal width carriers to generate the switching signals. Major drawback of this topology is the presence of 37% THD in the unfiltered output phase voltage. Samadaei et al. [19] discussed the a square T-type module for asymmetric MLI's as shown in Fig. 4, where ST- type modules with four DC sources are used to achieve the claimed 17 level output voltages at $V_{AB.}$

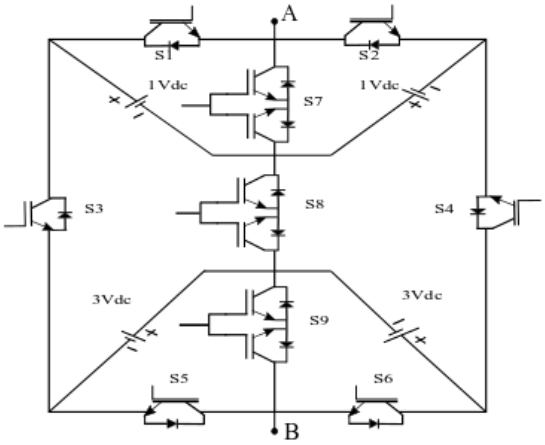


Fig. 4. ST-type module MLI.

Xu et al. [20] proposed a T2C converter for a low switching frequency MLI. The authors claimed to combine the merit of low conduction loss in two level converter and superior quality output of the three level converters. The system utilizes a bidirectional switch connection between the dc link midpoint voltage and

the output. The conduction losses in the converter topology are minimized with this interconnection. Even though THD levels are within the limits, the number of switching devices and the practical application of this topology is a major concern. Raman et al. [21] proposed a multi input switched capacitor MLI(SCMLI) for high frequency application where the availability of asymmetric dc sources are present. Inherent capacitor voltage balancing is claimed to be the vital specialty of this converter topology. The proposed systems lack detailed investigation on harmonic performance under varying load conditions. The major challenge pertaining to battery powered multilevel inverter systems is the effective utilization of battery sources. The reliability of battery-powered systems are always questioned in terms of its capability to operate long duration with minimum degradation of performance parameters. Since the controlling of battery sources is a multivariable problem, fuzzy logic controllers will be better suited for achieving the solution as discussed in several research articles [22-24].

From the aforementioned literature review about T-type topologies and its modulation techniques it can be observed that, most of systems presented either fall short in its line THD performance or in its capability to operate efficiently from an isolated power supply source. Thus, the need to devise a novel topology of T-type multilevel inverter to cater the segment of isolated powered systems like industrial cranes, fork lifts, electric vehicles, etc., are very high. A novel design of circuit topology will be acceptable to the industry only if it possesses the capability to carry out multiple operations like charging the battery source along with optimized utilization of battery source. A novel topology also demands for a new modulation strategy since the conventional PWM techniques are prone to poor line THD.

This paper proposes a hybrid T-Type multilevel inverter topology with inherent charging capability. A novel VFOC modulation technique is also introduced for minimizing the line THD harmonics of the system. A two-input fuzzy logic controller is devised for the optimized utilization of isolated power supply sources.

The structure of this paper is as follows: In Section 2, proposed topology is explained in detail, Section 3 details the VFOC modulation technique employed in the proposed system. Section 4 explains about the inherent battery charger in the proposed system and Section 5 details about the design of a fuzzy logic controller. Section 6 discusses about simulation and hardware results.

2. Proposed System

In view of the stated literature, this paper aims to introduce a battery powered Modified T-Type ANPC topology with a hybrid modulation strategy suitable for low power critical circuits. Battery powered or independent DC sources are related to the category of isolated power supply systems. The proposed topology is a congregation of an ANPC and T type MLI structure as shown in Fig. 5. To obtain five levels in phase voltage, nine power semiconductor switches S1-S9 are used. The topology is designed to work as a boost rectifier also for charging operation of battery source. This peculiarity makes the topology multifunctional in operation.

In general, to achieve ‘n’ levels in phase voltage and 2n-1 levels in line voltages (for three phase topology), 5+(n-1) switches are required per phase, where four switches are for the H bridge and five switches are for the ANPC -T type inter

connection. The proposed system uses three DC sources and two floating capacitors. The floating capacitors are C1 and C2 are dedicated for the T-bridge.

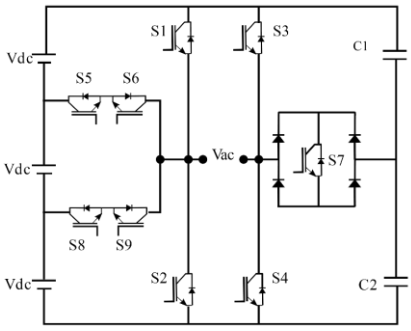


Fig. 5. Proposed hybrid T-type five level MLI.

Voltage level obtained are V/6, V/3, V/2, 2V/3, and V, where V is the input dc voltage. The switching states are shown in Table 1.

Table 1. Voltage levels/switching states of the proposed converter switching states.

Voltage levels	S1	S2	S3	S4	S5	S6	S7	S8	S9
(+)V	1			1					
(+)2V/3				1		1			
(+)V/2	1						1		
(+)V/3				1					1
(+)V/6						1	1		
0V		1		1					
(-) V/6							1	1	
(-) V/3			1		1				
(-) V/2		1					1		
(-)2V/3			1					1	
(-)V		1	1						

(S1, S2), (S3, S4), (S5, S6) and (S8, S9) are the four pairs of complementary switching states involved in the generation of output voltage levels. Consider S*f*1 to S*f*9 as the switching function for switches S1-S9. The switching function takes either logic 0 for OFF condition or logic 1 for ON condition. The output phase voltage V_{ph} can be determined from the mathematical Eqs. (1) and (2)

$$\overline{Sf2}\left[\frac{Vdc.Sf1}{4}+\frac{3Vdc.Sf4}{4}-\frac{Vdc.Sf6}{12}+\frac{Vdc.Sf7}{4}-\frac{5Vdc.Sf9}{12}\right]=V_{ph(+)} \quad (1)$$

$$\overline{Sf4}\left[\frac{-Vdc.Sf2}{4}-\frac{3Vdc.Sf3}{4}+\frac{Vdc.Sf8}{12}-\frac{Vdc.Sf7}{4}+\frac{5Vdc.Sf5}{12}\right]=V_{ph(-)} \quad (2)$$

Equations (1) and (2) depicts the generation of positive and negative phase voltages. i.e., for generating a phase voltage of V/2, switches S1 and S7 will be ON, which make the switching function S*f*1 and S*f*7 to be 1 and rest switching states 0. Substituting the switching state in (1) gives:

$$1\left[\frac{Vdc.1}{4}+\frac{Vdc.1}{4}\right]=\frac{Vdc}{2}= \quad V_{ph(+)} \quad (3)$$

Some of the obvious advantages of the proposed topology are (1) ease of extension to generate higher number of voltage levels due to its modularity (2)

inherent capacitor voltage balancing due to the bifurcation in floating capacitors (3) lower number of circuit components and reduced switching losses. Discussions pertaining to higher voltage levels are withheld in this paper to avoid complexity due to higher number of switching states.

3. Hybrid Modulation Technique

The novel hybrid modulation technique with VFOC triangular carriers are compared with a reference sine wave to generate the switching signals. Yu et al. [13] discussed that this hybrid modulation technique, which is a modification of the phase disposed sine pulse width modulation (PD-SPWM) scheme.

PD-SPWM is widely accepted as a modulating technique for MLI's due to its simplicity and inherent capacitor voltage balancing.

The modulation amplitude m_a (modulation index) is given by:

$$m_a = \frac{Amplitude\ of\ the\ Reference\ Signal(Sine\ Wave)}{(n-1).Amplitude\ of\ the\ Carrier} \tag{4}$$

where 'n' is the number of phase voltage levels. Modulation frequency can be expressed as

$$m_f = \frac{frequency\ of\ the\ Carrier}{frequency\ of\ the\ modulating\ wave} \tag{5}$$

The value of m_f is selected to be 40 in the proposed method. Arrangement of triangular carriers and sinusoidal reference signal in the proposed hybrid modulation scheme is shown in Fig. 6.

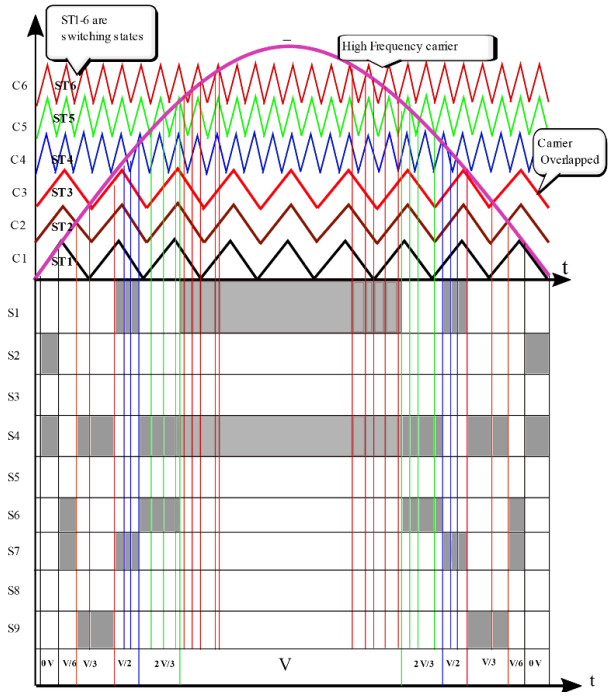


Fig. 6. VFOC modulation strategy for generation of phase voltages 0V, V/6, V/3, V/2, 2V/3 and V,S1-S9-semiconductor switches, C1-C6-carrier waveforms.

Amplitude of the carrier signals can be calculated as:

$$A_c = \frac{\text{Aref}}{n-1} \tag{6}$$

where A_{ref} is the amplitude of reference sine wave and A_c is the amplitude of carrier. The carrier signals are overlapped by a factor corresponding to the modulation index as per the control strategy shown in Fig. 7.

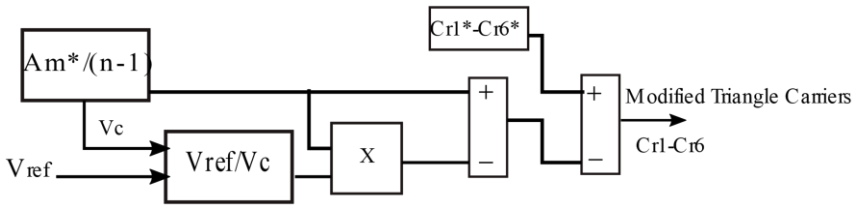


Fig. 7. Block diagram showing the control strategy for carrier overlapping.

Since the number phase voltage levels are restricted to five, there are six switching states ST1- ST6 and six carriers Cr1- Cr6. The frequency "f" of carriers corresponding to the states ST1-ST3 are switching at a frequency of "f/2" with respect to the frequency of carriers switching from ST4- ST6.

This particular strategy in carrier modulation is adopted to minimize the harmonic content in the output waveform. From the observed harmonic spectra shown in Section VI two observations can be made:

- Even order harmonic content is zero and the 3rd, 5th , 7th, 9th and 11th order harmonics are mitigated from the output waveforms.
- Linear variation of the output voltage is obtained even at low modulation index, m_a=0.1. The voltage levels are maintained upto a modulation index of 0.4.

4. Integrated Battery Charger

The H- Bridge in the proposed topology comprising of switches S1,S2,S3 and S4 are intended to perform the operation of a PWM rectifier also as shown in Fig. 8. This mode of operation can charge the inverter's battery source through a controlled boost rectification. Single-phase PWM rectifiers are mainly used for rectification purpose in order to preserve the quality of input sinusoidal waveform and maintain unity power factor [25]. An AC side inductor (Ls) shall be added with the bridge topology to achieve the boost rectification.

The operation is divided into four modes over positive and negative half cycles of input AC voltage: Mode I and II will be operating only during the positive phase of the supply voltage. The boost inductor Ls stores energy during mode I when the switch S2 is ON through Vs-Ls-S2-D4. In mode 2, when S2 is off the inductor will discharge through Vs-Ls-D1 and to the battery bank and D4. Mode III and IV will be operating during the negative phase of the supply voltage. During mode III, S1 will be on charging the inductor with current path Vs-D3-S1-L. Discharging of inductor takes place during mode IV when switch S1 is OFF through Vs-D3-Battery bank - D2 and L.

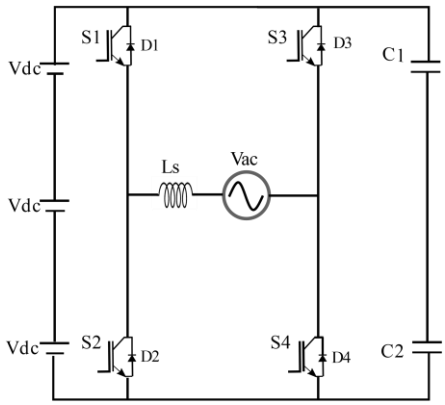


Fig. 8. Integrated boost rectifier circuit.

Inductive element is used for the boost operation and bidirectional power flow whereas the capacitor is included in the circuit to maintain the constant DC output to the load. The output voltage obtained from the boost rectifier is given by:

$$\frac{V_s M}{1-d} \tag{7}$$

$V_s - Supply\ voltage$, M-Modulation Index, d=switching period.

Inductance value is calculated by

$$L = \sqrt{(V_r^2 - V_s^2) + (\omega^2 I_s^2)} \tag{8}$$

where V_r is the voltage at the converter terminals, V_s is the source voltage. I_s is the source current.

Capacitance is calculated by $C \geq \frac{(M.I_S)}{4\omega\Delta V}$ (9)

M is the modulation index and ΔV is the ripple voltage

The capacitance value is adjusted to match the circuit floating capacitor and the inductance value is calculated to be 7.5 mH for a boost rectified DC voltage of 300 V. The boost rectified DC voltage obtained through the charging operation is shown in Fig. 9.

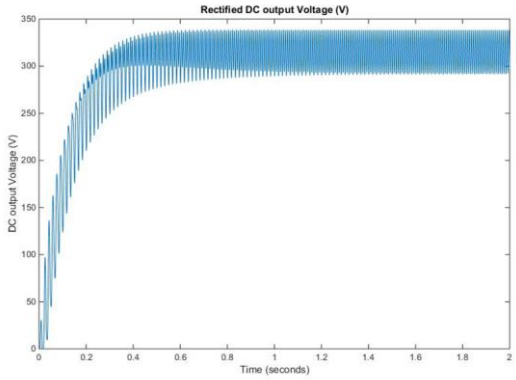


Fig. 9. Boost rectified DC output voltage from integrated charger.

5. Design of Fuzzy Logic Controller for Battery Management

A fuzzy system is designed to control the SoC (state of charge of the battery) for the optimised utilisation of isolated power supply source. As the state of charge of battery deteriorates during usage, the modulation index as well as the overlap factor of the triangle carriers are adjusted to sustain the operation of the inverter. Monitoring the SoC can avoid fast battery charge dissipation. Battery SoC and rate of change of SoC are taken as the input variables, modulation index and carrier overlap factor are the output variable. Fuzzy system is divided to three process as shown in Fig. 10, i.e., fuzzification, inferencing and defuzzification.

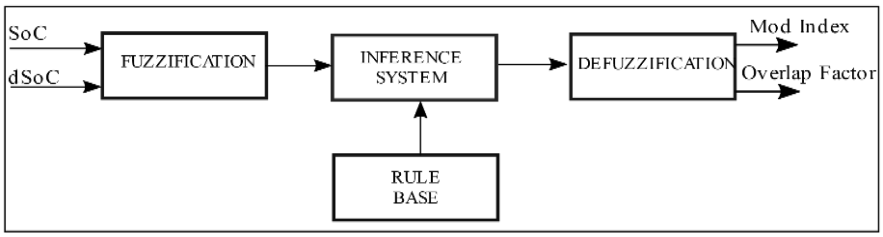


Fig. 10. Block diagram of fuzzy control system.

The input variable are converted to linguistic range. Universe of discourse of input variables battery state of charge (SoC) and change of SoC(dSoC) has three and five subsets respectively. Universe of discourse of the output variables, modulation index and overlap factor has three subsets each. The inference mechanism uses IF THEN rule base as shown in Tables 2 and 3 to define a fuzzy relationship between the input and output variables.

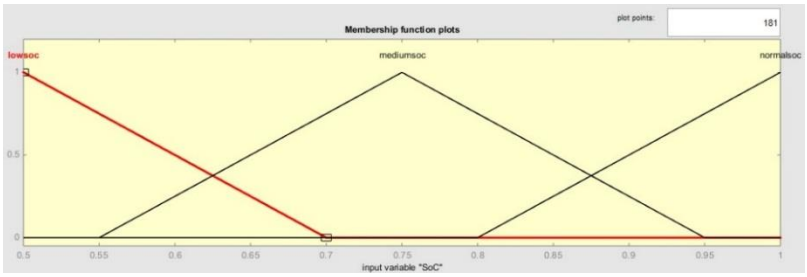
Table 2. Rule table for modulation index.

Modulation index		Change in SoC(dSoC)				
		VL	**L**	**Med**	**High**	**Very High**
SoC	L	L	L	L	L	L
	M	M	M	M	L	L
	N	H	H	H	M	M

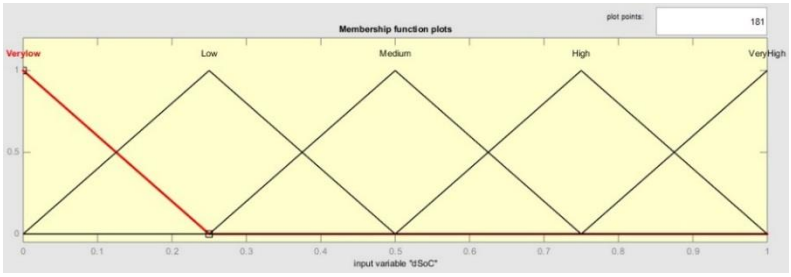
Table 3. Rule table for overlap factor.

Overlap factor		Change in SoC(dSoC)				
		VL	**L**	**M**	**H**	**VH**
SoC	L	H	H	H	H	H
	M	M	M	M	H	H
	N	L	L	L	M	M

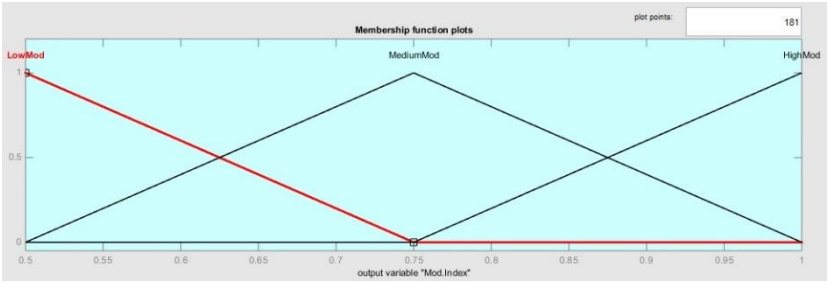
Fuzzy set for the input variable SoC is {L, M, N} and the range of SoC is selected from 0.5 to 1. Rate of change of SoC is defined by fuzzy set {VL, L, M , H,VH} the basic domain is [0 1]. Figure 11 shows the membership functions for the input and output variables.



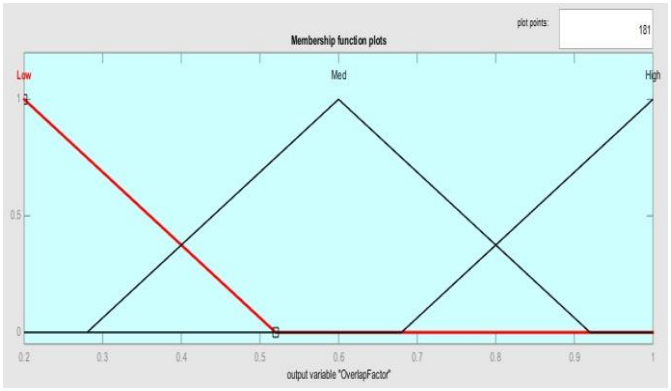
(a) SoC.



(b) dSOC and output variables.



(c) Modulation index.



(d) Overlap factor

Fig. 11. Membership function of input variables: (a) SoC, (b) dSOC and output variables, (c) Modulation index and (d) Overlap factor.

Surface view output of the controller between Modulation index, dSoC, and SoC. is shown in Fig. 12.

A Mamdani fuzzy inference system is used with triangular membership function to achieve high sensitive response. Centroid method is applied for the process of defuzzification.

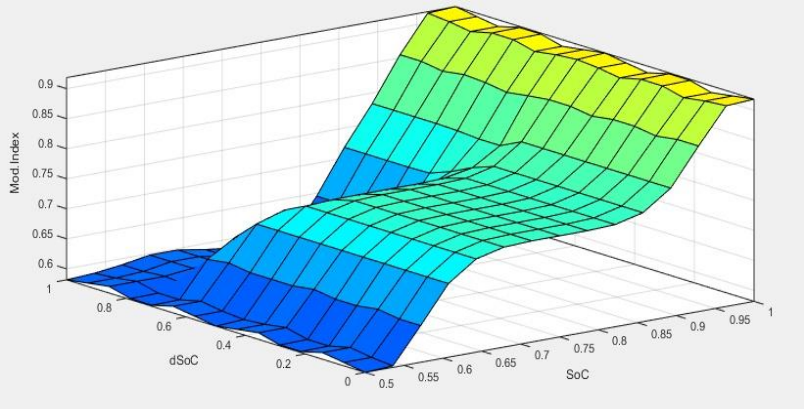


Fig. 12. Surface view output of fuzzy controller.

6. Results and Discussion

6.1. Simulation results

The single-phase five-level hybrid T-type MLI is simulated in MATLAB Simulink environment with VFOC based PWM method. Simulation parameters are shown in Table 4.

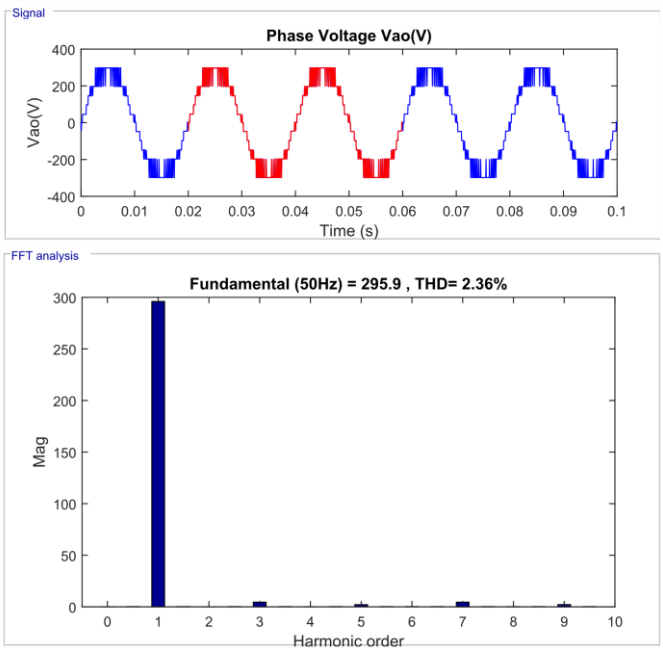
Table 4. Simulation parameters of the proposed system.

Particulars	Specification
Input DC voltage (VDC)	300 V
Switching frequency	2000 Hz
Output frequency	50 Hz
Floating capacitor(C1-C2)	4700 μF
RL,Load	12 Ω, 5 mH

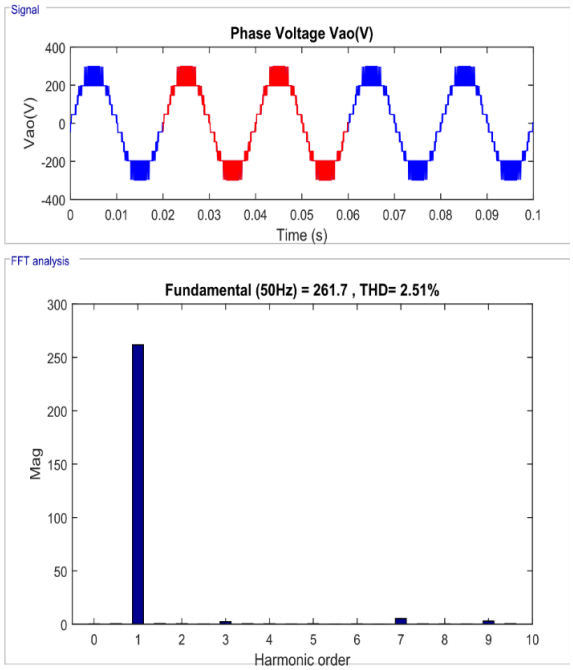
Analysis has been done in the proposed Hybrid MLI for various modulation indices and loads. The harmonic spectra of the output waveforms prove the effectiveness of the modulation technique in reducing the higher order harmonics.

Figures 13 and 14 show the output phase voltage and harmonic spectrum of the proposed MLI for different modulation indices.

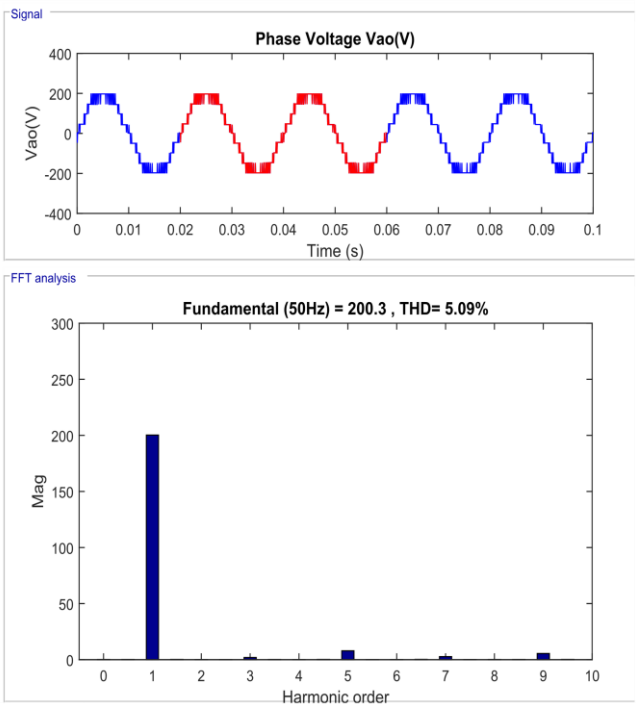
Vemuganti et al. [16] presented the simulation results of the proposed system, which have been compared with the results where a five level T-type multilevel inverter is presented with a dual reference modulation strategy.


Signal
Phase Voltage Vao(V)
Vao(V)
Time (s)
FFT analysis
Fundamental (50Hz) = 295.9 , THD= 2.36%
Mag
Harmonic order

(a) $m_a = 1.$

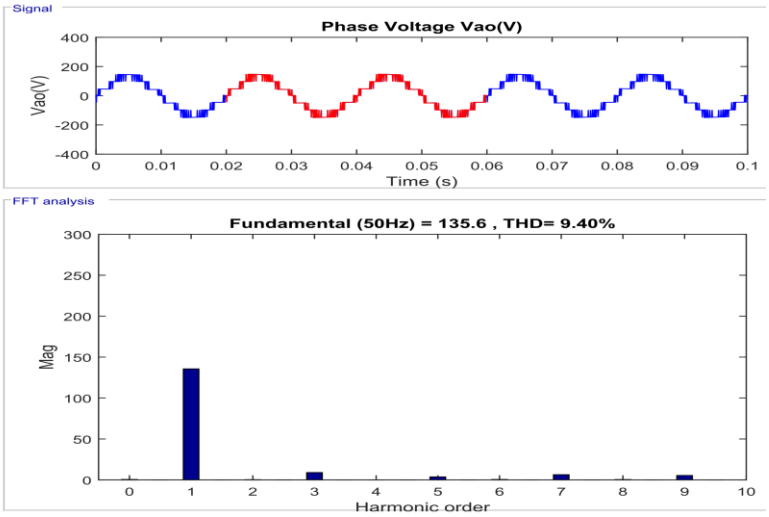

Signal
Phase Voltage Vao(V)
Vao(V)
Time (s)
FFT analysis
Fundamental (50Hz) = 261.7 , THD= 2.51%
Mag
Harmonic order

(b) $m_a = 0.8.$

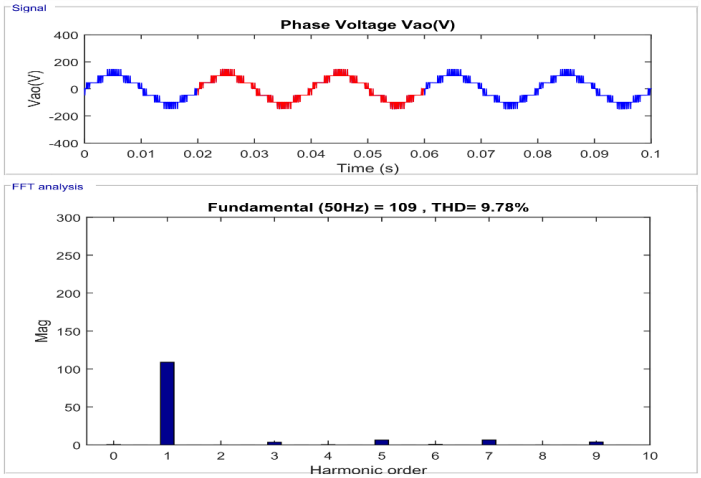


(c) $m_a = 0.6$.

Fig. 13. Output phase voltage and harmonic spectra for (a) $m_a = 1$ (b) $m_a = 0.8$ (c) $m_a = 0.6$.



(a) $m_a = 0.4$.



(b) $m_a = 0.3$.

Fig. 14. Output phase voltage and harmonic spectra for (a) $m_a = 0.4$ (b) $m_a = 0.3$.

Variation of parameters in Figs. 13 and 14 such as fundamental output voltage and THD with respect to the modulation index can be represented graphically as shown in Fig. 15.

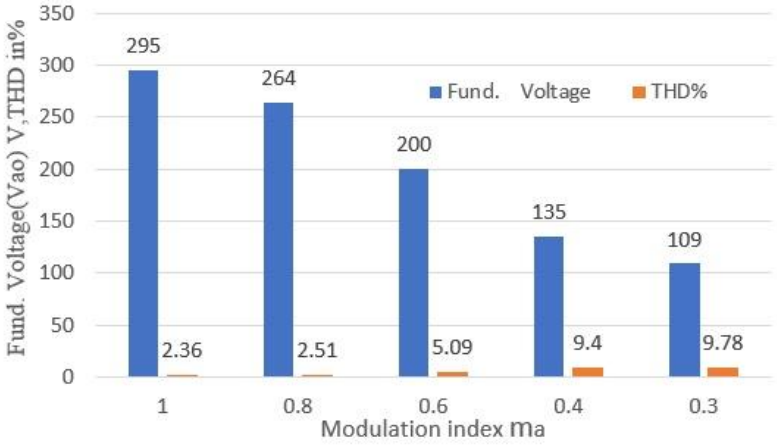
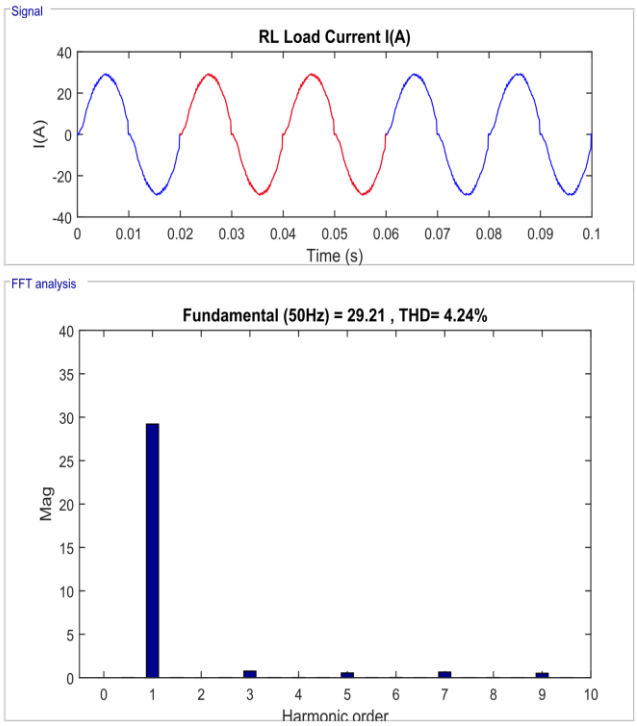
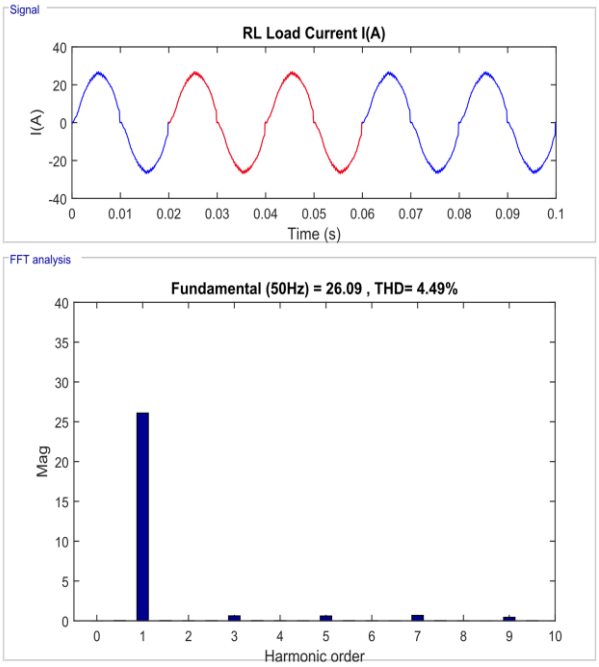


Fig. 15. Variation of voltage THD and fundamental output voltage with respect to modulation index m_a.

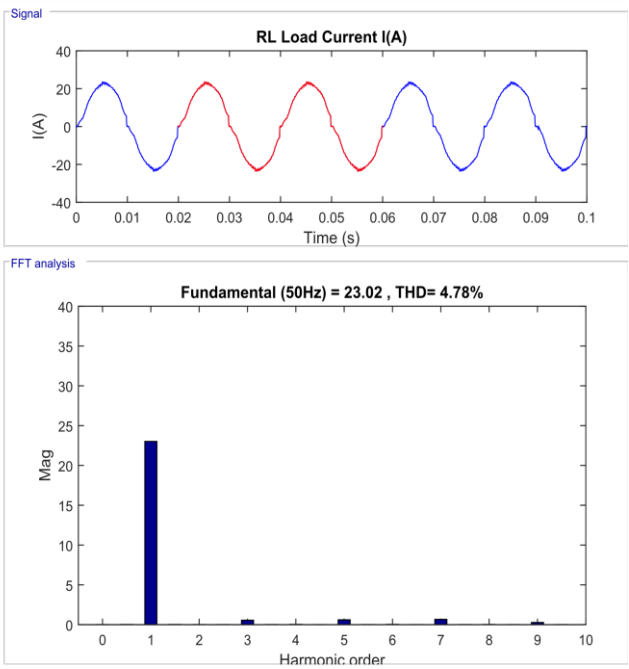
Analysis of proposed system has been conducted on RL load (R = 12 Ω, L=3 mH) from Fig. 16 a linear variation in output current can be seen with minimal increment in THD.


Signal
RL Load Current I(A)
I(A)
Time (s)
FFT analysis
Fundamental (50Hz) = 29.21 , THD= 4.24%
Mag
Harmonic order

(a) m_a = 1.


Signal
RL Load Current I(A)
I(A)
Time (s)
FFT analysis
Fundamental (50Hz) = 26.09 , THD= 4.49%
Mag
Harmonic order

(b) m_a= 0.8.



(c) m_a= 0.6.

Fig. 16. Load current I(A) with RL load for (a) m_a=1, (b) m_a=0.8 (c) m_a=0.6.

Variation in output parameters such as load current and THD with respect to modulation index m_a is diagrammatically represented in Fig. 17.

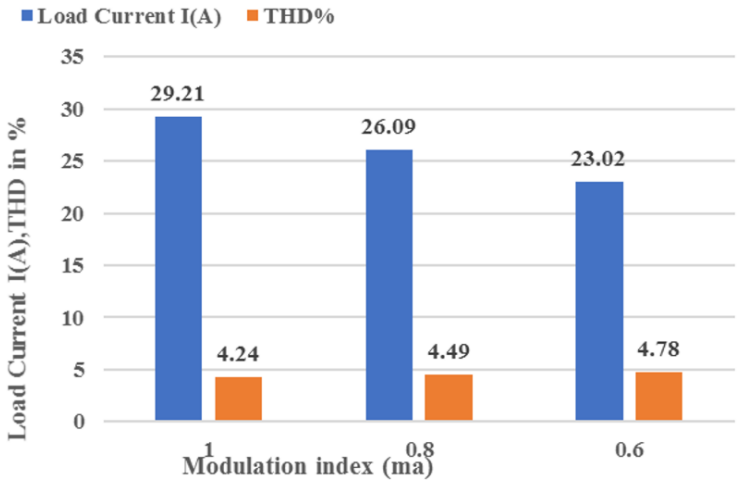


Fig. 17. Variation of current THD and load current with respect to modulation index m_a.

The harmonic spectra of the current waveforms shown in Figs. 16 and 17 sanction the proposed multilevel inverter for inductive loads such as low power motor drives, electric vehicles, portable cranes, etc.,

The above analysis shows that the change in modulation index gives a linear variation of output voltage and current keeping THD to the limit.

This linear variation is output voltage is achieved through the control strategy discussed in Fig. 7. The carrier control strategy also sustains the voltage levels even at low modulation index.

A graph plotting fundamental output voltage against modulation index in shown in Fig. 18. The graphs confirms linear relationship between output voltage and modulation index of the proposed system.

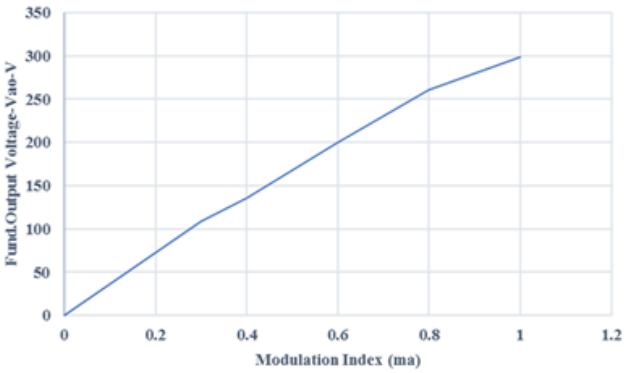


Fig. 18. Fundamental output voltage vs. modulation index.

Vemuganti et al. [16] discussed the comparison of harmonic spectrum pertaining to five level T-type MLI and cascaded H bridge MLI's, which are shown in Fig. 19.

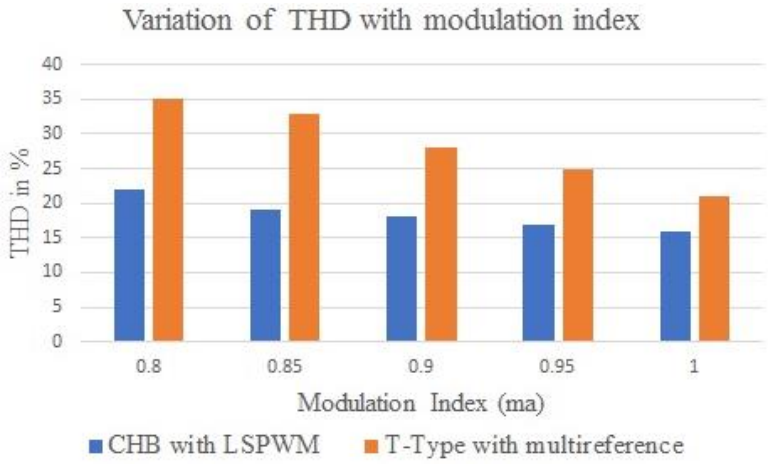


Fig. 19. Comparison of harmonic performance between T-type MLI and CHB MLI presented by Vemuganti et al. [16].

Vemuganti et al. [16] presented the variation of voltage THD for different modulation indices in Figs. 15 and 19 show that, for the topologies, the THD levels are in the range of 17-25% even for higher modulation indices.

Whereas the maximum THD of proposed MLI even at a lower modulation index of 0.3 is 9.78%. On comparison of Figs. 15 and 19, it can be justified that the proposed hybrid T-Type multilevel inverter with a VFOC modulation strategy can operate efficiently with a better harmonic spectrum and linear modulation index.

The proposed system can also be allowed to generate output ac waveforms for higher frequency applications (> 400 Hz) also, since the duty ratio of switches other than the H bridge module are very low.

High frequency operation can improve the inherent capacitor balancing capability of the system. Figure 20 shows the FFT analysis of the proposed prototype modified for a 115 V_{AC}, 400 Hz supply.

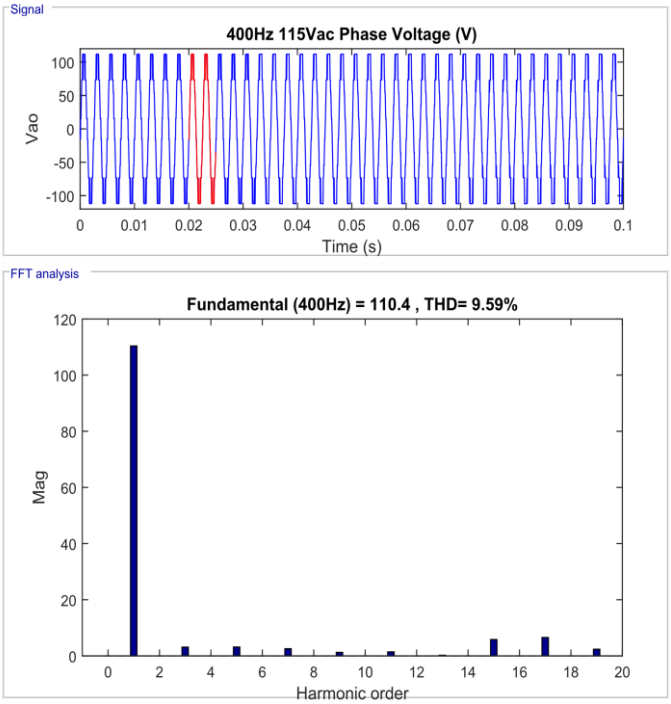


Fig. 20. 400 Hz, 115 V_{ac} output of MLI at m_a=1.

Higher order harmonics 3rd, 5th, 7th are eliminated and a small magnitude of 9th order harmonics can be observed from the harmonic spectra of output phase voltage. From the FFT analysis we can see that even for a high frequency operation (Fundamental frequency=400Hz, Carrier frequency=16000 Hz) THD levels are maintained at acceptable levels for high frequency operation also.

This response of the proposed system makes it suitable for high frequency applications in field of aerospace and telecommunication. Table 5 compares with the conventional T-type and ANPC multilevel inverters with the proposed system.

Table 5. Comparison of the proposed system with its conventional counterparts.

Type of MLI	No. of switches	No. of capacitors	No. of DC sources	THD (%)
5-Level ANPC	12	2	1	20
7 Level-T type MLI	8	3	1	15
7 Level-SCMLI	7	2	2	10
Proposed 11 level MLI (50Hz)	9	2	3	3
Proposed 11 level MLI(400Hz)	9	2	3	9.5

6.2. Capacitor voltage balancing

Capacitor voltages are balanced inherently with the VFOC modulation method as shown in Fig. 21. The switching cycles are arranged in such a way that the duty cycle for a particular capacitor voltage falls within the duration of switching state.

Hence, the charging and discharging period of floating capacitors will not affect the output voltage of the system.

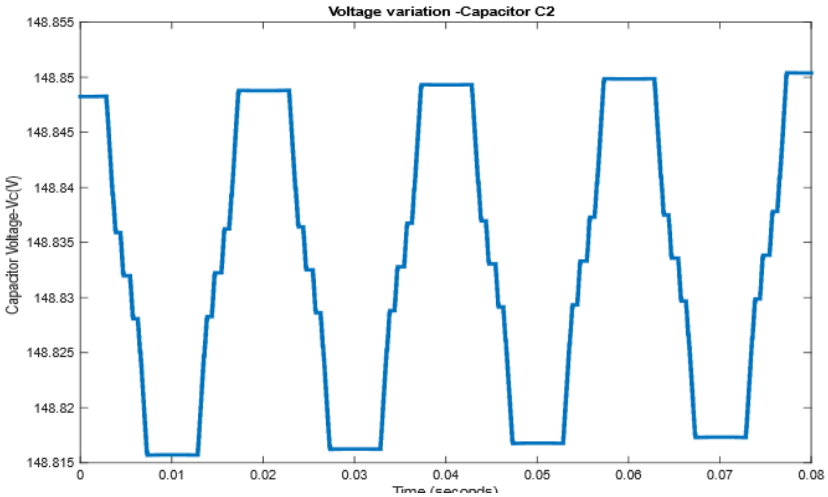


Fig. 21. Charging and discharging cycles of capacitor C2.

Figure 22 shows the hardware switching pulses generated through VFOC modulation technique, fed to switches S1-S9 at a frequency of 2 kHz.

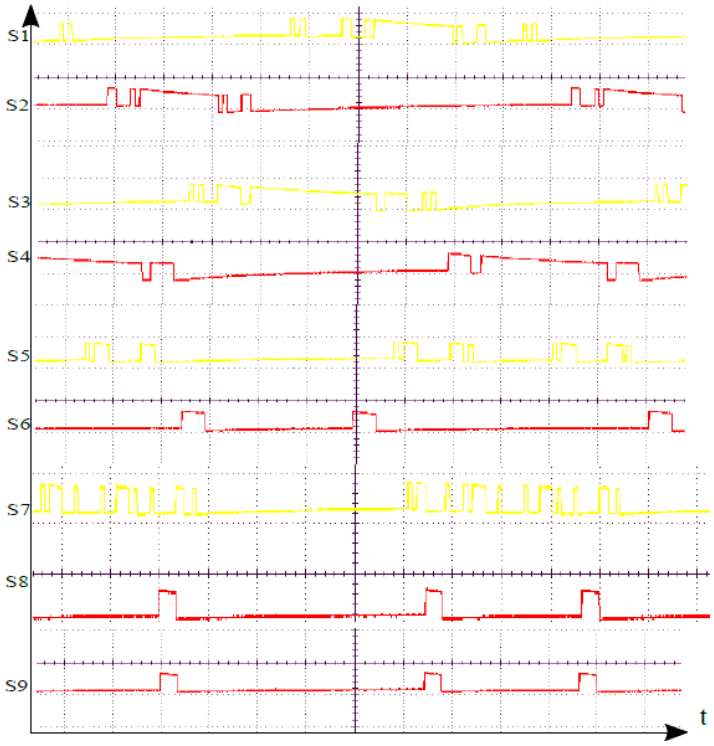


Fig. 22. 2 kHz hardware switching signals fed to switches S1-S9.

6.3. Hardware prototype

A low power experimental model of the proposed 11 level MLI is developed and tested for confirming the practicability of the proposed system. Specification of components used in hardware prototype is shown in Table 6.

Table 6. Specification and components list for the 11 level proposed MLI.

Particulars	Specification
Semiconductor switch, IGBT	FGA25N120
Electrolytic capacitor	4700µF
Diode	IN540
DC source	36V
Microcontroller	Arduino Mega 2560

Hardware prototype as shown in Fig. 23 is developed for an input DC voltage of 36 volts with three independent battery sources of 12 volts. The hardware prototype is divided into three sections; Active neutral point clamped section, T-type H Bridge section and floating capacitor section. Arduino Mega microcontroller is dedicated with the objective of switching signal generation along with parameter monitoring and control. The 36 volts prototype is also simulated in MATLAB Simulink to reaffirm the workability of the system with very low voltage systems.

Figure 24 shows the output phase voltage and harmonic spectra for a modulation index of 0.9.

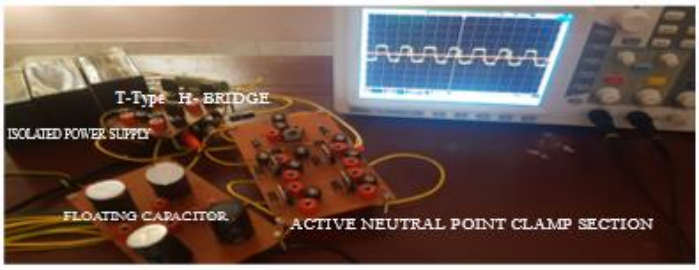


Fig. 23. Annotated photograph of the hardware prototype.

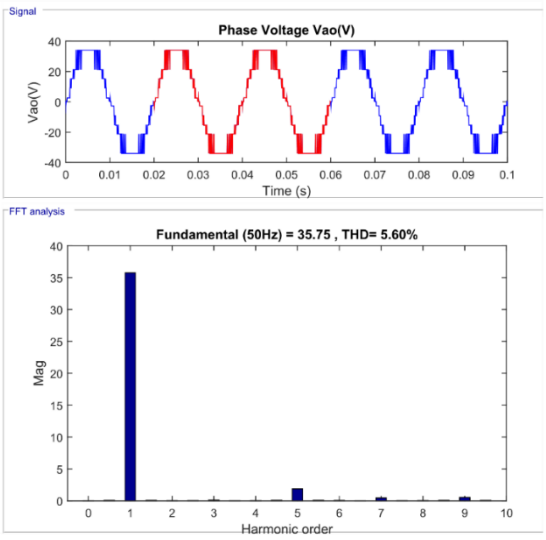


Fig. 24. Output phase voltage and harmonic spectra for $m_a = 0.9$.

The hardware prototype has been tested under varying load conditions and different modulation indices to confirm the adaptability of the system in rugged industrial conditions. Output phase voltage of the proposed system at a modulation index of 0.2 is shown in Fig. 25. The output waveform confirms that, even at a low modulation index of 0.2 the voltage levels are maintained without considerable degradation in the harmonic spectrum.

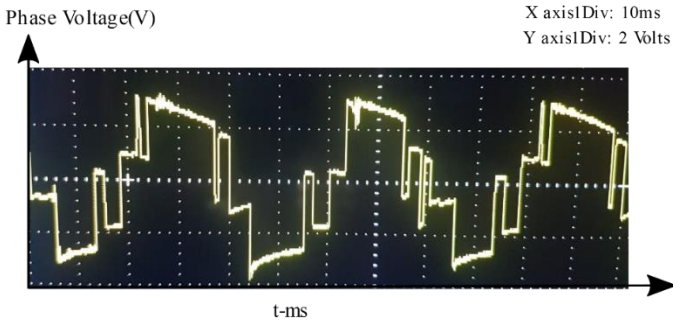


Fig. 25. Output phase voltage of 36 V system with modulation index $m_a = 0.2$.

7. Conclusion

A hybrid T-Type multilevel inverter is presented in this paper with a novel VFOC modulation strategy. The proposed system caters toward applications under low power category with isolated power supply sources. The proposed topology operates in inversion mode for driving electrical loads and conversion mode for charging batteries. A fuzzy logic controller is employed for the optimised utilization of the battery sources in the system. Analysis of simulation results from MATLAB/Simulink model confirms that the hybrid T-Type multilevel inverter with VFOC modulation strategy is inherently capable of capacitor voltage balancing and harmonic reduction. The proposed system can also accommodate high frequency (400 Hz , 115 Vac) operation without any change in the circuit topology due to its peculiarity. A laboratory prototype has been built and tested to substantiate the validity of simulation results.

Nomenclatures

A_c	Amplitude of carrier wave
A_{ref}	Amplitude of reference wave
C	Capacitance, mF
L	Inductance, mH
m_a	Modulation index
m_f	Modulation frequency
V_{dc}	DC voltage, V
V_{ph}	Phase voltage, V

Abbreviations

ANPC	Active Neutral Point Clamped
dSoC	Change of SoC
MLI	Multilevel Inverter
NPC	Neutral Point Clamped
SoC	State of Charge
THD	Total Harmonic Distortion
VFOC	Variable Frequency Overlapped Carrier

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