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PERFORMANCE EVALUATION OF SWITCHED-DIODE SYMMETRIC, ASYMMETRIC AND CASCADE MULTILEVEL CONVERTER TOPOLOGIES: A CASE STUDY

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Abstract

In this paper, a precise study is presented on switched-diode symmetric, asymmetric and cascade multilevel converter topologies, which have been introduced and published recently. According to the published papers, these topologies have many advantages over other topologies in the same class. However, it is proved here that the mentioned switched-diode topologies suffer from main problems, which make them completely impractical. First, a brief study is presented on a typical sub-multilevel converter that consists of a basic unit and an H-bridge converter. Then, extended inverter topologies based on the switched-diode basic unit and their problems are studied. It is revealed in this section that the main problem is because of the basic unit. Finally, comprehensive experimental and simulation results are presented to validate the analysis. The simulations have been performed in MATLAB/SIMULINK environment.

Keywords: Switched-capacitor, Sub-multilevel inverter, Symmetric, Asymmetric, cascaded.

1. Introduction

A multilevel converter is a power electronic based system, which its general function is to synthesize a near sinusoidal staircase voltage waveform from several levels of DC sources [1]. In recent years, multilevel converters have received wide attention of many researchers in medium and high voltage applications [2-7], such as induction machine and motor drives, interface of renewable energy sources, flexible AC transmission systems (FACTS). This popularity is because of their lower common mode voltage, lower voltage stress on power switches and lower harmonic contents in output voltage and current [6, 7]. The most famous conventional multilevel structures are grouped as diode clamped converter, flying capacitor converter and cascaded H-bridge converter [6, 7].

A multilevel converter structure has been introduced in [8], which needs fewer numbers of switches, compared with conventional cascade topology. However, this topology cannot create all steps (odd and even) at the output voltage and needs large numbers of bidirectional switches for creating the output voltage for a given number of steps. In order to overcome these disadvantages, a novel multilevel converter structure has been proposed in [9]. This structure consists of series-connected sub-multilevel converters blocks. In addition, another structure for sub-multilevel converter has been proposed with reduced number of power electronic components in [10].

Recently, a new switched-diode multilevel converter has been introduced in [11-13]. According to [11-13], this structure requires minimum number of power electronic components and produces more number of levels. However, introduced basic circuit cannot work as assumed in [11-13] for proposed multilevel topologies. In other words, the author's assumption of functionality of basic circuit does not match with reality. As proved in this paper, the extended symmetric and asymmetric switched-diode converter based on this basic circuit can only deal with pure resistive loads (Power Factor=1). In addition, it is shown that the proposed cascade switched-diode converter topology based on the mentioned basic circuit, has unacceptable responses for any kinds of loads. This cascade topology is unable to generate all desired levels at the output voltage. Consequently, the performances of the switched-diode converter topologies are not acceptable generally. In other words, the aim of this paper is to critical study, review and shed light on some of the already published papers [11-13], which have natural inability to perform as claimed. Therefore, it can stop time, energy, and expenses, which might be wasted investigating those solutions.

2. Sub-Multilevel Converter

Figure 1 shows a typical structure of sub-multilevel converter, which includes an H-bridge converter and a basic unit. In general, the basic unit generates a staircase voltage waveform with positive polarity. Then, polarity of this voltage can be alternated by H-bridge converter and a positive or negative staircase waveform can be produced. It should be noted here that the output voltage of basic unit must be independent of its current direction.

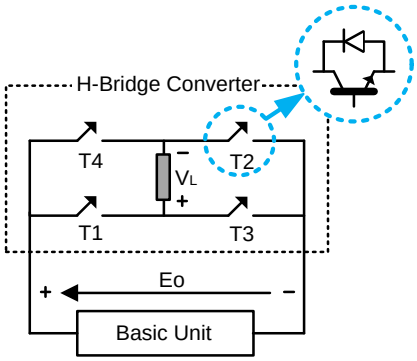
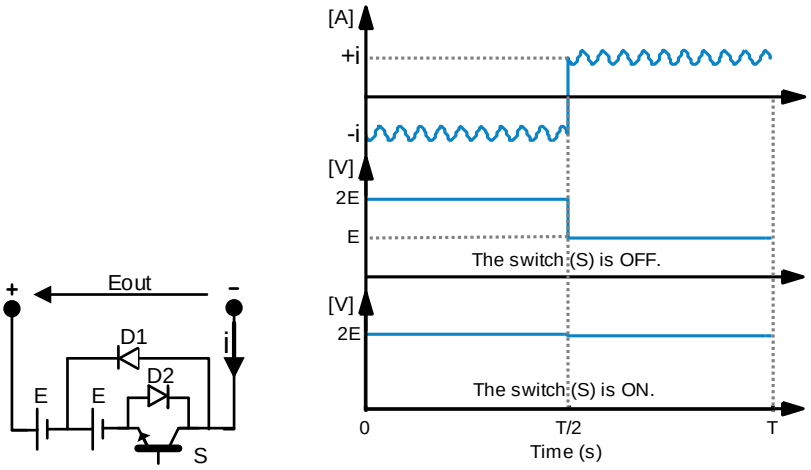


Fig. 1. Structure of a typical sub-multilevel converter.

3. Symmetric and Asymmetric Switched-Diode Multilevel Converter

The basic circuit of switched-diode sub-multilevel converter, presented in [11-13], is illustrated in Fig. 2(a). According to [11-13], the output voltage can be controlled between *E* and *2E* by turning off and on the switch *S* in this circuit. When the switch *S* is turned off, the current should flow through the diode D_1 and the output voltage must be *E*. When the switch *S* is turned on, the diode D_1 should be reverse biased and current must flow from both of the voltage sources and the output voltage will be *2E* [11-13]. However, this circuit can work properly if and only if the current flows in the specified direction, otherwise, the output voltage cannot be controlled correctly. As shown in Fig. 2(b), when the current flows in opposite of the specified direction for any reason, the output voltage of the circuit cannot be changed by changing the state of switch *S*, because the diode D_1 becomes open-circuit and D_2 will be conducting at all; therefore, the output voltage will be always equal to 2*E*. In other words, the output voltage of the basic circuit depends on its current direction, which will cause serious problems for converter topologies based on it.



(a) Proposed basic circuit. **(b) Output voltage (E_{out}).**

Fig. 2. Proposed basic circuit in [11-13] and its output voltage (E_{out}) for its output voltage (E_{out}) for different directions of current.

The proposed topology of switched-diode converter in [11-13] is shown in Fig. 3(a). It includes a basic unit and an H-bridge converter. In symmetric topology, all of the DC voltage sources have the same values:

$$E_1 = E_2 = ... = E_n = E \tag{1}$$

As mentioned before, the basic unit is responsible for generating a staircase voltage waveform. Then, this voltage will be alternated by the H-bridge converter. As a result, we can obtain a positive or negative staircase waveform at the output (±*E*, ± 2*E* ..., ± *(n* + 1)*E*) in symmetric topology.

In [12, 13], the switched-diode asymmetric converter topology has been introduced. For an increased number of output voltage levels with the same number of power electronic devices, asymmetrical topology is a suitable option, in which DC voltage sources are not equal:

$$E_1 \neq E_2 \neq ... \neq E_n \tag{2}$$

There are various methods for determining the values of these DC voltage sources. In [12], a method has been proposed for the asymmetrical switched-diode converter that is used here to study on this structure. According to the mentioned method, DC voltages are suggested to be chosen as shown below:

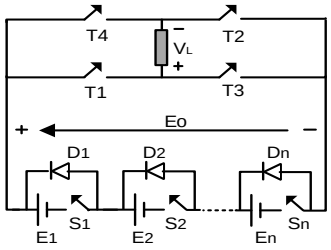
$$E_1 = E \tag{3}$$

$$E_j = 2^{(j-1)}E \qquad \text{for} \qquad j=2, 3,\ldots, n \tag{4}$$

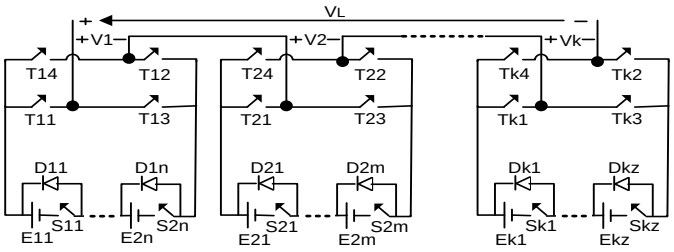
However, both symmetric and asymmetric topologies have an essential drawback for none-resistive loads (Power Factor≠1), which is caused by aforementioned problem about basic circuit. Because of phase difference between current and voltage in the case of none-resistive loads, there will be instants that the current flows in opposite of specified direction. Therefore, the basic unit will not be able to work properly. Therefore, its output voltage will be always equal to the sum of the DC link sources, as shown below:

For asymmetric: $$E_O = \sum_{j=1}^{n+1} (E_j) \tag{5}$$

For symmetric: $$E_O = E \times (n+1) \tag{6}$$



(a) switched-diode symmetric and asymmetric converter in [11-13].



(b) switched-diode cascade multilevel converter in [11-13].

Fig. 3. Proposed structures of switched-diode converters in [11-13].

4. Switched-Diode Cascade Multilevel Converter

For providing a large number of levels at the output voltage with minimum number of devices, cascade multilevel converter topology can be used. Figure 3(b) shows the structure of proposed switched-diode cascade multilevel converter in [11-13]. The,

output voltage of the proposed cascade multilevel converter is sum of the output voltages of the cascaded sub-multilevel converters, as expressed below:

$$V_L = \sum_{j=1}^{k} (V_j) \tag{7}$$

In fact, this cascade topology is not able to generate all the desired levels at the output voltage, which is caused by the mentioned problem about the basic circuit. According to [11, 12], it is necessary to subtract the output voltages of some of the sub-multilevel converters from the others in order to generate some of the levels in output voltage. It is obvious that there will be instants that the resultant current flows in opposite of specified direction for some of the sub-multilevel converters which are cascaded. Therefore, they cannot work properly and some of the levels at the total output voltage (V_L) cannot be generated.

5. Simulation and Experimental Results

In order to prove the mentioned defects about proposed switched-diode topologies in [11-13], the simulation results (in MATLAB/SIMULINK environment) and also experimental results are presented for three kinds of topologies. First, the simulation and experimental results are presented for a seven-level symmetric switched-diode converter. Then, a fifteen-level asymmetric switched-diode topology is considered. Finally, the experiments and simulations are performed for a twenty-five-level cascade switched-diode converter.

For multilevel converters, several switching techniques have been introduced like fundamental frequency-switching, sinusoidal PWM, etc. [7], [14, 15]. In this paper, the fundamental frequency-switching method has been used without considering calculation of the optimal switching angles, as used in [11-13]. As we know, the total harmonic distortion (THD) is a famous performance index for power converters, which for sinusoidal waveform can be expressed as below [11-13]:

$$THD = \frac{\sqrt{\sum_{h=3,5,..}^{\infty} (Voh)}}{Vo1} = \sqrt{\left(\frac{Vorms}{Vo1}\right)^2 - 1} \tag{8}$$

Where h is the order of harmonic. Therefore, V_{oh} is the rms of the h order harmonic of the output voltage. Additionally, V_{orms} is the rms value of the output voltage. In Eq. (8), the V_{o1} and V_{orms} can be calculated as shown below [11-13]:

$$V_{Orms} = \frac{2\sqrt{2}V}{\pi} \times \sqrt{\sum_{m=1,3,...}^{\infty} \left[\sum_{j=1}^{Nlevel} \frac{\cos(m\theta_j)}{m} \right]^2} \tag{9}$$

$$V_{O1} = \frac{2\sqrt{2}V}{\pi} \times \sum_{j=1}^{Nlevel} \cos(\theta_j) \tag{10}$$

where (θ_1, θ_2, ..., θ_{Nlevel}) are switching angles, which can be obtained as presented below [11, 13]:

$$\theta_j = \sin^{-1}\left[\frac{j-0.5}{N_{Level}}\right] \qquad J=1, 2, 3,\ldots, N_{Level} \tag{11}$$

For instance, a seven-level output waveform as sum of three-stepped waveforms is presented in Fig. 4(a). It is evident that THD has a direct relation with the number of levels and switching angles. It should be noted that the fundamental frequency is considered 50*Hz* for all simulations and experiments.

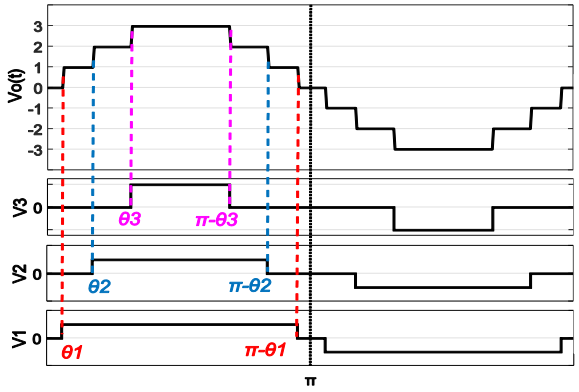
5.1. Seven-levels symmetric switched-diode converter

In this section, the simulation and experimental results for a seven-level symmetric switched-diode converter topology are presented. Figure 4(b) shows a seven-level symmetric switched-diode converter topology, which is presented in [12]. According to [12], we need three DC sources and six power switches for generating a seven-level output voltage. The magnitude of DC sources in this topology is considered E=116.7 V. As well as the switches, states for this symmetric converter are given in Table 1.

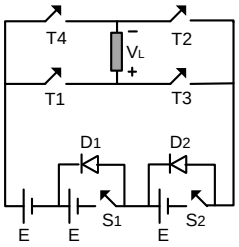
Table 1. Switches states of 7-level symmetric switched-diode converter.

States	Switches States						V_L
	T1	T2	T3	T4	S1	S2	
1	1	1	0	0	1	1	+350.1
2	1	1	0	0	1	0	+233.4
3	1	1	0	0	0	0	+116.7
4	1	0	0	1	0	0	0
5	0	0	1	1	0	0	-116.7
6	0	0	1	1	1	0	-233.4
7	0	0	1	1	1	1	-350.1

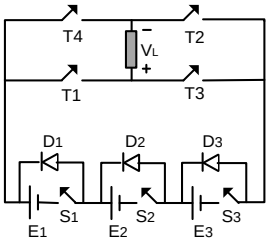
The output voltage of seven-level symmetric switched-diode converter (V_L) for different loads (Power Factor=0.7, 1) and their FFT analysis are shown in Fig. 5. Table 2 shows the simulation results for this seven-level structure for different power factors. It is obvious that the symmetric converter topology has undesirable performance for resistive-inductive loads (Power Factor≠1), which is because of the mentioned problem about the basic unit. It should be noted here that the presented results in [12] are insufficient and incorrect and cannot prove the performance of the seven-level switched-diode symmetric converter. The prototype of switched-diode converter topology is shown in Fig. 6, which consists of IXGH48N60C3D1 IGBTs (as switches), TLP250 as IGBT driver and ultra-fast diodes. The DC sources of the seven-level switched-diode symmetric prototype are considered 60 V. The experimental results of this seven-level switched-diode symmetric prototype are shown in Fig. 7. It should be noted here that the experimental results have been presented for the loads with the same power factor as used for the simulation of this seven-level symmetric switched-diode converter topology. Obviously, the experimental results (shown in Fig. 7) have excellent correspondences with simulation results (presented in Fig. 5). Consequently, the seven-level symmetric switched-diode converter topology can only work for the pure resistive loads properly.



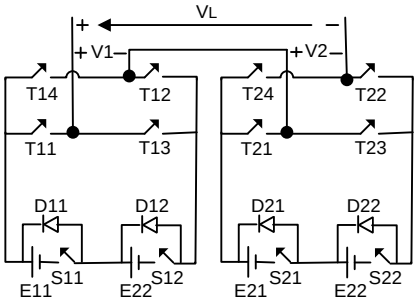
(a) 7-level output voltage of converter as a sum of 3-stepped waveform.



(b) 7-level symmetric topology.



(c) 15-level asymmetric topology.



(d) 25-level cascade topology.

Fig. 4. A sample 7-level output voltage of a converter; and different switched-diode converter topologies used in simulations and experiments.

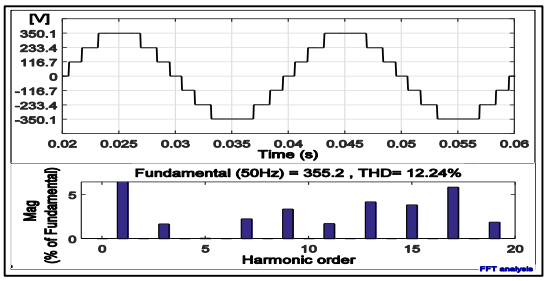
5.2. Fifteen-level asymmetric switched-diode converter

Figure 4(c) shows a fifteen-level asymmetric switched-diode converter topology, which is presented in [12]. According to [12], for generating a fifteen-levels output voltage, we need three DC sources and seven power switches and the magnitudes of DC sources in this topology should be considered E_1=50 V, E_2=100 V, E_3=200 V. The switches states for this converter are given in Table 3. The output voltage of fifteen-level asymmetric switched-diode converter (V_L) for different loads (Power Factor= =0.2, 1) and their FFT analysis are shown in Fig. 8. Table 4 shows the simulation results for this fifteen-level structure for different power factors. It is clear that the asymmetric converter topology has also unacceptable performance for

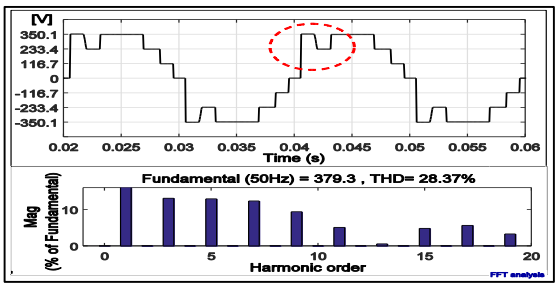
resistive-inductive loads. Figure 9 shows the experimental results of the fifteen-level asymmetric switched-diode converter topology. The DC sources of this topologies prototype are considered E_1=30 V, E_2=60 V and E_3=120 V. The experimental results have been presented for the loads, which have the same power factor as used for the simulation of this converter topology. The experimental results clearly have complete correspondences with simulations results, shown in Fig. 8.

Table 2. Simulation results of 7-level symmetric switched-diode converter for different power factors.

Resistive Load				
PF(cos φ)		**R (Ω)**	**$V_{L,Amp}$ (V)**	**THD%**
1		120	355.2	12.24
Inductive-Resistive Load				
PF(cos φ)	**R (Ω)**	**L (mH)**	**$V_{L,Amp}$ (V)**	**THD%**
0.9	108	166.5	361	24.05
0.8	96	229.2	370.2	27.57
0.7	84	272.8	379.3	28.37
0.6	72	305.6	386	28.34
0.5	60	330.8	393.6	27.36
0.4	48	350.1	401.6	25.6
0.3	36	364.4	404.4	25.02
0.2	24	374.3	404.7	24.98
0.1	12	380.1	403.8	25.15
Inductive Load				
PF($cos\varphi$)		**L (mH)**	**$V_{L,Amp}$ (V)**	**THD%**
0		382	394.7	26.65



(a) Load with PF=1.



(b) Load with PF=0.7.

Fig. 5. Output voltage and FFT analysis of 7-level symmetric switched-diode converter for different loads.

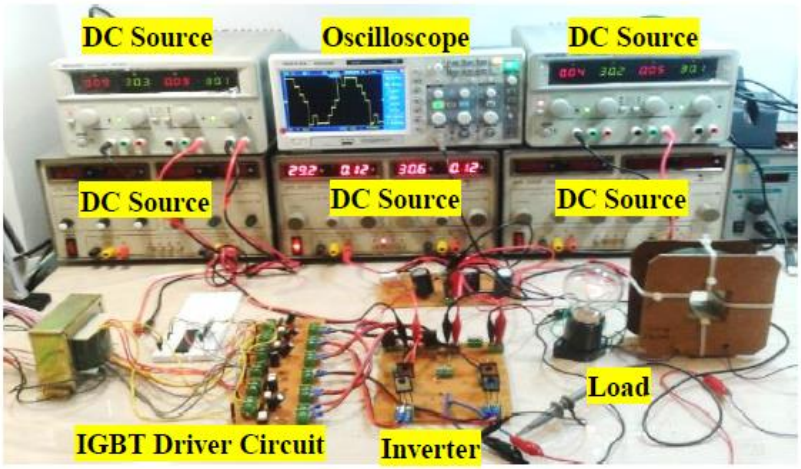
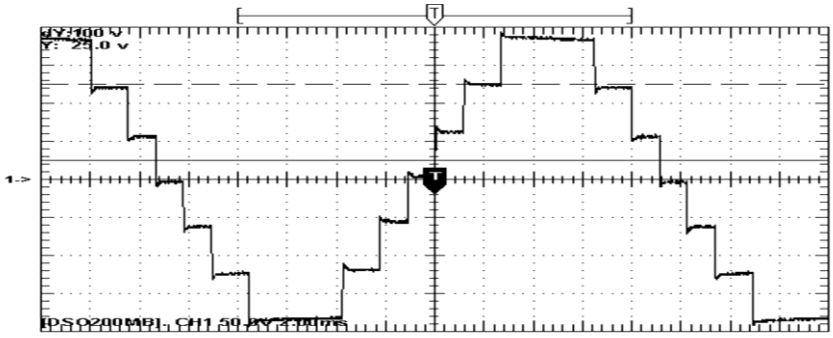
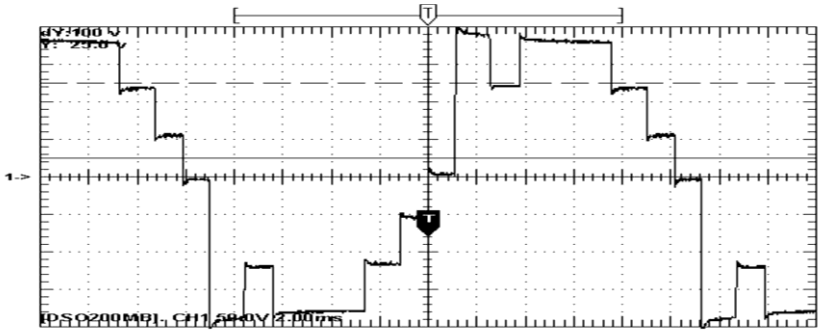


Fig. 6. Experimental circuit of switched-diode converter.



(a) Load with PF=1.



(b).Load with PF=0.7.

Fig. 7. Output voltage of 7-level asymmetric switched-diode converter prototype for different loads.

Therefore, the fifteen-level asymmetric switched-diode converter topology can only work for the pure resistive loads (Power Factor=1).

Table 3. Switches states of 15-level asymmetric switched-diode converter.

States	Switches States							V_L
	T1	T2	T3	T4	S1	S2	S3	
1	1	1	0	0	1	1	1	+350
2	1	1	0	0	0	1	1	+300
...	...	...	...	...	...	...	...	...
6	1	1	0	0	0	1	0	+100
7	1	1	0	0	1	0	0	+50
8	1	0	0	1	0	0	0	0
9	0	0	1	1	1	0	0	-50
10	0	0	1	1	0	1	0	-100
...	...	...	...	...	...	...	...	...
14	0	0	1	1	0	1	1	-300
15	0	0	1	1	1	1	1	-350

Table 4. Simulation results of 15-level asymmetric switched-diode converter for different power factors.

Resistive Load				
PF(cosφ)		R **(Ω)**	$V_{L,Amp}$ **(V)**	**THD%**
1		120	348.6	5.54
Inductive-Resistive Load				
PF(cosφ)	R**(Ω)**	L**(*mH*)**	$V_{L,Amp}$ **(V)**	**THD%**
0.9	108	166.5	355.4	26.02
0.8	96	229.2	365	30.16
0.7	84	272.8	374.2	31.02
0.6	72	305.6	381.8	30.78
0.5	60	330.8	390.3	29.78
0.4	48	350.1	397.1	28.61
0.3	36	364.4	401.2	27.87
0.2	24	374.3	404.6	27.15
0.1	12	380.1	404.3	27.17
Inductive Load				
PF(cosφ)		L **(mH)**	$V_{L,Amp}$ **(V)**	**THD%**
0		382	396.5	28.37

5.3. Twenty-five-level cascade switched-diode converter

Figure 4(d) shows the structure of twenty-five-level switched-diode cascade topology presented in [12]. According to [12], magnitudes of DC sources in this topology should be equal to E1=30 V and E2=150 V for generating a twenty-five-level output voltage with maximum amplitude of 360 V.

As well as, the switches states for this converter are given in Table 5. Figure 10 shows the output voltages of twenty-five-level cascade topology (V_L) and two cascaded converters (V_1 and V_2) for a pure resistive load (Power Factor = 1) and switching pulses for the switches S11 and S12. The results are completely different

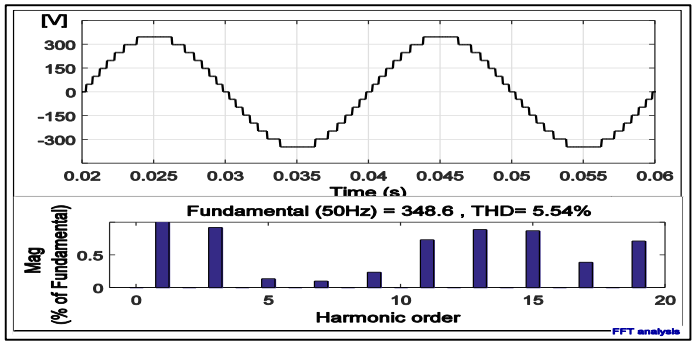
from the presented results in [12]. As we expected, this cascade structure has unacceptable results and cannot generate four voltage levels (±120 V and ±270 V) at output. For example to generate V_L= +270 V at t= t_1 s, the first and second converters should produce V_1= -30 V and V_2=+300 V. However, it can never happen, because the output voltage of second converter determines the direction of current. Therefore, the current will flow in opposite of specified direction for the first converter. This forces the first converter to generate $|V_1|$= 60 V at the output, regardless of states of the switches S11 and S12. As a result, V_L= +270 V cannot be generated at the output voltage of the cascade topology.

Table 5. Switches states for 25-level switched-diode cascade topology.

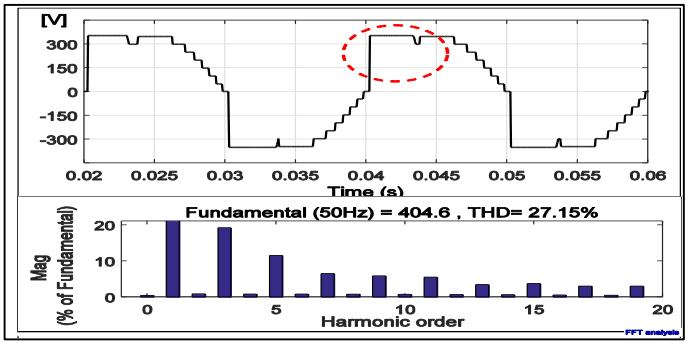
States	Switches States												V_1	V_2	V_L
	S11	S12	S21	S22	T11	T12	T13	T14	T21	T22	T23	T24			
1	1	1	1	1	1	1	0	0	1	1	0	0	+60	+300	+360
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
4	1	0	1	1	0	0	1	1	1	1	0	0	-30	+300	+270
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
9	1	0	1	0	0	0	1	1	1	1	0	0	-30	+150	+120
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
12	1	0	0	0	1	1	0	0	1	0	0	1	+30	0	+30
13	0	0	0	0	1	0	0	1	1	0	0	1	0	0	0
14	1	0	0	0	0	0	1	1	1	0	0	1	-30	0	-30
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
17	1	0	1	0	1	1	0	0	0	0	1	1	+30	-150	-120
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
22	1	0	1	1	1	1	0	0	0	0	1	1	+30	-300	-270
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
25	1	1	1	1	0	0	1	1	0	0	1	1	-60	-300	-360

Table 6. Simulation results of 25-level cascade switched diode converter for different power factors.

Resistive Load			
PF (*cosφ*)	***R* (Ω)**	***V_{Amp}* (*V*)**	**THD%**
1	120	351.8	5.71
Inductive-Resistive Load			
PF (*cosφ*)	***R* (Ω)**	***L* (*mH*)**	***V_{Amp}* (*V*)**	**THD%**
0.9	108	166.5	357.2	13.07
0.8	96	229.2	364.5	16.84
0.7	84	272.8	372.9	19.27
0.6	72	305.6	375.4	19.87
0.5	60	330.8	377.3	19.32
0.4	48	350.1	378.3	19.02
0.3	36	364.4	379.4	18.89
0.2	24	374.3	381	18.67
0.1	12	380.1	381.5	18.61
Inductive Load			
PF (*cosφ*)	***L* (*mH*)**	***V_{Amp}* (*V*)**	**THD%**
0	382	380.9	18.5

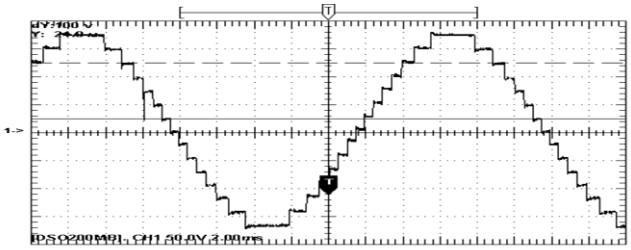


(a) Load with PF=1.

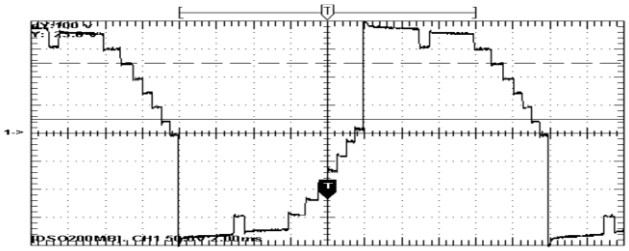


(b) Load with PF=0.2.

Fig. 8. Output voltage and FFT analysis of 15-level asymmetric switched-diode converter for different loads.

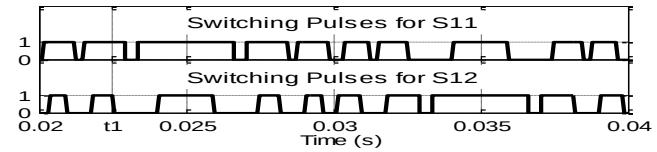


(a) Load with PF=1.

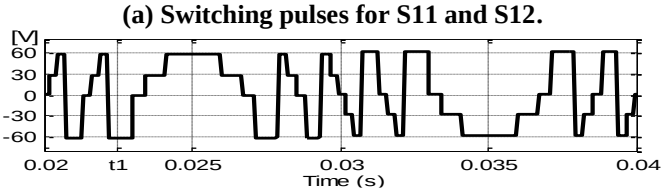


(b) Load with PF=0.2.

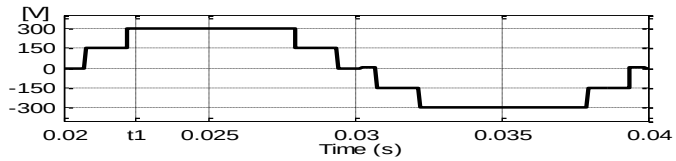
Fig. 9. Output voltage of 15-level asymmetric switched-diode converter prototype for different loads.



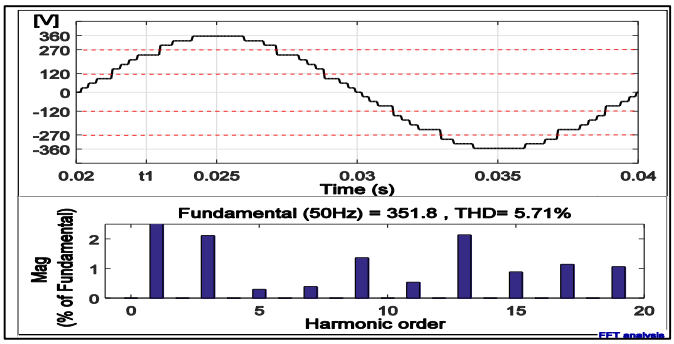
(a) Switching pulses for S11 and S12.



(b) The output voltage of first cascaded converter (V_1).



(c) The output voltage of second cascaded converter (V_2).



(d) Output voltage of 25-level cascade (V_L) converter and its FFT analysis.

Fig. 10. The simulation results of 25-level cascade switched-diode converter for load with PF=1.

Figure 11 shows the output voltage of twenty-five-level cascade topology (V_L) with its FFT analysis for an inductive-resistive load (Power Factor ≠ c). As expected, the performance of this topology gets worst in the case of resistive-inductive loads. As well as, Table 6 shows the simulation results for this twenty-five-level cascade topology for different power factors.

Figure 12 shows the experimental results of the twenty-five-level switched-diode cascade topology. The DC sources of this prototype are equal to E1=15 V and E2=75 V. The experimental results have been shown for the loads, which have the same power factor as used for the simulation of this converter topology. The experimental results evidently have great correspondences with simulations results, presented in Figs. 10 and 11. Therefore, the switched-diode cascade converter topology has not acceptable results at all. It is obvious that none of the switched-diode converter structures have stable and acceptable performance, unlike the presented results and conclusions in [11-13].

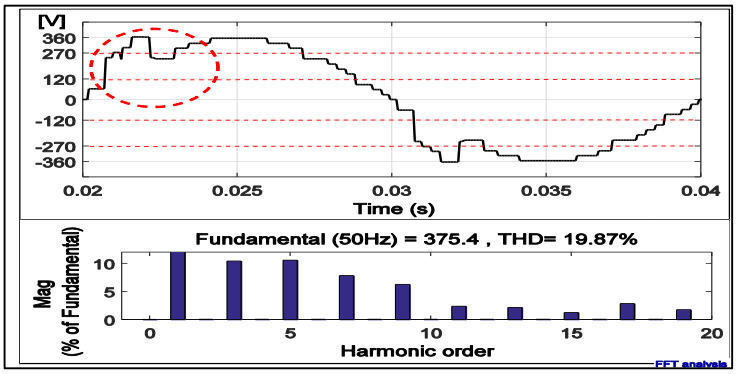
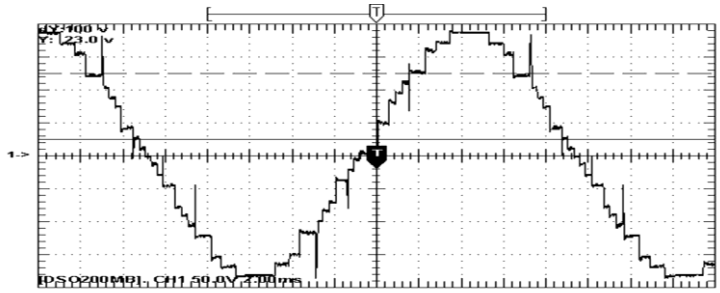
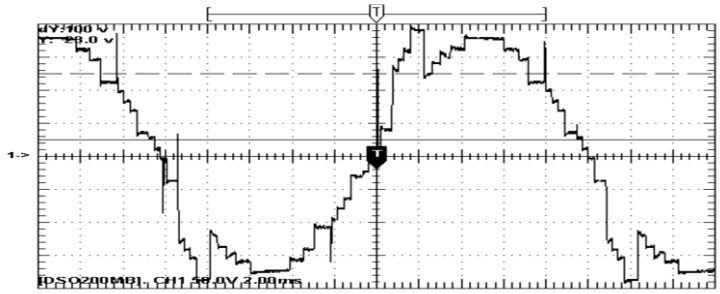


Fig. 11. The output voltage of 25-level cascade switched-diode converter (V_L) for load with PF≠1 and its FFT analysis.



(a) Load with PF=1.



(b) Load with PF≠1.

Fig. 12. Output voltage of 25-level cascaded switched-diode converter prototype for different loads.

6. Conclusions

This paper presents a precise discussion about recently introduced switched-diode sub-multilevel converter and the extended topologies based on it. The switched-diode converter includes an H-bridge converter and a basic unit. The output voltage of basic unit should be independent of the current direction, as the voltage source of the H-

bridge converter. However, it is proved in this paper that the output voltage of the basic circuit of switched-diode topology depends on the direction of its current, which is not acceptable. Because of this defect, the symmetric and asymmetric switched-diode converter topologies have unacceptable performances for loads with $PF \neq 1$. In addition, the performance of switched-diode cascade structure is unacceptable at all. As verified by the results, the cascade topology cannot generate all the desired levels of the output voltage for all kinds of load.

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