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IMPROVED SPEED LOW POWER AND LOW VOLTAGE SRAM DESIGN FOR LDPC APPLICATION CIRCUITS

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Abstract

The design of SRAM has evolved to suffice the need of the industry in terms of speed, power dissipation and other parameters. This paper proposed a SRAM design and an attempt has been made to design circuits using dynamic logic and pass transistor logic to obtain better performance in terms of speed, power dissipation and throughput. The dynamic logic would maintain voltage degradation by using the PMOS and NMOS transistor just as the CMOS logic, even though the design cell uses majority NMOS transistors. The proposed circuits are simulated using BSIM for different CMOS feature sizes of 70 nm, 90 nm, 120 nm and 180 nm. The results obtained have been analysed and shows that the proposed circuit of 8T performs much better as compared to other circuit configurations. There is significant improvement in power dissipation by 99.64 %, delay by 99.9 %, throughput of 490 Mbps and power delay product of 99.96 %.

Keywords: Improved speed, Dynamic logic, SRAM, LDPC, Throughput, Power dissipation.

1. Introduction

Very-large-scale integration or VLSI design has been researched in different areas but low power operation has become one of the parameters of prime importance. Power reduction has become essential due to the use of new technology in designing integrated circuit chips. In order to achieve low power, various methods have been researched and tested. One of the vital criteria in the design of IC is to lower the power of memory circuits having the least possible trade off on its performance [1]. Current trends have made it essential for the VLSI industry to constantly endeavour to achieve high density, high speed and low power devices in CMOS technology. The scaling in CMOS technology involves the SRAM memory

Nomenclatures

BL	Bit line
C_{out}	Output capacitance
I_{DD}	Supply current
Q	Charge across capacitance
t	Time, secs
V_{DD}	Supply voltage, V
V_{IH}	Intermediate high voltage, V
V_{out}	Output voltage, V
V_T	Threshold voltage, V
WL	Word line

Abbreviations

CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
GND	Ground
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide semiconductor
SRAM	Static Random Access Memory
VLSI	Static Random Access Memory
VTC	Very-large-scale integration

design. The SRAM design faces the challenges of faster performance and low power consumption. The SRAM accounts for a considerable portion of power consumption and the high density of the design necessitates a reduction in power [2].The SRAM uses a memory cell with internal feedback that retains its value as long as power is applied. The power consumption of SRAM varies widely depending on how frequently it is accessed. When it is used at a slower pace it draws very little power and when in idle condition, the power drawn is negligible. SRAMs are used mostly as cache memory, as buffers in routers and as storage for printers too. SRAMs are expensive and less dense as compared to DRAMs, but have the advantage of low power when designed using CMOS technology.

In this paper the design approach looks to achieve a better performance in terms of power dissipation, propagation delay and efficiency using various circuit design configurations such as 8T, 11T, 13T and ZA. A modified SRAM cell is proposed to be implemented for LDPC decoders. The proposed SRAM design is compared with other SRAM cell designs. The proposed SRAM is designed using DSCH2 for the logic design, layouts are generated using Microwind3 and parametric analysis is done using BSIM 4 analyser. A simulation of the proposed circuit has been conducted and the results obtained have been compared with other published results. A parametric analysis has been done to evaluate the design for parameters such as rise time, fall time, Output voltage and power dissipation. The simulation results of the proposed design show an enhanced performance in terms of propagation delay, power dissipation and efficiency.

2. Related Work

Many researchers have strived to obtain substantial power savings. Singh et al. [3] have made a comparative study of various SRAM cell structures. They analysed

the parameters such as power dissipation, output voltage, chip layout area and power efficiency. The simulation results reveal the 10T SRAM cell performs best for the range of power consumption, operating frequency and temperature. Sriram et al. [4] designed a low power 64 bit SRAM using 13T cell. Simulations were performed at 180 nm and obtained a power dissipation of 4.513 mW. Ming et al. [5] showed that a SRAM using 180 nm technology and 11T circuit obtained a leakage power of 42 nW and a dynamic power of 200 nW. Rahman and Singh [6] proposed an 8T circuit that improves cell stability and reduces power consumption. Khayatzadeh et al. [7] proposed a zero-awareness asymmetric (ZA) cell which reduces the power dissipated during writing drastically. Weste and Harris [8] stated that the size of the cell increased but was more power efficient.

Upadhyay et al. [9] showed that an 8T SRAM circuit design improved the power consumption. They also showed that the proposed circuit improved cell stability by increasing the Read static noise margin. Pal and Islam [10] showed that the due to stacking effect low power dissipation was achieved. Joshi et al. [11] presented a novel half select disturb free transistor SRAM cell which is 6T based and uses decoupling logic. They focussed on 90 nm and used read assist architecture. This enhanced the overall array low voltage operability and reduced the power consumption. The performance and speed was seen to be comparable with the normal 6T design. Ramakrishnan and Harirajkumar [12] added an extra word line to change the random access memory to read only memory so that the speed of the processor could be improved. Their proposed circuit helped to overcome mismatches in access transistor between neighbouring transistors and also reduced the area spacing in internal memory of SRAM.

Moradi et al. [13] presented in their paper a stable differential SRAM cell that consumes low power. The design had additional two buffer transistors along with the conventional 6T and one tail transistor and one complementary word line. The design saw a reduction in read/write power consumption and a narrower spread in hold power too. Anandraj and Jagadale [14] stated that in many mission - critical embedded systems the power consumption is mainly due to memory access.

3. Design Method

According to related works, the design methods are a trade off with all issues in the existing circuits. The author here has analysed various design methods for the trade-off of the above-mentioned issues. The appropriate techniques have been identified and implemented in the designed circuits.

3.1. Dynamic logic design:

The circuit is designed using the dynamic CMOS logic technique. This design technique reduces the number of transistors than other CMOS techniques, since the function transistors are using pass transistor logic and pre-charges the PMOS and NMOS transistors that are used for the implementation of a logic function. This method also known as the 'pre-charge – evaluate' logic works such that the output capacitance at the node is first pre-charged and evaluation of the circuit is based on the applied inputs. In every dynamic stage, a clock signal is used to drive the NMOS-PMOS transistor pairs. When the clock signal is low, the PMOS pre-charge transistor starts to conduct while the complementary NMOS transistor is off [15]. The output capacitor is charged up through the conducting PMOS

transistor to a logic high level of $V_{out} = V_{DD}$. During pre-conditioning of the node, which is the pre-charge state, the sole purpose of the interval is to add the charge given by $Q = C_{out}V_{DD}$ to the output node [16]. The input voltages at this stage have no effect on the output as one of the transistors is turned off. When the clock signal becomes high, the pre-charge transistor turns off and the other transistor which is the complementary one is turned on. The output node voltage now changes either high or low depending on the input voltage levels. If the input signals create a path to conduct between the output node and the ground, then the output capacitance will start to discharge to 0 levels.

Dynamic CMOS has been often used for high speed circuits because parasitic capacitance can be made small due to unique connection configuration of MOSFETs inside a logic gate, although good layout is not easy. Dynamic circuits have low input capacitance and no contention during switching. They also have zero static power dissipation. Dynamic CMOS may consume power by repeating pre-charging. They require careful clocking, consume significant dynamic power and are sensitive to noise during evaluation.

The proposed dynamic SRAM circuits are designed by dynamic logic, which are shown in Figs. 1(a) to 1(d). The proposed circuit operation and its working principles are explained in detail in the forthcoming paragraphs. The initial focus of this work was the design of SRAM cell using dynamic logic. An NMOS pass transistor that drives the gate of another NMOS transistor constitutes a basic NMOS dynamic logic circuit [17]. The pass transistor is driven by a periodic clock signal to either charge up or charge down the capacitance depending on the input to the circuit. Hence the concept of logic '0' when the clock is low (0) or discharge of the capacitance and logic '1' when the clock is high (1) or when the capacitance is charged up. The inverter will show an output logic 1 or logic 0 value based on the voltage at the capacitance.

3.2. Logic '1' transfer:

If the voltage at the node is assumed to be 0 initially, and logic 1 level is applied to the input terminal. The clock signal at the gate will now increase from 0 to V_{DD} at $t = 0$. Now the pass transistor will start to conduct as soon as the clock becomes active. The pass transistor will work in the saturation state and charges up the capacitor. The pass transistor will turn off when the voltage at the node equals the maximum voltage and the gate source voltage will be equal to threshold voltage.

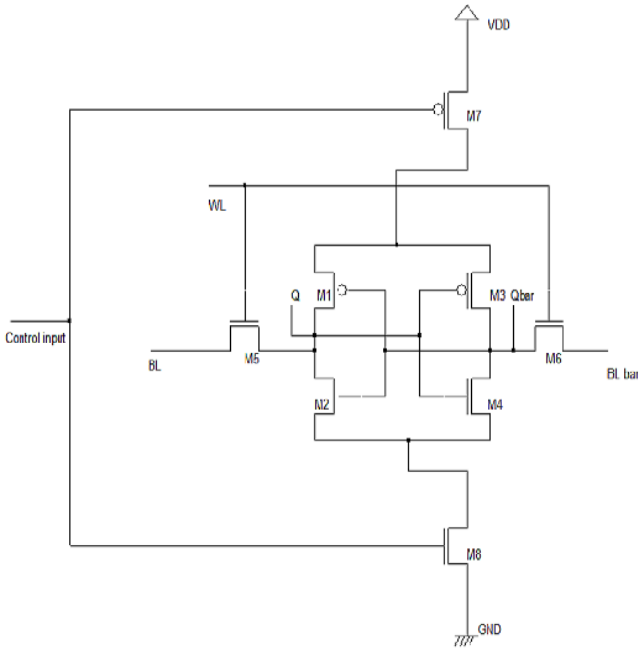
3.3. Logic '0' transfer:

If it is assumed that the voltage at the node is 1 initially and logic 0 is applied at the input terminal. The clock signal at the gate of the pass transistor changes from 0 to V_{DD} [16]. The pass transistor starts to conduct as soon as the clock signal becomes active and the current flows in the opposing direction of as during charge up of the capacitor. The pass transistor operating in the linear region discharges the capacitor and the source voltage now becomes 0.

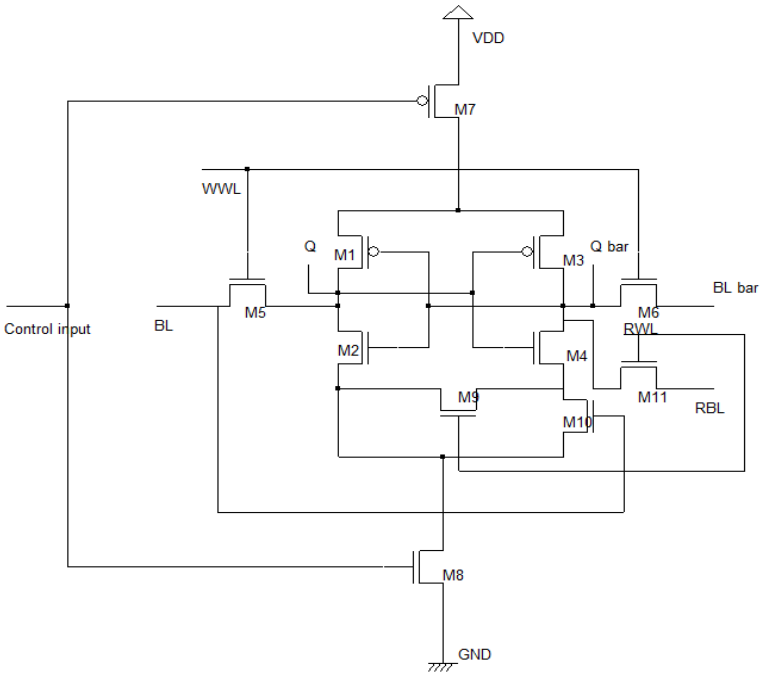
The proposed design uses a 70 nm, 90 nm, 120 nm and 180 nm technology sizes for 8T, 11T, 13T and ZA circuits using the logic '0' and logic '1' transition for inputs of *WL*= 1 and the *BL* input as '0' and '1'. The circuits below show the basic setup for the simulation. Using the dynamic logic technique along with pass

transistor logic, the 8T, 11T, 13T and ZA circuits are designed and shown in Figs. 1(a) to 1(d) respectively. The operation of the circuit is divided by the control input into two distinct phases that are the pre-charge and evaluate intervals. A condition of '0' at the control input defines the pre-charge where the PMOS is conducting while the NMOS is cut off. The circuit is designed using the domino logic wherein the input is not required to be inverted to be used in the design which leads to lower power consumption [18, 19].

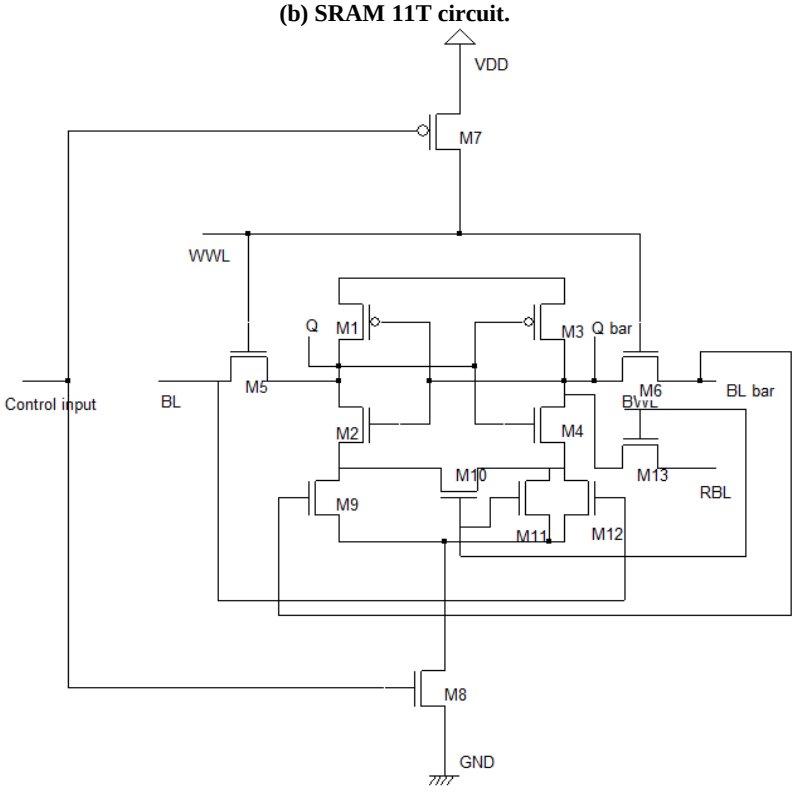
The diagrams in Fig.1, the circuit for a standard 6T circuit has been improved with the addition of two more transistors making it an 8T and similarly for the 9T, 11T and ZA making it 11T, 13T and ZA. The additional transistors are added to provide a control of the circuit operation for logic '0' and logic '1'. This is achieved by connecting the two transistors between the source voltage V_{DD} and the ground GND points [16]. The common point is used as a control input. It has three main inputs word line (*WL*), bit line (*BL*) and control input (*CI*). The *BL* has logic '1' and a logic '0' input which is applied as *BL* and $\overline{BL}$ respectively. The *WL* and *BL* inputs follow the Boolean identities. According to NMOS and PMOS operation the circuit stores or writes into the logic. During operation of the circuit, the control input is initially made '0'. When *WL*=0 and *BL*=0, transistor *M5* is inactive due to NMOS operation and *M3* and *M1* are active but there is no output due to pull down effect which brings the voltage down nearly equal to zero [18]. So the outputs *Q* and $\bar{Q}$ are logically low. A similar simulation is done with the control input made logic '1'. When the control input is made 1 and *WL*=1 and *BL*=0, which refers to the bit line being zero. During simulation it is seen that even though the control input is high and *WL*=1, the node capacitance of the transistor *M5* is not charged up as *BL*=0. Therefore, the output is seen as *Q*=0. When control input is 1 and *WL*=1 and *BL*=1, then the pass transistors charge up as current flows and the output reads a value 1 that is *Q*=1 and $\bar{Q}$= 0.



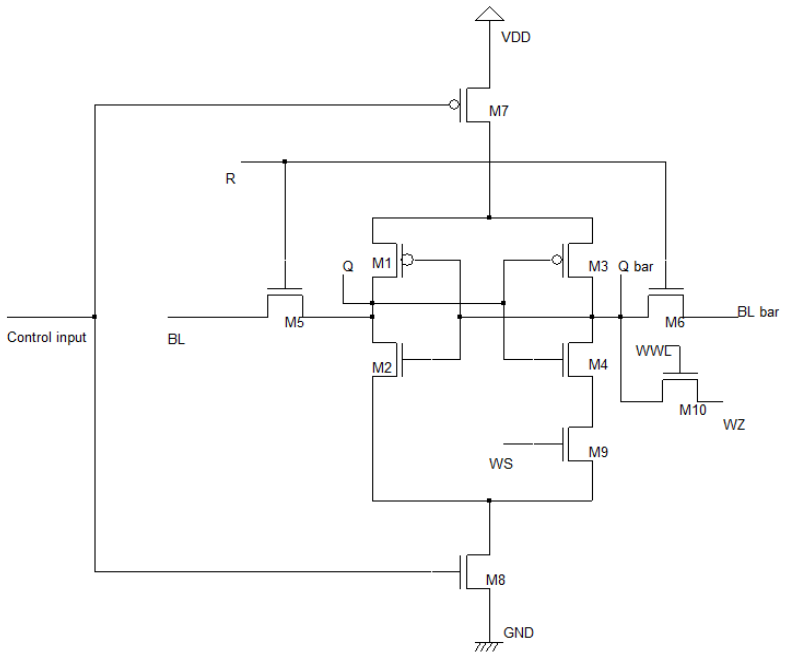
(a) SRAM 8T circuit.



(b) SRAM 11T circuit.



(c) SRAM 13T circuit.



(d) SRAM ZA circuit.

Fig. 1. Proposed circuits of SRAM 8T, 11T, 13T and ZA configurations.

4. Results and Discussion

The proposed SRAM cell has been designed using dynamic logic due to which the intended achievement of low power dissipation, improved speed and better throughput is obtained. The proposed circuit uses lower number of transistors for WRITE and READ bit logic function which means it can store higher evaluation cycles in memory circuits.

The SRAM circuit is simulated using various technologies namely 70 nm, 90 nm, 120 nm and 180 nm with cell structures of 8T, 11T, 13T and ZA using dynamic logic. The parameters that can be observed are power output, propagation delay, efficiency, latency and throughput. Due to dynamic logic design the author expects lower power dissipation, improved efficiency, smaller delay and better throughput These SRAM circuits designed using dynamic logic gives good performance in logic '0' and logic '1' drivability. Increase in the number of transistors in SRAM cells technically gives better performance in terms of pre-charge and evaluation cycle in memory circuits. This circuit is designed using dynamic logic that can achieve $V_{DD} - V_T$ losses in NMOS transistor so the output logic stored data and READ/WRITE data are in the retained form.

The proposed SRAM cells are imposed in various parameter simulations such as power dissipation calculation, delay measurements, area, latency and throughput. The parameters of Voltage Vs Power simulation for the various circuits have been compared using different technologies. In the layout aspect the

memory cell's charging and discharging has been validated by the aspect ratio factor which can be expressed with scaling methods of current technology.

The scaling method of the node increases the power-density as expected. The design method of CMOS technology beyond 70 nm node represents a real challenge for any sort of voltage and frequency scaling starting from 120 nm node, which is a new process and has inherently higher dynamic and leakage current density with minimal improvement in speed. The design method of CMOS with feature size between 180 nm to 70 nm has seen the dynamic power dissipation to be almost the same. Based on dynamic power dissipation, the values are analysed by the following graphs given in Figs. 2(a) to 2(d).

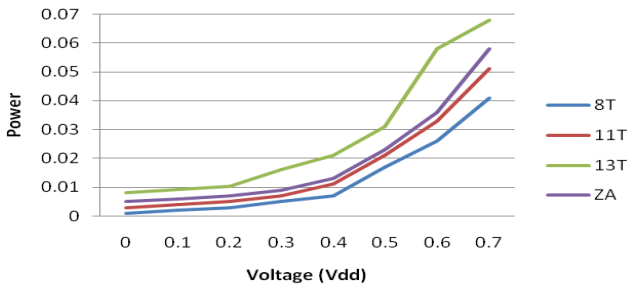
As per MOSFET operation technique, the supply voltage creates (bias) voltage drop across the layouts. The layout capacitance stores the energy during charge up and discharges the energy during evaluation time. The summation of all layout capacitances is called load capacitance at the output terminals. The power dissipation is normally proportional to load capacitance and charges when supply voltage (V_{DD}) and operating frequency are constant. In particular, for our analysis, the supply voltages are varied and its outcome depends on the applied input voltage. The power remains constant until the intermediate voltage (V_{IH}) exponentially changes the power due to input voltage across the intermediate region and the output regions as illustrated in the graphs.

Low cost always continues to drive higher levels of integration; whereas low cost technological breakthroughs which help to keep power under control are getting very scarce. The power dissipation of SRAM circuit could be calculated by logic transitions causing the designed cell of the charge/discharge load capacitance. The designed dynamic logic has a P-transistor as a pull up transistor and N-transistor as a pull down transistor that are momentarily shorted as logic gate changes state resulting in short circuit power dissipation.

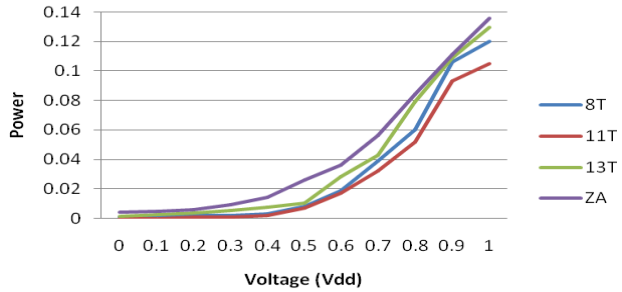
The other way of power dissipation occurs, when the system cells are in standby mode or are not powered. There are many sources of leakage current in MOSFET such as, diode leakages around transistors and n-wells, Sub threshold Leakage, Gate Leakage, Tunnel Currents etc. As per dynamic design techniques, the SRAM cells are given low leakage current in terms of standard 6T designed transistors and the added technique related transistors. Dynamic power varies as V^2_{DD} that can be minimized by dynamic logic. So reducing the supply voltage reduces power dissipation. According to Figs. 2(a) to 2(d), our proposed SRAM 8T dynamic based design circuit gives less power dissipation than other designed circuits that are clearly shown in Figs. 2(a) to 2(d) due to the circuit having a low critical path and equally sharing charges among themselves.

The graphs in Fig. 2 depict that as the voltage increases there is a slow increase in the power that is dissipated. A significant change as compared to other circuits is seen in the 13 T circuit simulations. A lower power dissipation of within 0.2 µW is observed for all technologies using the 180 nm technology except the 13T due to overlapping of logic transitions.

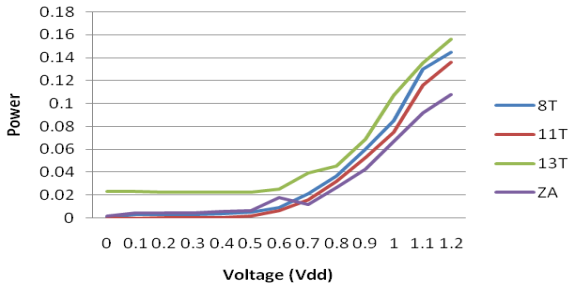
The parameters of Voltage vs. Final voltage simulation for the various circuits have been compared using different technologies as shown in Figs. 3(a) to 3(d).



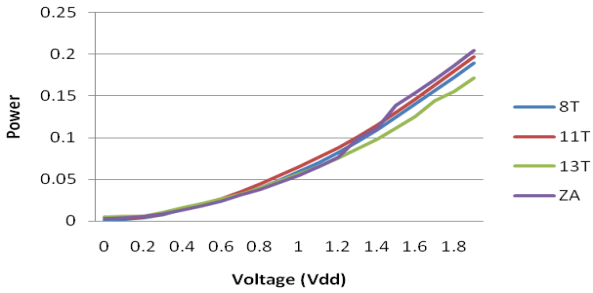
(a) Voltage (Vdd) vs. power 70 nm.



(b) Voltage (Vdd) vs. power 90 nm.



(c) Voltage (Vdd) vs. power 120 nm.



(d) Voltage (Vdd) vs. power 180 nm.

Fig. 2. SRAM VTC characteristics for various feature sizes.

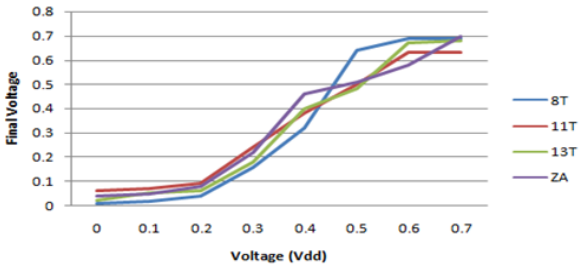


Fig. 3.(a) Voltage (Vdd) vs. final voltage 70 nm.

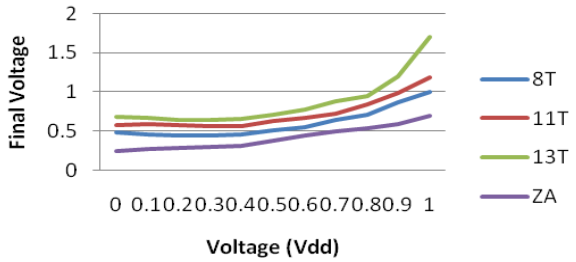


Fig. 3.(b) Voltage (Vdd) vs. final voltage 90 nm.

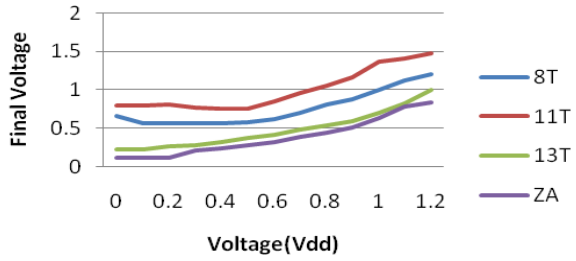


Fig. 3.(c) Voltage (Vdd) vs. final voltage 120 nm.

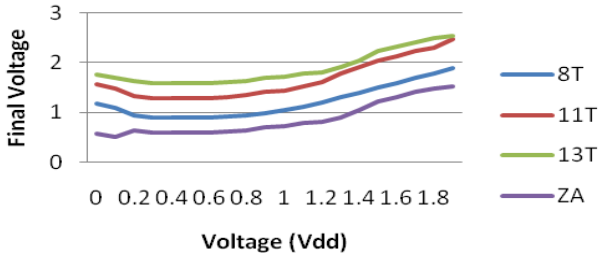


Fig. 3.(d) Voltage (Vdd) vs. final voltage 180 nm.

Fig. 3. The variation of voltage V_{dd} with the final voltage for different feature sizes.

It can be observed from the above diagrams that the performance of final voltage for a cell structure of 8T follows a steady increase and reaches a value of 0.7 V. The final voltage increases to higher values of 1V, 2 V and 1.2 V for 90 nm, 180 nm and 120 nm respectively due to the increase in area. It can also be observed that the performance of the 11T structure is better compared to the 8T. The *W/L* of each feature size shrinks based on the aspect ratio. The Microwind 2 software is vertical based that is, the width is made constant and the length is varied with gate length of feature size. The layout analysis of the proposed SRAM circuit is carried out for the entire circuit including the connecting wires and the input and output pad. The circuits are exposed to parametric analysis in terms of input voltage and output final voltage and examined for the VTC characteristics.

According to design methodology, the 8T based SRAM cell varies the voltage linearly than other SRAM cells. The 8T cell is designed to be a balanced circuit using the *BL* and $\overline{BL}$ inputs. The connecting NMOS tree structure conducts the charges quickly but the power dissipation and delay are increased due to NMOS drivability given by V_{DD} - V_T. The above mentioned errors can be traded off by using dynamic logic design method. The reason for the proposed 8T SRAM cell to better perform is the equally connected logical effort which reduces the critical path.

4.1. Parametric Analysis:

The parametric analysis for the proposed 8T, 11T, 13T and ZA SRAM circuits was conducted using the Microwind 3 simulation tool. Based on the data obtained during simulation the circuit has been analysed. For the 8T SRAM circuit, the *WL* was maintained at high (*WL* = 1) and the *BL* and $\overline{BL}$ inputs were given the values of 0 and 1 (*BL* = 0, $\overline{BL}$= 1 and *BL* = 1, $\overline{BL}$= 0). The input conditions were controlled by the periodic clock signal given the values of logic '0' and logic '1'. During logic '0' condition and with *WL* =1, *BL* = 0, $\overline{BL}$= 1, the output pass transistor is turned off, the node voltage is zero since the bit line is reading a zero. Hence no current flows and the voltage across the capacitance starts to drop. The output will record a zero, *Q* = 0. When *WL*=1, *BL*=1 and $\overline{BL}$= 0, the pass transistors charge up the node capacitance and the output reads a 1 (*Q* =1) due to the influx of charges and the output voltage increases. For the logic '1' condition and with *WL* = 1, *BL*= 0 and $\overline{BL}$=1, the output is still at *Q* = 0 as the bit line is not activated. When *BL* = 1 then the output voltage reaches a high and *Q* = 1.

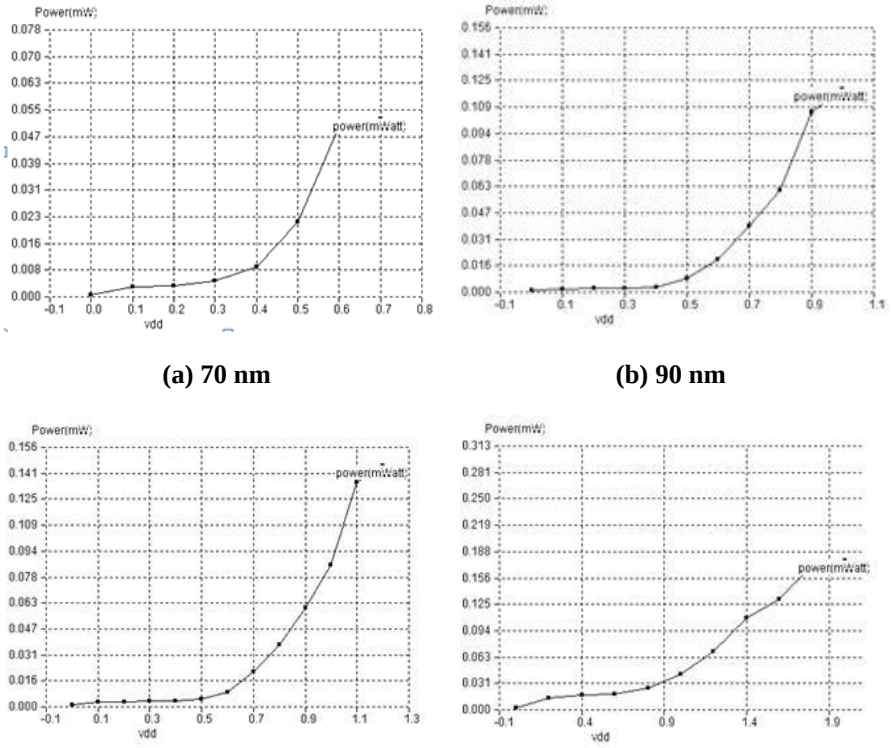
The proposed SRAM 8T circuit parameters are analysed by advance BSIM4 analyser. The layouts are imposed with a range of voltage variations of supply voltage (V_{DD}). There are many parameters that can be analysed using different methods such as capacitance, voltage, temperature and Monte Carlo. Here the SRAM cell was simulated and analysed using the voltage method for a variation of supply voltage V_{DD} [19]. The supply voltage is varied in terms of unit voltage and analysed the power dissipation. The analysis has been carried out for 70 nm, 90 nm, 120 nm and 180 nm technologies and the simulated results directly taken from CAD tool and shown in Figs. 4(a) to 4(d).

The SRAM 8T transistor is related to storing the charges as bit logic and discharging the charges as word logic. According to VTC characteristics, the transition of output voltages into other voltages is described by VOL, VIL, VIH and VOH. Hence the SRAM cells changes the charges from lower input to high outputs. Based on dynamic logic the 8T SRAM cell gives better final output

voltage transition in select feature size such as 70 nm, 90 nm, 120 nm and 180 nm are directly taken from CAD tool and shown in Figs. 5(a) to 5(d).

According to layout simulation, the SRAM 8T circuit gives less power dissipation than 11T, (50.8 %), 13T (89.05 %), and ZA (52 %) SRAM circuits due to the equal charge sharing among bit line and word line cells, which are shown in Table 1. The equal tree structure design method gives an increased V_o. There is no longer a negligible value of gate voltage which makes it inaccurate. Conversely, the potential of the channel at the grounded source is zero, while at the output it is maximum due to the saturation mode of the output transistor. Hence the power dissipation of the transistor is low compared to other designs.

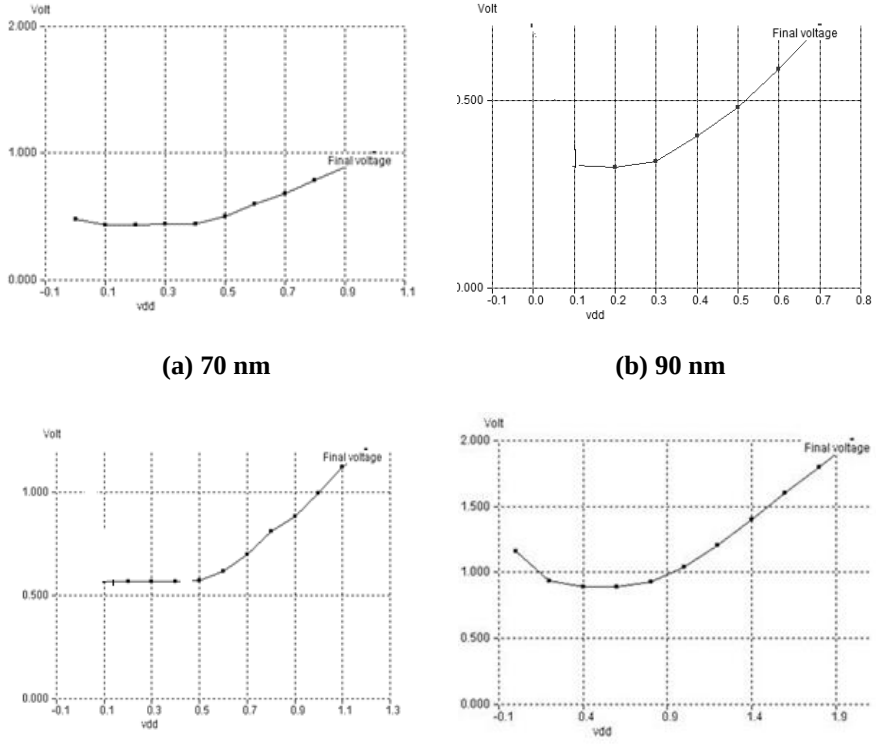
According to Table 1, the delay measurements made for the 8T SRAM circuit are compared using a feature size of 70 nm with 11T, 13T and ZA SRAM circuits. The proposed 8T SRAM cell gives an improvement in terms delay for the 11T circuit by 64.32 %, 13T by 60.5 % and ZA by 96.23 %. This improvement in delay is due to the equal time required to charge and discharge the potential as seen during rise and fall time periods. This is because the transistor is in the saturation mode.



(a) 70 nm **(b) 90 nm**

(c) 120 nm **(d) 180 nm**

Fig. 4. SRAM simulated results for 8T circuit voltage vs. power dissipation



(a) 70 nm **(b) 90 nm**

(c) 120 nm **(d) 180 nm**

Fig. 4. SRAM simulated results for 8T circuit voltage vs. power dissipation

Figs. 5. SRAM simulated results for 8T circuit voltage vs. final voltage.

Table 1. Simulation results of SRAM cell.

Feature size	Cell structure	Power Dissipation (μW)	Delay (s) $\times 10^{-12}$	PDP (W/s)	Area μm^2	Efficiency (%)	Latency ($\times 10^{-9}$)	Throughput Mbps
70 nm	8T	0.876	37.2	1.462×10^{-15}	112	62.83	2.087	490
	11T	1.781	104	4.087×10^{-15}	136	74.04	2.104	475
	13T	8	9.42	1.563×10^{-12}	160	76.29	2.942	339
	ZA	1.825	984	1.988×10^{-14}	152	75.17	2.984	335
90 nm	8T	1.106	45	1.215×10^{-16}	216	76.5	4.045	247.22
	11T	30.7	9	2.763×10^{-16}	264	78.5	4.009	249.44
	13T	0.6	1129	6.774×10^{-16}	300	78.5	7.129	140.27
	ZA	2.7	5	5.53×10^{-18}	252	76.5	12	83.33
120 nm	8T	0.387	190	1.664×10^{-16}	180	77	4.19	238.66
	11T	2.062	567	1.169×10^{-15}	220	76.5	4.567	218.92
	13T	20	945	18.9×10^{-15}	240	77	6.945	143.98
	ZA	0.949	7	6.643×10^{-18}	210	76	8.007	124.89
180 nm	8T	2	49	9.8×10^{-14}	621	76.96	4.049	246.97
	11T	2	23	4.6×10^{-14}	828	76.96	4.023	248.57
	13T	11	1379	1.517×10^{-14}	966	77.75	7.379	135.52
	ZA	11.85	36	6.534×10^{-14}	759	76.96	13.036	76.71

The power efficiency calculated shows a value of 62.83 % for the 8T circuit while for the other circuits it is 74.04 % for 11T, 76.29 % for 13T and 75.17 % for ZA circuits. Power efficiency depends on aspect ratio of the MOSFET. This ratio gives a trans-conductance parameter (*K*) whose value depends on the size of the layout. In line with the design aspects of 8T SRAM circuit, the output drain current which flows between the source and drain terminals leads the output currents. When the output voltage is equal to V_{DD} and the current flow is almost equal to the input current, then the efficiency of the power is higher than other designed SRAM cells. In the case of throughput calculations, the improvement of 8T circuit is 3.06 % for 11T, 30.08 % for 13T and 31.63 % for ZA circuits. Throughput depends upon reduction of many factors namely, power supply, voltage swing in all nodes, transition factor and load capacitance. As determined by the 8T SRAM design, the nodes are all equal in all aspects hence switching power reduces and there is no effect of load capacitance. This gives a better throughput to the proposed 8T SRAM circuit compared to other designs.

4.2. Comparison of Results:

In comparison of results Table 2, our proposed SRAM circuit (8T) is compared with other existing references and SRAM cell configuration such as 11T, 13T and ZA in terms of power dissipation, propagation delay, Latency and Throughput. Our proposed SRAM circuit when compared with Ref 5 gives better power dissipation by 99% at 180 nm technology. The propagation delay is smaller than the results obtained by Ref 7 which was measured at 0.13µm. The delay was improved by 99.9% than CMOS at 0.13µm. The latency calculated for the proposed circuit was the best at 8T cell structure as compared to the others having values of a minimum of 2.08×10^{-9}at 70 nm and a maximum of 4.049×10^{-9} at 180 nm. The throughput obtained for 70 nm was 490×10^{6} bps and for the rest showed a similar range. The power delay product PDP of the proposed circuit showed an improvement 99.9% compared to Ref 3.

Table 2. Comparative results using 8T circuit configuration.

	F. size (nm)	Delay $\times 10^{-12}$ (s)	%	P.E (%)	Power dissipation $\times 10^{-6}$ (W)	%	Latency $\times 10^{-9}$ (s)	Throughput $\times 10^{6}$ (bps)	PDP $\times 10^{-15}$ (W/s)	%
P. Circuit	70	37.2	-	62.8	1.825	-	2.08	490	0.0678	-
	90	190	-	77	1.387	-	4.19	238	0.1664	-
	120	45		76.5	2.7	-	4.04	247	0.1215	-
	180	49		76.9	2	-	4.05	246	-	-
Ming et al. [5]	180	-	-	-	561.89	99.64	-	-	-	-
Khayat-zadeh et al. [7]	130	166.6	99		0.756	-257.1				
Singh et al.[3]	90	-	-	-	-	-	-	-	503	99.9

%=% of achievement, P. =Proposed, P.E=Power Efficiency

5. Conclusion

The proposed SRAM 8T, 11T, 13T and ZA circuits are designed using dynamic logic which reduces the number of transistors in the designed cell and gives the output parameters comparable to CMOS technique. Our proposed 8T SRAM cell gives better performance than other designed circuits due to the inherent characteristics of a regular tree structure which has been used in the design and taken as a standard during analysis. The proposed circuits have been simulated

and tested for various technologies using the 8T cell structure. This design involved the 8T cell structure using domino logic at 70 nm, 90 nm, 120 nm and 180 nm. The various simulations have been carried out and showed better performance than other existing circuits. The analysis revealed an improvement from other existing circuits in terms of power dissipation, propagation delay, propagation delay product, power efficiency and throughput. The designed circuits may be used in low power consumption and high speed memory application circuits since charge sharing and storage of charges equate out the output power loss.

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