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ALL-MOS HIGH PRECISION AND WIDE BANDWIDTH ANALOGUE MULTIPLIER CIRCUIT

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Abstract

A new four-quadrant analogue multiplier circuit is presented in this paper, which is designed in the voltage mode. The key feature of the circuit is the high-precision operation as well as its linear performance due to the symmetrical configuration. Compared to the recent works, the precision of the circuit, as well as the linearity performance, is improved. The performance of the circuit, in terms of the conceivable mismatches in threshold voltage and trans-conductance parameters, are analyzed in detail. In order to prove the efficiency of the proposed circuit, it is utilized in a modulator structure and then the simulation results of the design are adopted with the best possible performance of that application. The designed circuit is simulated via HSPICE software with TSMC level 49 (BSIM3v3) parameters in 0.18 μm CMOS technology, where the supply voltage is 1.8 V, the -3 dB bandwidth of the circuit is obtained 1.45 GHz and the total harmonic distortion at 1 MHz, remains as low as 0.4%.

Keywords: Four-quadrant, High precision, Multiplier circuit, Wide bandwidth.

1. Introduction

The analogue multilier is a main building block for various applications such as phase locked loops, automatic gain controlling, modulators, adaptive filters, image processing and fuzzy based systems. As explained by Naderi et al. [1] and Menekay [2], different methods in CMOS technology already exist in the literature, in either current-mode or voltage-mode [3-5]. The linearity and power consumption are the main factors emphasized in most of the previous works, while some of them suffer from low bandwidth [1-4].

The trans-linear method is the most desirable method, which employs loop transistors that operate either in sub-threshold [6-8] or saturation regions [9-12]. Although this approach causes low power consumption in the sub-threshold region, but the operation range of the designed circuits is too narrow and their speed is low. Based on studies by Alikhani and Ahmad [10], on the contrary, the trans-linear based circuits in the saturation region, have better operation range, higher bandwidth and slightly lower distortion, thus these circuits are more popular compared to the circuits, which operate in the sub-threshold region.

Another key element of the multiplier circuits is the low distortion performance, a serious problem in some related works [2, 4-7]. As reported by Lopez-Martin et al. [13], Siripruchyanun and Jaikla [14] and Roy et al. [15], in addition, multipliers require two supply voltage, which is not preferable for integrated and compact circuit design.

Linearity error in some of the presented multipliers affects the performance of the circuit in term of the accuracy [16-19]. This drawback originates from the inherent behaviour of CMOS transistors, which include body effect [16], channel length modulation [17] and mobility reduction issues [18]. Therefore, for designing high precision multiplier circuit, the linearity error should be minimized. One method to minimize these errors is the usage of symmetrical configuration in order to achieve highly precision performance.

Another important characteristic of the multiplier circuit is the operational capability in four-quadrant, which is useful in different applications [19, 20]. Several proposed multiplier circuits operate in one [2], two [21] and some others work in four quadrants [22, 23].

The objective of this paper is the designing and implementation of a novel single supply voltage multiplier circuit, which operates in four-quadrant. The key feature of the circuit is the high-precision operation as well as its linear performance due to the symmetrical configuration.

The paper is arranged in five parts: The designed circuit is presented in Section 2, followed by the performance analysis in Section 3. In Section 4, HSPICE results of the circuit are demonstrated to verify the efficiency of the circuit. The comparison table is included in this section. Finally, the paper is concluded in Section 5.

2. Proposed Analogue Multiplier

The multiplier circuit explains the multiplication of two signals such as a and b, which leads to the output of $z = Cab$, where C is commonly a constant less-dimension value. One possible technique to design a multiplier circuit is to utilize the square-difference algebraic of $(a+b)^2 - (a-b)^2 = 4ab$. In order to implement this equation, two squaring

circuits should be designed and then their outputs need to be subtracted. Based on this identity, the proposed four-quadrant analogue multiplier is shown in Fig. 1. The circuit is designed in a symmetrical configuration, which compensates the conceivable non-idealities performance of the overall circuit.

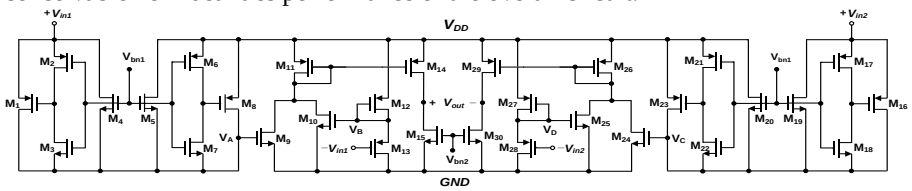

Fig. 1. The proposed four-quadrant analogue multiplier circuit.

Let us consider the left half side of the circuit; the transistors M_1-M_4 provide a Voltage Controlled Resistor (VCR), which its value can be controlled via V_{bn1}. The total current of VCR is dominated by I_{D1} or I_{D4} as follows:

Suppose that $V_{bn1}<V_{T4}$, in this case, M_4 is off and since M_2 and M_3 form an inverter, the drain voltage of M_3 starts transition; therefore, M_1 goes to triode region, which in turn linearly changes the VCR current via V_{in1}. For the case that $V_{bn1}>V_{T4}$, M_4 operates in the triode region and I_{D4} constructs the resistor current. If V_{bn1} increases more, M_4 goes to the saturation region and I_{D4} decreases, while I_{D1} and I_{D3} increase due to the increasing of V_{DS4}. Consequently, the nonlinearity caused by I_{D4} is effectively compensated via M_1 and M_3, the linear characteristic of VCR will be satisfied. Consider the second VCR consists of transistors M_5-M_8, which are connected to the first VCR and V_{DD}. One can find the voltage of V_A as $(V_{DD}+V_{in1})/2$, which is employed to turn transistor M_9 on. The transistors M_{12} and M_{13} are biased in the saturation region and their currents are equal ($I_{D12}= I_{D13}$). Therefore their relationship can be written as:

$$K_{12}(V_{DD} - V_B - |V_{TP}|)^2 = K_{13}(V_B + V_{in1} - |V_{TP}|)^2 \quad (1)$$

The voltage of V_B is derived after few mathematical manipulations as $(V_{DD}-V_{in1})/2$. This voltage is also caused to operate transistor M_{10} in the saturation region. Summation of currents I_{D9} and I_{D10} flow to transistor M_{11} and then is mirrored to transistor M_{14} in which, its drain current can be written as:

$$I_{D14} = K_{9,10}\{[0.5(V_{DD} + V_{in1}) - V_{TN}]^2 + [0.5(V_{DD} - V_{in1}) - V_{TN}]^2\} \quad (2)$$

Simplifying above equation yields:

$$I_{D14} = 2K_{9,10}\left[\left(\frac{V_{DD}}{2} - V_{TN}\right)^2 + \left(\frac{V_{in1}}{2}\right)^2\right] \quad (3)$$

The same calculation can be done on the right side of the figure to derive I_{D29}. Since transistors M_{15} and M_{30} are biased in the triode region and have the equal value of the resistor ($R_{M15}= R_{M30} = R$), currents of I_{D14} and I_{D29} are converted to the voltage at the differential node of V_{out}. Therefore, the output of the circuit is obtained as:

$$V_{out} = R_{M15}I_{D14} - R_{M30}I_{D29} = 0.5RK_{14,29}\left({V_{in1}}^2 - {V_{in2}}^2\right) \quad (4)$$

Considering V_X and V_Y as the input signals, by applying $V_{in1}=V_X+V_Y$ and $V_{in2}=V_X-V_Y$ the output voltage with respect to the input voltages is expressed as:

$$V_{out} = 2RK_{14,29}(V_X V_Y) \quad (5)$$

It is seen that Eq. (5) explains the multiplication of two signals of V_X and V_Y and the constant parameters of linear resistance and transistor trans-conductance.

3. Performance Analysis

The derivation of output voltage was designed based on the assumption that all of the transistors are well matched. In order to examine the mismatch effect in the output of the circuit, two mismatched parameters are discussed: threshold voltage and transconductance of the devices. If we define the mismatch of the trans-conductance as Δk and then K_i-K_j=Δk, the error value at the circuit output with ignoring the term of Δk^2 is derived as follows:

$$V'_{error} = \left[\frac{R(V_X-V_Y)^2(K_{12,13}a+0.5\Delta kV_{DD})}{a+0.5V_{DD}-|V_{TP}|}\right] \quad (6)$$

where

$$a = \frac{\Delta k(V_{DD}-|V_{TP}|)}{RK_{9,10}K_{24,25}(1+\frac{V_{TN}}{|V_{TP}|})(V_X+V_Y)} \quad (7)$$

Equation (6) implies that the mismatch in the trans-conductance parameter leads to a DC offset at the output. Also, the threshold voltage mismatch can be modelled as ΔV_T in the form of V_{Ti}-V_{Tj}=ΔV_T. In this case, supposing that $\Delta V_T^2 << 1$, any conceivable mismatch in the threshold voltage causes the error, which is given by:

$$V''_{error} = \left[\frac{RK\Delta V_T(1+\frac{\Delta V_T}{V_T})(V_X{}^2-V_Y{}^2)(V_{TN}-|V_{TP}|)}{(V_{DD}-3V_{TN}+2\Delta V_T)(0.5V_{DD}-\Delta V_T)}\right] \quad (8)$$

Take notice that, since the denominator of Eq. (8) is much larger than the nominator, the resulted error is negligible.

3. Simulation Results

In order to prove the theoretical analysis of the multiplier circuit, the simulation results are considered with the supply voltage of 1.8 V, via HSPICE in 0.18 μm CMOS technology and with TSMC level 49 (BSIM3v3) parameters.

DC transfer behaviour of the designed circuit in the defined range of the inputs is depicted in Fig. 2. In this simulation, input voltages are chosen between -250 mV and +250 mV and then the output voltage swings between -250 mV to +250 mV. The measured linearity error in this range is obtained by 1.1%.

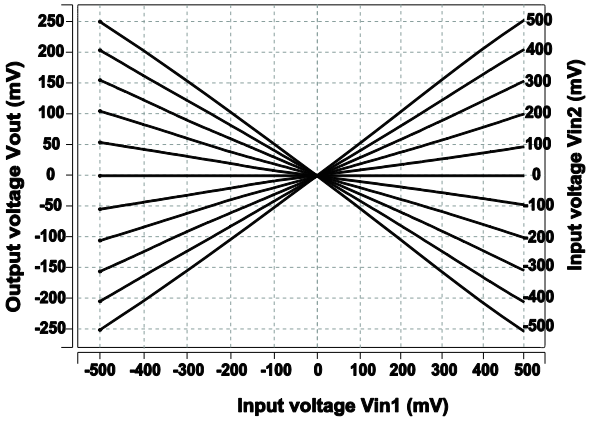

Fig. 2. Simulation results for DC transfer characteristic.

Figure 3 demonstrates the multiplier circuit, which is used as a balanced modulator and the error quantity is also calculated. The signal of V_x has a frequency of 500 kHz and considered as a carrier signal. Also, the frequency of V_y is 50 kHz, which is considered as a modulation signal. The amplitude of both voltages is 800 mV_{P-P} sinusoidal signal. The middle waveform shows AC modulated output, which results from the multiplication of input voltages. Also, the lower waveform depicts error measurement of the modulator circuit, which is the subtraction of ideal output and simulated waveform.

The frequency response of circuit in Fig. 4 depicts that -3 dB bandwidth is 1.45 GHz in the case that the input signal is fed to V_x and V_y = 400 mV. The same result is obtained for the constant value of V_x and AC signals for V_y. It should be pointed out that input signals are applied in which, the output of circuit be equal to 0 dB for precise measuring of -3 dB bandwidth of the circuit. Also, the total power consumption is obtained 84 µW. The total harmonic distortion versus input voltage at 1 MHz and 100 kHz are sketched in Fig. 5. In the worst case, it is found to be 0.37% when V_X is sinusoidal (500 mV_{P-P} at 1 MHz) and V_Y is set to 250 mV.

In order to examine the performance of the proposed design against the process variation, the Monte Carlo with 100 iterations is carried out by applying ±5% Gaussian distribution at $\pm 3\sigma$ level in the variation of all transistor threshold voltage and aspect ratio, simultaneously. Two sinusoidal voltages with the amplitudes of 400 mV_{p-p} and 800 mV_{p-p} and also frequencies of 500 kHz and 1 MHz are fed for the multiplier circuit and then the output signals are adapted with the theoretical values. The result is demonstrated in Fig. 6, in which, 73% of the total iterations happened with the error of less than ±0.5%.

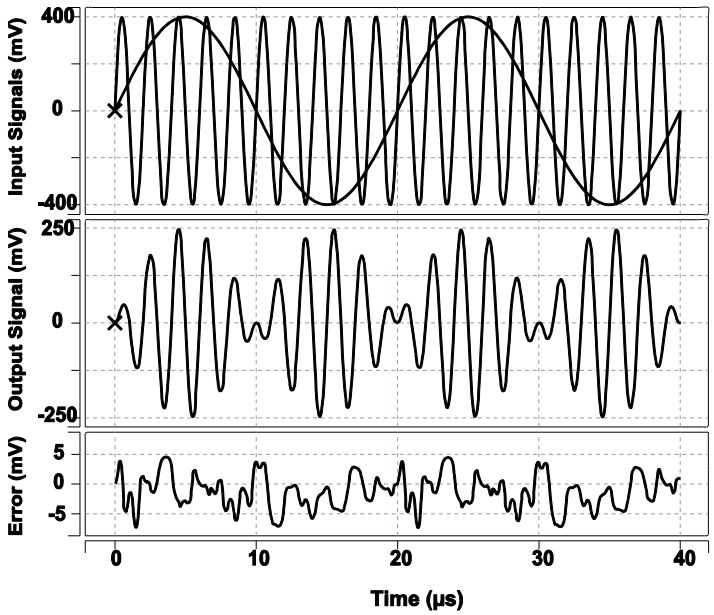

Fig. 3. The multiplier circuit is considered as a modulator. 50 kHz modulating signal and 500 kHz carrier sinusoid (upper part); the modulated signal (middle part); Error quantity (lower part).

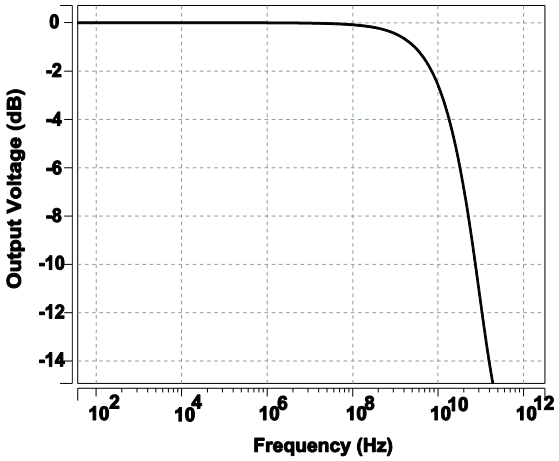

Fig. 4. Frequency response of the circuit.

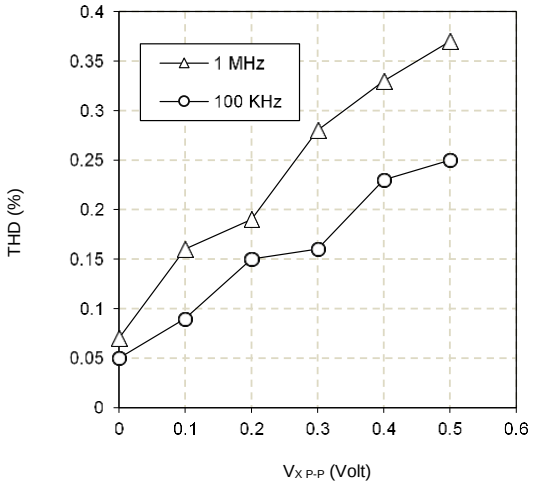

Fig. 5. Relation between THD and V_X.

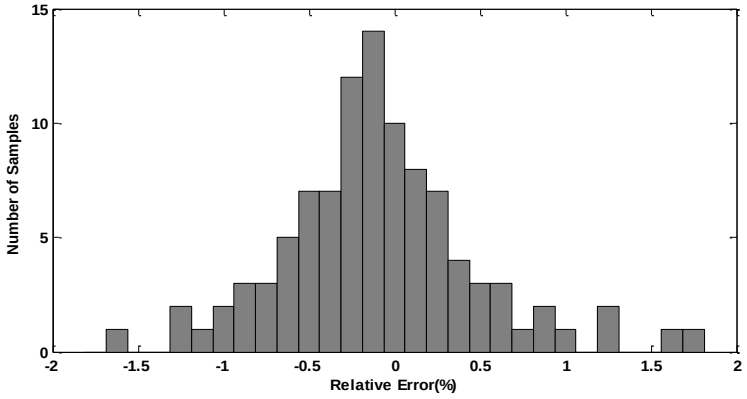

Fig. 6. Monte Carlo analysis of the circuit for ±5 % mismatch in threshold voltage and transistors aspect ratio.

Simulation results of the circuit are summarized in Table 1, which allows a deep comparison of this work and reported papers. According to Panigrahi and Paul [3], it is designed in the sub-threshold region, thus its power dissipation is low, while the dynamic input and output ranges are narrow. Also, the bandwidth of the circuit is limited to 221KHz. As reported by Roy et al. [15] benefits are from high input and output dynamic ranges, but the linearity of the circuit is poor. Based on a study by Naderi and Ozoguz [16], it is designed in the current mode and suffer from high power consumption, while the linearity of the circuit is satisfactory. According to Aloui et al. [18], it needs a double power supply and its bandwidth is limited to 300 MHz, the THD of the circuit is low while the linearity of the circuit is acceptable. The most optimization in our proposed work, includes high bandwidth, low THD and linearity, which guaranty the accuracy of the circuit.

Table 1. Comparative parameters of the proposed multiplier with recent works.

Year	**[3]**	**[15]**	**[16]**	**[18]**	**This work**
	2013	**2018**	**2016**	**2017**	**-**
Power supply (V)	0.5	± 2.5	2.8	± 0.75	1.8
Input range (mV)	± 80	± 250	± 10µA	± 10µA	± 500
Output range (mV)	± 10	± 250	± 10µA	± 10µA	± 250
Power consumption (µW)	0.714	230	520	150	84
THD (%)	4.11	2.25	1.45	0.8	0.4
Nonlinearity (%)	5.6	5.3	1.12	1.1	1.1
-3dB bandwidth (MHz)	0.221	68.55	137	300	1450
Technology (µm)	0.18	0.35	0.35	0.18	0.18

4. Conclusions

A novel CMOS analogue four-quadrant multiplier was presented in this paper. The precision of the circuit was significantly improved in comparison with recent work. In addition, the designed circuit was suitable for low power applications. To evaluate the performance of the proposed multiplier, the harmonic distortion due to the mismatches in threshold voltage and the trans-conductance parameter were discussed in detail. In order to verify the applicability of the circuit, it was utilized in a modulator structure and the simulation result was compared with the ideal performance of this application. The performance of circuit was characterized via HSPICE simulator in 0.18 µm CMOS technology with TSMC level 49 (BSIM3v3) parameters, where under a supply voltage of 1.8 V, the total harmonic distortion of the proposed circuit at 1 MHz, was lower than 0.4% and -3dB bandwidth was obtained 1.45 GHz.

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