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A NEW CURRENT TUNABLE CURRENT INPUT CURRENT OUTPUT BIQUAD USING CFTAS

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Abstract

A new current-tunable current input current output universal biquad circuit synthesized with three current follower trans-conductance amplifiers (CFTAs) and two grounded capacitors is presented in this paper. The proposed circuit simultaneously, realizes all five different standard filter functions i.e. low-pass, band-pass, high-pass, band-reject and all-pass across explicit high impedance current output terminals by the use of single current input signal. Moreover, the proposed filter circuit doesn't require any component matching conditions for the filtering functions realizations. Non-ideal and parasitic effects on filter's performance are also discussed. The validity of designed filter is verified through PSPICE programs using 0.25μm standard CMOS model parameters from TSMC.

Keywords: Analog signal processing, Biquad, Current-mode filter.

1. Introduction

The synthesis of low-voltage operated analog circuits using different current-mode active elements still attracts researchers owing to their advantages and usefulness at different stages of the high-performance systems designed for signal processing applications such as communication, sensing/automation, control, signal separation, signal generation and measurement etc. Some of the inherent advantages of current-mode active elements over their voltage-mode counter parts are, low supply voltage operation, high current swing, larger band width, higher slew rates, better immunity towards switching noise, low power consumption and high frequency operation [1-3].

Nomenclatures

g_m	Trans-conductance parameter, siemens.
Q	Quality factor

Greek Symbols

α_ι	Current pathway error
β_n	NMOS process parameter
γ_{ni}	Negative trans-conductance imprecision factor
γ_{pi}	Positive trans-conductance imprecision factor
ω_o	Angular pole frequency, rad

Abbreviations

AP	All Pass
BP	Band Pass
BR	Band Reject
BW	Band Width, hertz
CCCCTA	Current Controlled Current Conveyor Trans-Conductance Amplifier
CCCII	Current Controlled Current Conveyor
CCII	Second Generation Current Conveyor
CFTA	Current Follower Trans-Conductance Amplifier
HP	High Pass
LP	Low Pass
SIFO	Single Input Five Output
SITO	Single Input Three Output
TISO	Three Input Single Output

In the present scenario, low voltage portable electronic gadgets/equipments consuming less power are in demand. Therefore, low voltage operable current-mode circuits have become an attractive choice for the circuit designers. CFTA and its modified versions suggested in [4-7] are among the recently incepted current-mode active elements. The combined features of current follower and multi output trans-conductance amplifiers assist for the suitable terminal impedances and single current control property of the CFTA. Therefore, numbers of analog blocks such as current-mode filters, oscillator [8-19], etc., based on CFTA have been reported in the literature.

Each of the reported CFTA based single input three output (SITO) current mode filters having two [8] or three [9-10] CFTAs and two grounded capacitors, realizes LP, BP, HP filtering functions simultaneously. Other functions like BR and AP functions can also be obtained in these filters by adding appropriate current outputs (LP and HP for BR) and/or (LP, BP, and HP for AP) together. Other reported four CFTAs based current mode filter [11] realizes LP and BP filtering functions simultaneously, whereas remaining filtering functions can also be realized by adding explicitly obtained current outputs appropriately. Another valuable single input five output (SIFO) current-mode filter circuit requiring four CFTAs [12] and two grounded capacitors in the implementation, realizes five generic functions (LP, BP, HP, BR, and AP), simultaneously, across explicit current output terminals. However, all these circuits require a supply voltage greater than ± 1.2V which is not a prominent situation for low voltage low power operation.

On the other hand, each CFTA based three input single output current-mode filters [13-16] having two [13-15] or three [16] CFTAs and two grounded capacitors and can realize all the five standard filtering functions, but one at a time through appropriate selection of input(s). Unfortunately, most of the filter circuits [13-15] require scaled and/or inverted current inputs for at least one filtering function realization which actually need additional active elements in realization. Beside it, each of these current-mode filters suffers from the problem of current insertion at several nodes which may further increase the additional hardware.

Few more current-mode filters based on three or more active elements other than CFTAs such as CCCIIs [20-25,] and CCCCTAs [26-28] are also proposed in the literature. However, these filter circuits still suffer from at least one of the following drawbacks.

i. Does not realize all five filtering functions, simultaneously [20, 24, 25, 28].
ii. Need of inverted current input to realize AP function, which further required additional active elements to obtain inverted current signal [22].
iii. Either requires one floating passive element [27] or more than two passive elements to realize filtering function in current-mode [23, 26].
iv. Use of more than ± 1V power supply for filter implementation [20-27].

The proposed current input current output biquad in this paper is competent to realize all five different generic filter functions, simultaneously across various high impedance explicit current output terminals and does not require inverted/scaled current input signal(s) for the realization of any filtering function(s). Moreover, the circuit is a resistor less CMOS topology employing three CFTAs and two grounded capacitors and operated at low supply voltages (± 0.75 V) with total power consumption of only 0.98 mW. The performances of the circuit under concern are illustrated by PSPICE simulations.

2. Proposed Circuit

Since after its inception as a current-mode active element and its terminal impedance suitability for the current-mode signal processing applications, CFTA has been received considerable attention from the circuit designers [4, 6-19]. The CFTA with symbolic diagram as shown in Fig. 1 can be characterized by the Eq. (1).

$$V_f = 0, \quad I_Z = I_f, \quad I_{\pm X} = g_m V_Z \tag{1}$$

where g_m is the trans-conductance parameter of CFTA whose value depends upon the biasing current of I_S.

The proposed current input current output biquad filter is shown in Fig. 2.

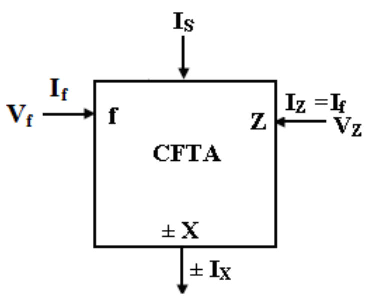

Fig. 1. CFTA schematic symbol.

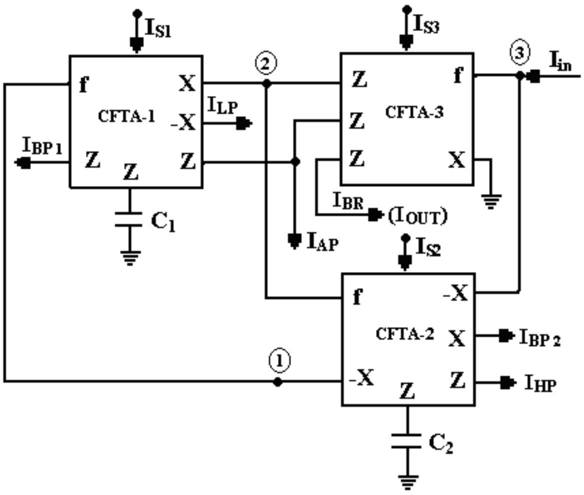

Fig. 2. Proposed universal current-mode biquad filter.

Through routine analysis of the proposed filter circuit, the following current transfer functions can be obtained across explicit high impedance terminals at I_{LP}, I_{HP}, I_{BP1}, I_{BP2}, I_{BR} and I_{AP}.

$$\frac{I_{LP}}{I_{in}} = \frac{g_{m1}g_{m2}}{D(s)} \tag{2}$$

$$\frac{I_{HP}}{I_{in}} = \frac{C_1C_2s^2}{D(s)} \tag{3}$$

$$\frac{I_{BP1}}{I_{in}} = \frac{g_{m2}C_1s}{D(s)} \tag{4}$$

$$\frac{I_{BP2}}{I_{in}} = \frac{-g_{m2}C_1s}{D(s)} \tag{5}$$

$$\frac{I_{BR}}{I_{in}} = \frac{-(C_1C_2s^2 + g_{m1}g_{m2})}{D(s)} \tag{6}$$

$$\frac{I_{AP}}{I_{in}} = \frac{-(C_1C_2s^2 - g_{m2}C_1s + g_{m1}g_{m2})}{D(s)} \tag{7}$$

where, $D(s) = C_1C_2s^2 + g_{m2}C_1s + g_{m1}g_{m2}$ (8)

It is evident from Eqs. (3) to (8) that non-inverting LP, non-inverting HP, non-inverting BP, inverting BP, inverting BR, and inverting AP responses are explicitly and simultaneously obtained across high impedance output terminals. Thus, proposed filter is single input five output (SIFO) current-mode filter. Accordingly, the expressions of ω_o, Q and BW (ω_o/Q) for these filtering responses can be expressed in Eq. (9).

$$\omega_o = \left(\frac{g_{m1}g_{m2}}{C_1C_2}\right)^{\frac{1}{2}}, Q = \left(\frac{C_2 g_{m1}}{C_1 g_{m2}}\right)^{\frac{1}{2}} \text{ and } BW = \left(\frac{g_{m2}}{C_2}\right) \tag{9}$$

CMOS implementation of CFTA [13] is shown in Fig. 3. The trans-conductance parameter g_{mi} of CMOS based i^{th} CFTA (i = 1,2,3), can be controlled through the biasing current I_{Si} as shown in Eq. (10).

$$g_{mi} = \sqrt{\beta_n I_{S_i}} \tag{10}$$

where, $\beta_n = \mu_n C_{OX}\left(W/L\right)$ is the process parameter for NMOS transistors M_7-M_8 forming differential pair at the trans-conductance stage of CFTA. On substituting inherent trans-conductance parameter g_{mi} from Eq. (10) into Eq. (9), it yields;

$$\omega_o = \left(\frac{\beta_n\sqrt{(I_{S_1}I_{S_2})}}{C_1C_2}\right)^{\frac{1}{2}}, Q = \left(\frac{C_2}{C_1}\sqrt{\frac{I_{S_1}}{I_{S_2}}}\right)^{\frac{1}{2}}, \text{ and } BW = \frac{\omega_o}{Q} = \frac{1}{C_2}\left(\beta_n I_{S_2}\right)^{\frac{1}{2}} \tag{11}$$

From Eq. (11), it can be seen that by maintaining a constant ratio of I_{S1} and I_{S2} the ω_o can be orthogonally electronically adjusted by I_{S1} and I_{S2} without disturbing Q. Furthermore, it can also be noted that the Q can also be electronically tuned independent of ω_0 by maintaining the product of I_{S1} and I_{S2} to be invariable.

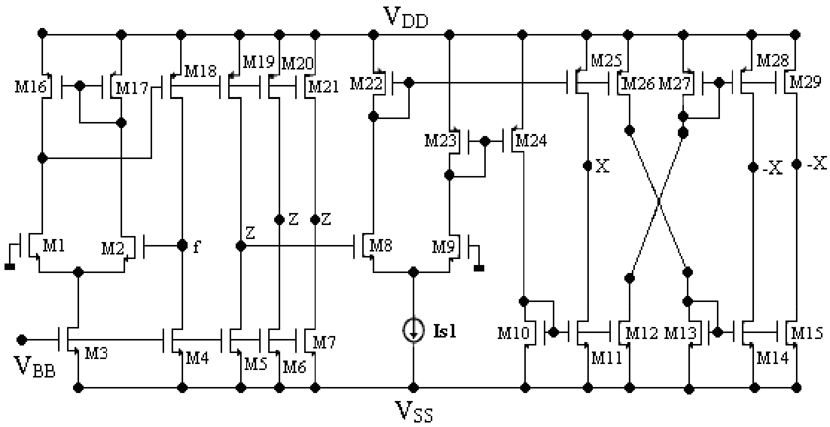

Fig. 3. The CMOS implementation of CFTA.

3. Non-Ideal Analysis

Taking the non-ideal factors of CFTA into account, the port depiction of the non-ideal CFTA can be revised in Eq. (12).

$$V_{f_i} = 0, \quad I_{Z_i} = \alpha_i\, I_{f_i}, \quad I_{+Xi} = \gamma_{pi}\, g_{mi}V_{Zi}, \quad I_{-Xi} = -\gamma_{ni}\, g_{mi}V_{Zi} \tag{12}$$

where, α_i =1-ε_i and ε_i (| ε_i | <<1) signify the current pathway error between f and $+Z$ terminal. Similarly, γ_{pi} and γ_{ni} are the trans-conductance imprecision factor between Z

to *X* and *Z* to -*X* terminals, respectively. The non-ideal analysis of the proposed filter circuit in Fig. 2 relent the following characteristic Eq. (13).

$$D(s) = C_1 C_2 s^2 + \alpha_2 \alpha_3 \gamma_{n2} g_{m2} C_1 s + \alpha_1 \alpha_2 \gamma_{p1} \gamma_{n2} g_{m1} g_{m2} \tag{13}$$

Accordingly, for the proposed filter the ω_o and Q are changed to Eq. (14).

$$\omega_o = \left(\frac{\alpha_1 \alpha_2 \gamma_{p1} \gamma_{n2} g_{m1} g_{m2}}{C_1 C_2} \right)^{\frac{1}{2}}, Q = \frac{1}{\alpha_3} \left(\frac{\alpha_1 \gamma_{p1} C_2 g_{m1}}{\alpha_2 \gamma_{n2} C_1 g_{m2}} \right)^{\frac{1}{2}} \; BW = \left(\frac{\alpha_2 \alpha_3 \gamma_{n2} g_{m2}}{C_2} \right) \tag{14}$$

The active and passive sensitivities of the circuit in Fig. 2, can be calculated as shown in Eqs. (15) and (16).

$$S^{\omega_o}_{\alpha_1, \alpha_2, \gamma_{p1}, \gamma_{n2}, g_{m1}, g_{m2}} = \frac{1}{2}, S^{\omega_o}_{C_1, C_2} = -\frac{1}{2} \tag{15}$$

$$S^{Q}_{\alpha_1, \gamma_{p1}, C_2, g_{m1}} = \frac{1}{2}, \; S^{Q}_{\alpha_2, \gamma_{n2}, C_1, g_{m2}} = -\frac{1}{2}, \; S^{Q}_{\alpha_3} = -1 \tag{16}$$

From Eqs. (15) snd (16), we can conclude that all the incremental active and passive sensitivities are low and not more than one in magnitude.

4. Parasitic Study

In this section, the performance of the proposed current input current output SIFO biquad filter in the presence of various parasitic impedance effects of CFTAs is to be considered. A practical CFTA, similar to any other active element includes various ports parasitic as shown in Fig. 4. The parasitic resistance at f- terminal of i^{th} CFTA (*i*= 1, 2, 3) are R_{f1}, R_{f2}, and R_{f3}, respectively. Besides it, practical CFTA has port *Z* parasitic in the form of $R_{Zi}//C_{Zi}$ and port ±*X* parasitic in the form of $R_{Xi}//C_{Xi}$. In the proposed circuit topology in Fig. 2, we can see that low impedance f terminal of each CFTA is connected to high impedance +*X* or -*X* terminals of other CFTA. This use of current feedback minimizes or eliminates the possibilities of parasitic impedance effects. Furthermore, to eradicate the effect of these parasitic elements in the proposed circuit of Fig. 2, identical CFTAs with low input parasitic resistance R_f should be employed. Ideally, the R_f is zero. Since R_f parasitic impedances are connected between true ground node *f'* and virtually grounded node *f*. Therefore, these are almost ineffective. As a result, parasitic impedances of –*X* terminal of CFTA-1 at node1, -*X* terminal of CFTA-2 at node 3 and X, Z terminal of CFTA-3 at node 2 are almost vanish or ineffective. The only parasitic impedances for consideration are Z_1 and Z_2 across external capacitors C_1 and C_2 connected between high impedance *Z* terminal and ground of CFTA-1 and CFTA-3. The parasitic resistances at Z_1 and Z_2 terminals are R_{Z1} and R_{Z2} and the external working capacitances C_1 and C_2 get increase to C_a and C_b by absorbing parasitic capacitances C_{Z1} and C_{Z2}, respectively. With $C_a = (C_1 + C_{Z1})$ and $C_b = (C_2 + C_{Z2})$, a much greater value for the externally used capacitances C_1 and C_2 must be chosen in comparison to the parasitic capacitances at the *Z* and ±*X* terminals of CFTA i.e. C_1, $C_2 >> C_Z$, C_X. By choosing $(C_1 = C_2) >> C_Z$, C_X and $g_{m1} = g_{m2}$ in the design, these undesirable factors can be eliminated or minimized and hence, the proposed filter may approach towards ideal response, if we choose the following design criterion.

$$\frac{1}{g_{m2}R_{Z1}} << 1, \frac{1}{g_{m2}R_C} << 1 \text{ and } \left|\frac{1}{\omega C_1}\right| << R_{Z1} \tag{17}$$

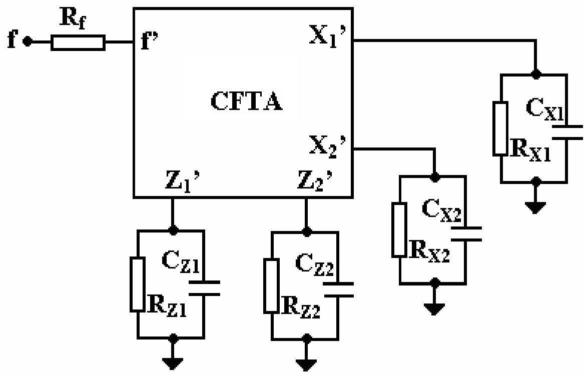

Fig. 4. CFTA with port parasitic.

5. Simulation Results and Discussion

In this section, the proposed circuit in Fig. 2 has been simulated using the P-spice programs on cadence tools to demonstrate its feasibility. The CFTA given in Fig. 1 was realized using CMOS implementation as shown in Fig. 3, with TSMC 0.25μm CMOS process model parameters [29]. The circuit was biased with power supply V_{DD} = -V_{SS} = 0.75V and V_{BB} = -0.3V. The dimensions of MOS transistors were used as specified in Table. 1. The proposed filter was designed for the biquadratic performance with $f_o = \omega_o/2\pi$ = 6.4 MHz and Q = 1. In design, the active and passive components were set as $I_{S1} = I_{S2} = I_{S3}$ = 25μA with ($g_{m1} = g_{m2} = g_{m3}$ = 398μA/V), and $C_1 = C_2$ = 10pF, which results a total power consumption of only 0.98 mW. Figure 5 shows the simulated current gain responses of the LP, BP, BR, HP and AP filtering functions. Figures 6 and 7 show the gain and phase responses of BR and AP filtering functions respectively. The pole frequency measured from simulation results is 6.33 MHz which is much closer to theoretical value. To show the electronic tuning aspects of the proposed current-mode filter, the circuit is further simulated to obtain various BR and BP responses at different sets of I_{S1} and I_{S2} in such a way so that $I_{S1} = I_{S2}$ = 7μA, 10μA, 25μA, 100μA which result in the pole frequency variation as 2.68 MHz, 4.22 MHz, 6.33 MHz and 11.18 MHz, respectively, at constant Q = 1.

Table 1. Transistor dimensions of CMOS implemented CFTA.

Transistors	Dimensions
NMOS	***W*(μm)/L(μm)**
M_1, M_2	1/0.25
M_3-M_7, M_{10}-M_{15}	3/0.25
M_8,M_9	7.5/0.25
PMOS	***W*(μm)/L(μm)**
M_{16}-M_{23}, M_{25}-M_{29}	5/0.25
M_{24}	4.5/0.25

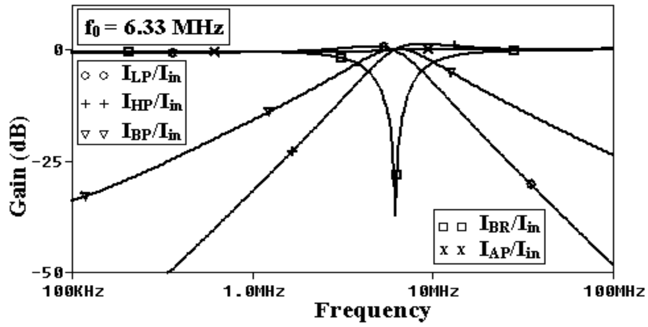

Fig. 5. Current gain responses of the proposed SIFO current-mode filter.

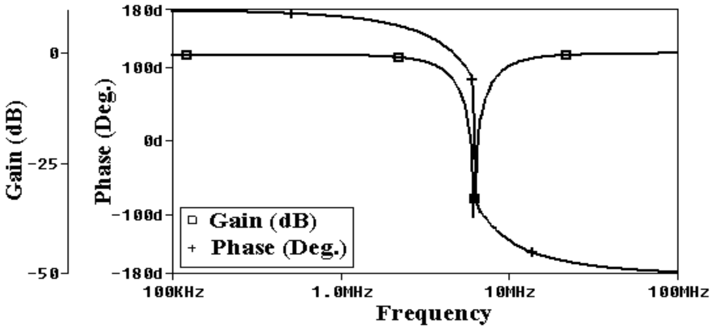

Fig. 6. Gain and phase responses of BR filter function.

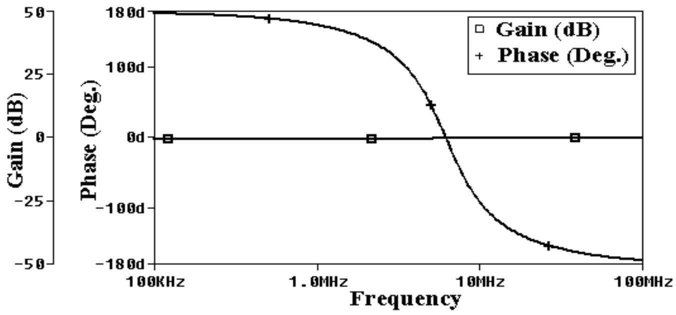

Fig. 7. Gain and phase responses of AP filter function.

The simulated result showing the pole frequency tuning aspect independent of Q is shown in Fig. 8. In Fig. 9, the time-domain analysis of BP filter is displayed, which is obtained by applying a sinusoidal input of 50µA peak to peak at 6.33 MHz. Similarly, the time-domain analysis of HP filtering function is also shown in Fig. 10 which is obtained by applying a sinusoidal input of 40µA peak at 150 MHz. Next, the THDs of the BP response of the proposed circuit was also measured by applying a current input sinusoidal signal of varying amplitude from 10 µA to 55 µA at constant frequency of 6.4 MHz. THDs result is shown in Fig. 11 which confirms that the %THD figures are adequate and not more than the acceptable range of 2.5% [28] which causes the BP output will not be distorted significantly for an applied sinusoidal current input of variable amplitude and constant frequency.

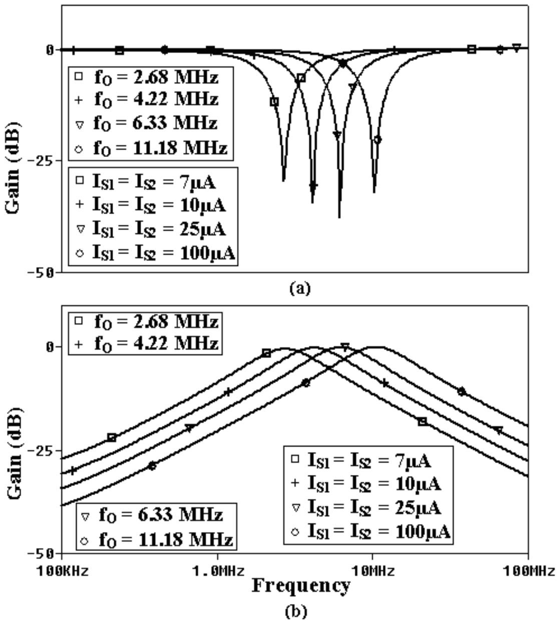

Fig. 8. Simulated responses of the proposed filter, showing variation in pole frequency (f_o) at constant Q = 1 (a) BR (b) BP.

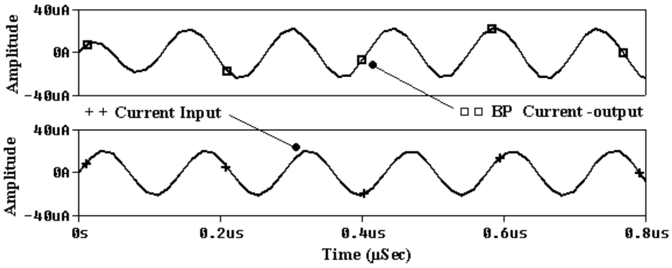

Fig. 9. Time-domain response of proposed BP filter with respect to sinusoidal current input signal.

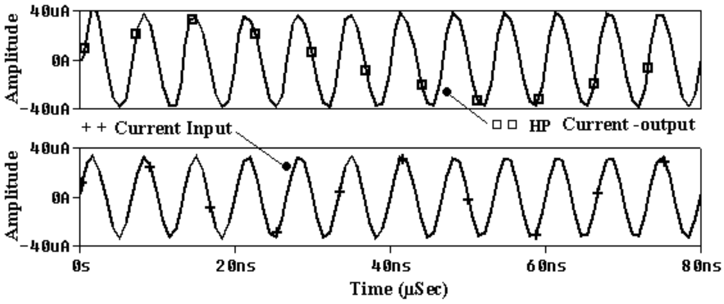

Fig. 10. Time-domain responses of proposed HP filter function with respect of sinusoidal current input signal.

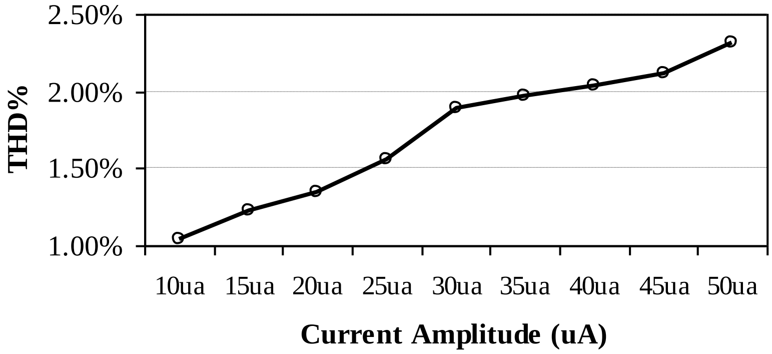

Fig. 11. Variation in %THD of BP response.

To observe the effect of passive component mismatching on the filter's performance, Monte-Carlo analysis has been performed for 100 samples. For this, the BP filter was simulated by selecting the values of capacitors C_1 and C_2 with 5% Gaussian deviation. The statistical results in histogram are shown in Fig. 12, where the simulated mean, median and standard deviations were obtained 6.76 MHz, 6.74 MHz and 131.62 kHz, respectively which reveal that with respect to the simulated pole frequency of 6.33 MHz, the proposed filter is less sensitive to the changes in capacitors value and thus offers good passive sensitivity.

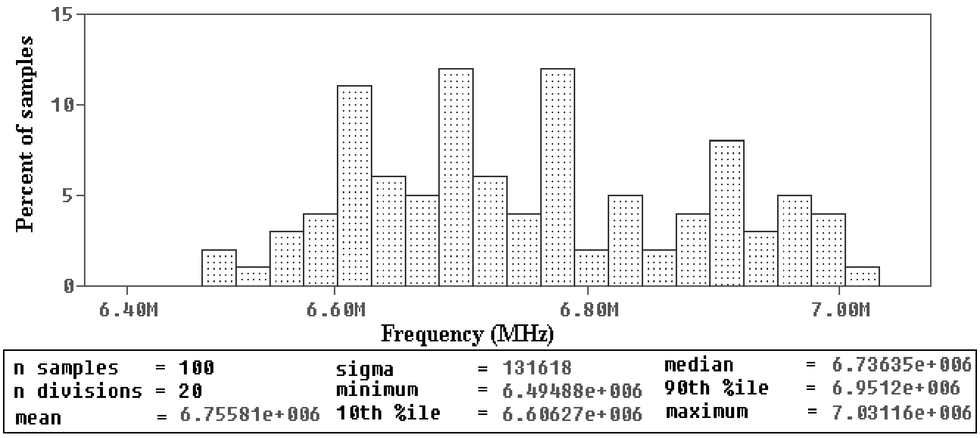

Fig. 12. Statistical results of Monte-Carlo analysis for the BP response with 5% deviation in the capacitor values.

6. Another Aspect of Proposed Topology

In addition of single input five output current-mode operation of proposed topology as discussed in the above sections, the same topology has another interesting aspect which is three inputs single output (TISO) current-mode operation and can also be used as TISO current-mode filter as shown in Fig. 13.

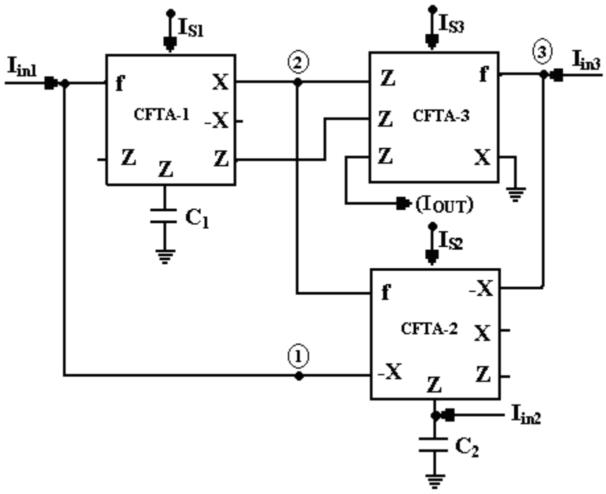

Fig. 13. TISO configuration of the proposed circuit in Fig. 2.

The configuration can still realize all five filtering functions at current output Iout, depending upon the appropriate selection of current input(s) which are follow as

i. A non-inverted LP response with $I_{in1} = I_{in}$ and $I_{in2} = I_{in3} = 0$.

ii. A non-inverted BP response with $I_{in2} = I_{in}$ and $I_{in1} = I_{in3} = 0$.

iii. An inverted HP with $I_{in3} = I_{in1} = I_{in}$ and $I_{in2} = 0$.

iv. An inverted BR with $I_{in3} = I_{in}$ and $I_{in1} = I_{in2} = 0$.

v. An inverted AP with $I_{in2} = I_{in3} = I_{in}$ and $I_{in1} = 0$.

However, the TISO configuration of current-mode filter suffers from some problem like current insertion at several nodes which may increase additional hardware. So in general, there is no use of presenting the TISO, when SIFO can be realized from same topology.

Although, few of the current-mode topologies are reported in the literature which have realized all five standard filter functions (LP, BP, HP, BR and AP) in both SIFO (single input five output) and TISO configurations [30-32]. Hence, the proposed work which having capability of realizing all five standard filter functions with both SIFO and TISO configurations is compared with the similar works in cited Refs. [30-32] as arranged in Table 2. Study of Table 2 reveals the following;

- The number of active elements used in the present proposal is only three which is same as that in Ref. [30, 31]. However, the elements used in Ref. [32] are two, but as it requires component matching constraints to realize HP function which may need additional elements.
- In the present work, the circuit is operated at low voltage power supply of ± 0.75V and consume less power (0.98 mW) as compared to the works reported in [30-32], which use at least ± 1.65V power supply [30].
- In the present work, the circuit is successfully designed for a high pole frequency of 6.4 MHz with low value capacitors (10pF) as compared to the proposals in [30-32].

- In contrast to the present work, the circuit in [31] uses capacitor at low impedance input terminal of the active element which will limit the higher operating frequency range of the circuit [33].

Table 2. Comparison with the similar type works reported in [30-32].

Features	Ref. [30]	Ref. [31]	Ref. [32]	Proposed
Active elements	3 CCCIIs	2 CCIIs and 1 CCIII	2 CCCCTAs	3 CFTAs
Passive elements	$C_1=C_2 = 100pF$	$C_1= C_2 = 1nF$ $R_1=R_2 = 1K\Omega$	$C_1= C_2 = 0.2nF$	$C_1=C_2 = 10pF$
Orthogonal tunability of Q and ω_0	No	No	Yes	Yes
Matching Conditions required	No	No	Yes	No
Capacitor connected at high impedance input port of the element	No	Yes	No	No
Low active and passive sensitivity	Yes	Yes	Yes	Yes
Power Supply Rails	± 1.65 V	± 2.5 V	± 1.75 V	± 0.75 V
Operating pole frequency	1.27 MHz	159 kHZ	2.76 MHz	6.4 MHz

From the above comparison, it may be concluded that the proposed design affords low cost, lower operated supply rails and low power solution for the applications where cost and power are of prime concern.

7. Conclusion

A universal current input current output also called current-mode biquad filter consisting of three CFTAs and two grounded capacitors is described in this proposal. Effect of non-ideal factors and parasitic of the active element on the performance of the proposed circuit is studied and discussed in detail. Besides it, extensive PSPICE simulation results are also made to study all aspect of new current-mode filter. As expected, the simulation results agree quite well with theoretical ones. However, slight deviation may arise due to non-ideal factors and the parasitic involved. Moreover, the proposed filter offers subsequent noticeable advantages:

- Versatility: The proposed circuit realizes all five current-mode filtering functions, simultaneously by the use of single current input and thus, providing SIFO structure. The proposed structure can be made versatile in the sense that same structure can also realize all five standard filtering functions using TISO configuration as discussed in section 6.
- Canonical structure: The proposed circuit is a canonical structure as it requires only two grounded capacitors as passive elements. The canonical structure is ideally suited for the integrability.

- Low supply and power consumption: The circuit is operated at DC power supply rails of ± 0.75V and its total power consumption is only 0.98 mW, which is attractive for the battery operated portable electronic gadgets and mobile communication systems.
- Impedance matching: With the use of CFTAs as active elements in the filter design, there is availability of high impedance explicit output terminals for proper impedance matching and no external buffers will be needed to draw the current-mode responses. High impedance explicit outputs are also suitable for direct cascading to implement higher order filters.

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