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MODELING OF MTJ AND ITS VALIDATION USING NANOSCALE MRAM BITCELL

CHANDRAMAULESHWAR ROY[1,*],
ARUNDHATI BHATTACHARYA[2], A. ISLAM[3]

Department of Electronics and Communication Engineering,
Birla Institute of Technology, Mesra, Ranchi, Jharkhand, India, Pin-835215
* Corresponding Author: chandram@bitmesra.ac.in

Abstract

Magnetic Tunnel Junction (MTJ) is a promising candidate for nonvolatile and low power memory design. MTJ is basic building block of STT-MRAM bitcell. We develop a Verilog-A based behavioral model of MTJ which effectively exhibits electrical characteristics of MTJ with a very low switching current (27.2 μA for parallel to antiparallel and 19.2 μA for antiparallel to parallel switching). To verify the versatility of the proposed model, we have employed it to design MTJ- based MRAM bitcell. Simulation results (of read margin, write margin and variability analysis of MTJ-MRAM bitcell) demonstrate importance of our proposed model.

Keywords: MRAM; TMR; CIMS; Read margin; Write margin.

1. Introduction

Extensive investigation is going on MTJ (Magnetic Tunnel Junction) due to their fertile physics and potential applications [1]. An MTJ nanopillar is mainly consists of three thin films, namely, a thin oxide barrier and two ferromagnetic (FM) layers [2]. The magnetization direction of one layer, called pinned layer (PL) is fixed, and magnetization of other layer, called free layer (FL) is changed by changing bias condition and passing appropriate amount of current. When magnetic moments of two layers are aligned in same direction, they are said to be in parallel state (P: low resistance state) and when free layer magnetization is opposite to that of fixed layer, then they are said to be in anti-parallel state (AP: high resistance state) [3].

Traditionally magnetic orientation of free layer was changed by applying external magnetic field above a threshold value. This is known as FIMS

Nomenclatures

e	Electronic charge
g	Spin polarization efficiency
g_{sv}	Spin polarization efficiency value in a spin value
t_{unnel}	Spin polarization efficiency value of a Tunnel junction nanopillar
H_k	Anisotropy field
I_c	Switching threshold current
I_{ds}	drain to source current
I_{HL}	Nominal high to low switching current
I_{LH}	Nominal low to high switching current
I_{RAP}	Mean read current when MTJ is in AP sate
I_{RP}	Mean read current when MTJ is in P state
$I_{w AP-P}$	Anti-parallel to parallel write current
$I_{w P-AP}$	Parallel to anti-parallel write current
J_c	Critical current density
M_s	Saturation magnetization
p	Polarization percentage of the tunnel current
R_{AP}	Antiparallel state resistance
R_p	Parallel state resistance
RM_{AP}	Read margin in Antiparallel state
RM_p	Read margin in parallel sate
t_{ox}	Oxide thickness
V	Volume of the free space
v_b	bias voltage when $TMR_{real} = 0.5 \times TMR(0)$
V_{DD}	supply voltage
WM_{AP-P}	Write Margin from antiparallel to parallel state
WM_{P-AP}	Write Margin from parallel to antiparallel state

Greek Symbols

α	Magnetic damping constant
γ	Gyromagnetic ratio
Φ	Potential barrier
μ_0	Permeability of free space
μ_B	Bohr magnetron
θ	Angle between the magnetization direction of the fee and fixed layer

Abbreviations

AP	Antiparallel
BL	Bit Line
CIMS	Current Induced Magnetic Switching
DRAM	Dynamic Random Access Memory
FIMS	Field Effect Magnetic Switching
FL	Free Layer
FM	Ferromagnetic
MFF	Magnetic Flip-Flop
MRAM	Magnetic Random Access Memory
MTJ	Magnetic Tunnel Junction
P	Parallel

PL	Pinned Layer
PMA	Perpendicular Magnetic Anisotropy
SL	Source Line
SRAM	Static Random Access Memory
STT	Spin Transfer Torque
TMR	Tunnel Magneto-resistance Ratio
WL_R	Read word line
WL_W	Write word line

(Field Induced Magnetic Switching). But the limitations of FIMS are scalability and power consumption [4]. Tsoi et al. [5] and Myers et al. [6] showed that magnetic switching can occur by passing spin polarized current through MTJ. This is known as Spin Transfer Torque or Current Induced Magnetic Switching (CIMS). CIMS shows considerable improvement over FIMS as it simplifies the circuitry used in this device [7]. Switching of MTJ with spin polarized current leads to very high density on-chip magnetic storage with very lower power consumption [8, 9]. STT switching is dependent on current densities (in ampere per square meter). This shows that smaller device requires lower current. So it becomes easier to correlate between CMOS device and MTJ [4]. However it needs to efficiently simulate hybrid MTJ/CMOS devices to evaluate their impact on system design because such circuit use both electron charge and spin [8]. Recently many MTJ-CMOS hybrid magnetic flip-flop (MFF) and memory circuits [10], [11], digital circuits (such as full adders), and oscillator circuit (such as spin-torque oscillator) have been proposed. MTJ also has numerous application including magnetic field sensors and high-frequency detectors [12].

Based on the physical origin of the free layer magnetization magnetic tunnel junctions are classified into two types: in- plane and perpendicular MTJ [13]. Lateral shape of former causes the magnetic anisotropy while the latter has no shape anisotropy. It depends upon the materials choice. Though in- plane MTJs are far more matured than their perpendicular counterparts, there is growing interest in the perpendicular devices as they are believed to have a low switching current density [14].

One of the applications of MTJ is nonvolatile memory circuit like STT-MRAM circuit. The conventional memory like SRAM, DRAM and flash memories are not meeting the requirement of high speed and memory hungry processors. STT-MRAM is answer to all issues of previous memory technologies because it has all desired memory attributes like nonvolatility, unlimited endurance, low power, high speed, and high memory density [15].

So it is very imperative to effectively model the static and dynamic behavior of MTJ due to its wide non-volatile applications in memory as well as logic circuits. In this paper we model the behavior of the MTJ in Verilog-A as Verilog-A language has become the preferred compact modelling language for both academic and industrial research groups because of its flexibility to run in numerous electrical simulators (Spectre, HSPICE, ADS, Eldo) [16]. Investigation is going on to improve performance metrics of MTJ such as tunneling magneto-resistance ratio (TMR), critical switching current, etc. [17]. So the focus of this paper is to make a reliable MTJ model which can be used in various applications.

This paper proposes a behavioral model of STT-MTJ using Verilog-A. Moreover, the model is employed to design 2T-1 MTJ MRAM bitcell for verifying its versatility. To verify and validate the proposed model extensive simulation of

MRAM bitcell is performed on HSPICE using 32 nm Predictive Technology Model (PTM) [18] of NMOS.

The rest of the paper is organized as follows. Section 2 presents the proposed MTJ model. Section 3 validates the proposed model using MRAM bitcell. Finally, Section 4 represents the comparison of proposed MTJ model with existing model, the concluding remarks are provided in section 5.

2. Switching Principle of Magnetic Tunnel Junction and Modeling of MTJ using Verilog-A.

Nanopillar of MTJ consists of tunneling barrier (MgO) sandwiched between two ferromagnetic (FM) layers. The FM layers of nanopillar (≈100 nm) are engineered in such a way that one layer is made thicker enough to be insensitive to spin transfer torque (STT) so that its magnetic alignment remains fixed. The other layer is sized thin enough to be sensitive for CIMS. In other words, the magnetic polarization of thin FM layer can be made parallel (P) or antiparallel (AP) with respect to thick FM layer. Of course, if the current density ($>10^6$ A/cm^2) is high enough resulting in sufficient spin transfer torque to reverse the magnetic polarization.

Figure 1(a) shows a schematic of nanopillar, in which magnetic alignment of FM layers are initially antiparallel. When current is passed from thin FM layer to thick FM layer electrons move from thick-to-thin layer. The thin FM layer exerts torque to the electrons for aligning their spin moment toward its magnetic direction. According to Newton's third law of motion, the electrons also exert spin transfer torque to the thin FM layer. If the current density is high enough the spin transfer torque exerted by electrons causes reversal of magnetic alignment of thin FM layer establishing antiparallel-to-parallel alignment.

Figure 1(b) shows a schematic of nanopillar, in which magnetic alignment of FM layers are initially parallel. When current is passed from thick FM layer to thin FM layer the electrons (moving from thin-to-thick layer) reflected by (thick FM layer) scattering are aligned antiparallel to thick FM layer and these reflected electrons exert spin transfer torque to thin FM layer. This results in reversal of magnetic direction establishing parallel-to-antiparallel alignment. The CIMS from parallel-to-antiparallel requires higher switching current than CIMS from antiparallel-to-parallel [19].

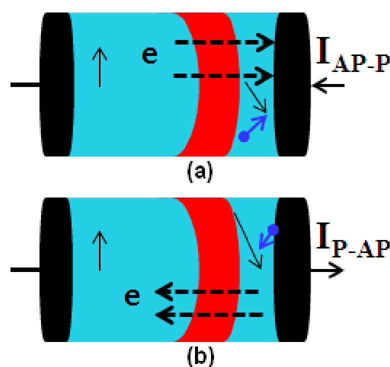

Fig. 1. Switching mechanism (a) antiparallel-to-parallel, (b) parallel-to-antiparallel.

2.1. Background

Researchers are trying to model behavioral characteristics of MTJ. The static, dynamic, and stochastic behavior of MTJ is required to be electrically integrated in the behavioral model. Therefore, physical model represents the static, dynamic, and stochastic behavior of the STT PMA (Perpendicular Magnetic Anisotropy) MTJ. Physical model of MTJ gives the resistance which depends upon magnetic configuration –parallel (P) or antiparallel (AP). It also defines switching threshold current which is required to switch between two states [2].

The focus of this paper is to improve the design metrics of MTJ such as decreasing the switching current and increasing TMR value. The resistance and critical switching current depends on oxide thickness, area and volume of MTJ. Model in this paper is based on some latest experimental data available in [2, 20, 21] which are used to calculate resistance and critical switching current of MTJ.

Now a day's Verilog-A/MS is becoming very popular as it is widely used in analog and mixed signal modeling of devices and circuits in the semiconductor industry. Though Garg et al. [22] have described their model in Verilog-A but the value of critical switching current of their model is very high (390 µA in P to AP) and (500 µA in AP to P) and TMR value is also less (95%). Therefore, this paper proposes a Verilog-A based behavioral model which characterizes MTJ with the use of latest fabricated data.

2.2. Modeling of parallel resistance

A simplified equation for parallel state resistance is defined below:-

$$R_P = \frac{(t_{ax} \times \exp(1.025 \times t_{ox} \times \phi^{1.4})}{(F \times \phi^{1.4} \times Area)} \tag{1}$$

where t_{ox} = oxide thickness, ϕ = potential barrier height for crystalline MgO = 0.4. F is a parameter that depends on material composition of three thin layers. It is calculated from Resistance Area product (R.A) value. In our model, R.A (resistance area) is 9.2 Ω · µm^2, which gives F = 332.2 [2].

2.3. Modeling of TMR (Tunnel Magneto-resistance) and antiparallel resistance and their bias voltage dependence

One of the properties of MTJ is that its tunnel magneto-resistance and antiparallel resistance changes with bias voltage. With increase in bias voltage there is a sharp decrease in TMR and antiparallel resistance [23] (Figs. 2 and 3). This happened because tunnelling probability decreases across the insulator with the increase in barrier height which further depends on junction bias [24]. This can be described by the following equation defined in [25].

$$TMR_{real} = \frac{TMR(0)}{(1 + (\frac{V_{bias}}{V_h})^2)} \tag{2}$$

$$R_{AP} = R_P \times \left(1 + TMR_{real}\right) \tag{3}$$

TMR_{real} can also be expressed as $\frac{(R_{AP}-R_P)}{R_P}$

where TMR_{real} is the real value of the *TMR* ratio during simulation, *TMR*(0) is the *TMR* ratio with 0 bias voltage, and V_h is the bias voltage when $TMR_{real} = 0.5 \times TMR(0)$. For this model, the default value of *TMR (0)* is set to 150% [2, 20] and $V_h = 0.9$ V.

By using a crystalline MgO layer instead of amorphous Al_2O_3, the *TMR* increases from 30–70% to 300% [26]. We have taken the value of *TMR(0)* (*TMR* with 0 bias voltage) as 150% as per latest experimented data and we have modified the equation of R_p accordingly so that it satisfy the equation $TMR_{real} = \frac{(R_{AP}-R_P)}{R_P}$

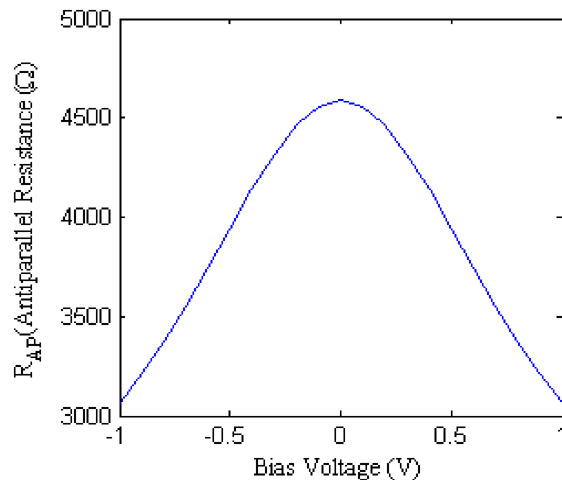

Fig. 2. Effect of bias voltage on antiparallel state resistance.

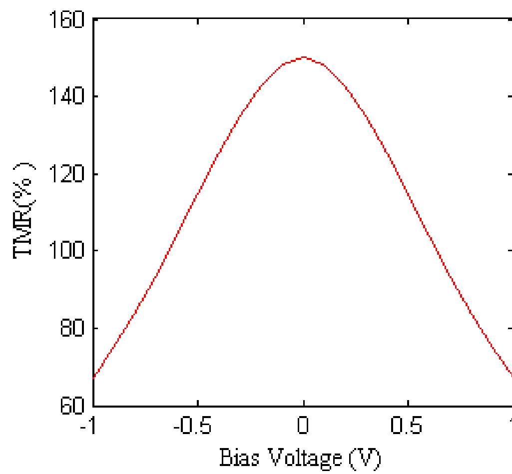

Fig. 3. Effect of bias voltage on TMR.

2.4. Modeling of switching threshold current

Switching occurs in STT-MTJ when current through MTJ exceeds the switching threshold current. The switching threshold current can be expressed as [27]

$$I_c = \frac{\left(\alpha \times \gamma \times e \times \mu_o \times M_S \times H_K \times V\right)}{\left(\mu_B \times g\right)} \tag{4}$$

where α is the magnetic damping constant, γ is the gyromagnetic ratio, e is the electronic charge, μ_0 is the permeability of free space, M_s is the saturation magnetization, H_k is the anisotropy field, V is the volume of the free layer, μ_B is the Bohr magneton, g is the spin polarization efficiency. Their default values are given in Table 1.

Table-1. MTJ model parameters.

Parameters	Description	Value
H_k	Anisotropy field	113.0×103 A/m
M_s	Saturation Magnetization	456.0 ×103 A/m
α	Magnetic damping constant	0.027
e	Electronic charge	1.6× 10-9 C
μ_B	Bohr Magneton	9.274× 10-24 J/T
μ_0	Permeability in free space	1.2566 ×10-6 H/m
P	Spin polarization of the tunnel current	0.56
θ	Angle between the Magnetization of the free and reference layer	θ = 0 for parallel magnetization and θ = π for antiparallel magnetization.
t_{CoFeB}	Free layer height	1.3 nm
t_{ox}	Oxide layer height	0.85 nm
Area	Area of MTJ surface	40 nm × 40 nm × π /4
TMR(0)	TMR with 0 voltage bias	150%
V_{bias}	Biasing Voltage	0.9 V
R_p	Parallel state resistance	1.84 kΩ
R_{ap}	Antiparallel state resistance	4.5 at (0 bias voltage) 3.2 at (0.9 V bias voltage)
I_{CPtoAP}	Switching Current from parallel to antiparallel state	27.2 µA
I_{CAPtoP}	Switching Current from antiparallel to parallel state	-19.2 µA

Spin polarization efficiency can be obtained by the following equations defined in [28].

$$g = g_{sv} \pm g_{tunnel} \tag{5}$$

where the sign is dependent on the free-layer alignment, g_{sv} and g_{tunnel} are the spin polarization efficiency values in a spin valve and tunnel junction nanopillar, respectively. They both are predicted by Slonczewski, i.e.

$$g_{sv} = \left[-4 + \frac{\left(P^{-\frac{1}{2}} + P^{\frac{1}{2}}\right)^3 (3 + \cos\theta)}{4} \right]^{-1} \quad (6)$$

$$g_{tunnel} = \frac{p}{2 \times (1 + P^2 \cos\theta)} \quad (7)$$

where P is the spin polarization percentage of the tunnel current, and θ is the angle between the magnetization direction of the free and fixed layers [2].

There are several ways to reduce the critical switching current density. As it is seen from equation, the critical current density J_c can be reduced by using materials with a low saturation magnetization M_s and/or a high spin polarization efficiency g. Recent experiments showed that CoFeB is one of the most promising materials for this purpose [26]. Besides that, J_c can be improved if volume of the free layer is decreased. We have used lower value of area (taken from latest experimental data) of free layer of MTJ and found J_c to be decreased.

2.5. Time domain analysis of MTJ model

In this section we show time domain analysis of MTJ. This analysis gives the view that how the resistance state of MTJ changes with respect to time when specific input (current in this case) is changed. It gives the dependence of MTJ resistance on input current over time characteristics (Fig. 4). When the input current is changed from 0 to 27.2 μA in a positive direction, the MTJ resistance is changed from 1.84 kΩ (parallel state resistance) to 3.2 kΩ (antiparallel state resistance). After a time delay, when the input current is changed from 27.2 μA to 0, the value of the MTJ resistance remains unaltered. That is, MTJ shows its nonvolatility. When the input current is changed from 0 to −19.2 μA in a negative direction, the MTJ resistance is changed from 3.2 kΩ (antiparallel state resistance) to 1.84 kΩ (parallel state resistance). MTJ retains this resistance value even if the applied negative current is withdrawn. Thus, MTJ proves its nonvolatility and hence can retain data even if the power supply goes OFF.

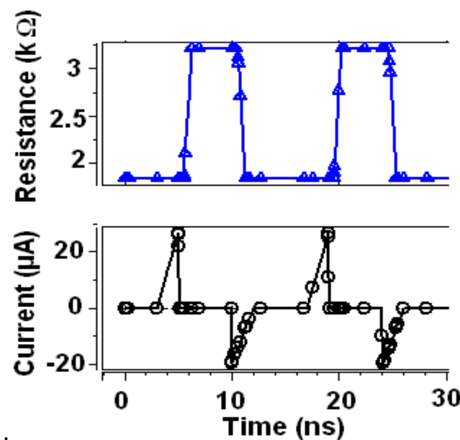

Fig. 4. Dependence of MTJ resistance on input current over time characteristics.

2.6. Hysteresis characteristics of MTJ

MTJs are two-terminal current-controlled device. It has hysteresis nature. The state of an MTJ flips when sufficiently high current passes through the device. The MTJ can be in either parallel state or antiparallel state. When the current through the device exceeds the critical switching current, the state of the device is changed [13]. From Fig. 5, it can be observed that hysteresis characteristic of MTJ begins when write current through MTJ exceeds -19.2 µA tending to zero and ends when write current exceeds 27.2 µA. The MTJ changes its resistance from 1.8 kΩ to 3.2 kΩ when $I_{C(P\text{-}AP)}$ exceeds 27.2 µ. Further increase in current followed by reduction of current to zero value does not affect the resistance state. It remains in that state until the write current falls below -19.2 µA. This shows hysteresis characteristics of MTJ.

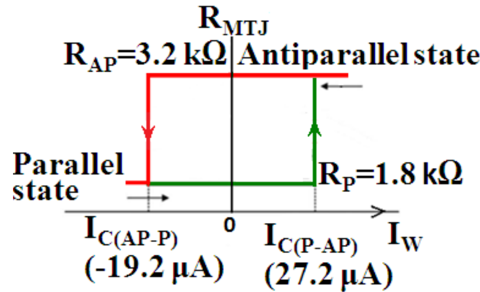

Fig. 5. MTJ hysteresis characteristics.

3. Validation of MTJ Model Using 2-NMOS 1-MTJ Based MRAMs Bitcell.

This section presents the proposed design of MRAM bitcell which is simulated to validate our proposed model. It also describes operating principle of proposed MRAM bitcell.

3.1. Proposed design

Our MRAM cell consists of 1-MTJ, 2-NMOSFETs, two Wordlines (WL_R and WL_W), and a source line (SL) and a bit line (BL). The spintronics device is connected at the bottom of the transistors with its pinned (fixed) layer connected to the source line (SL). The free layer is connected to the common sources of two transistors. Word line WL_R is connected to the gate of the MN1 and Wordline WL_W is connected to the gate of MN2. Bitline (BL) is connected to the drains of MOSFETs (see Fig. 6).

3.2. Design principle in a flow chart method

Design principle of our proposed work is shown in a flow chart method. As described in Fig. 7, first we model MTJ parameters like R_p, R_{ap}, I_{cptoap} and I_{captop}. We propose a Verilog-A MTJ model with these MTJ parameters. Using this proposed MTJ model we design a MTJ-CMOS hybrid MRAM bitcell. We evaluate Read Margin, Write Margin and analyse variability of read current. So our proposed MTJ model proves its suitability in designing MTJ based memory and logic circuit.

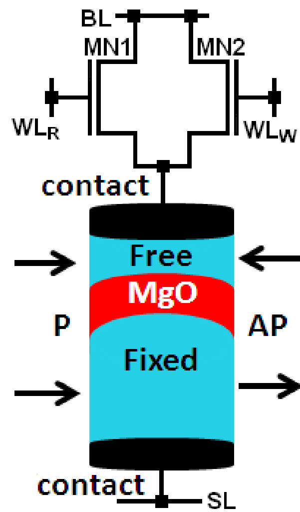

Fig. 6. 2-NMOS 1-MTJ based MRAM circuit.

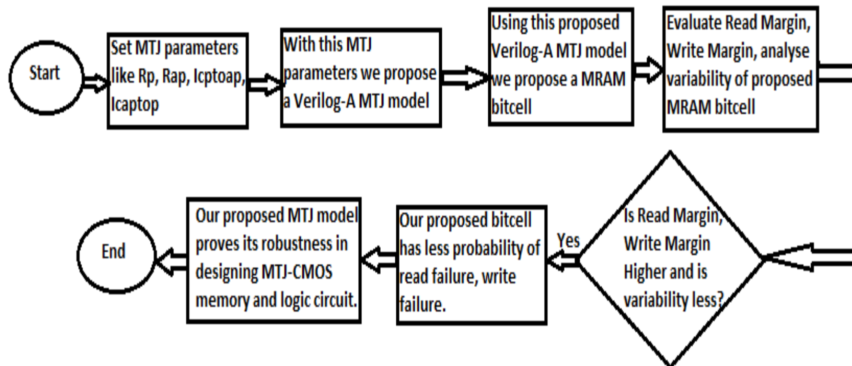

Fig. 7. Flowchart of design principle.

3.3. Read Margin (RM) analysis

When read operation is done the sensed parameter (i.e. current passing through the MTJ) is compared to a reference value which determines the state of the cell.
Read margin is defined as the relative difference between the reading point and the trip point (switching threshold) [15]. When the MTJ is in AP state, read margin is defined as

$$RM_{AP} = (I_{HL} - I_{RAP}) \tag{8}$$

where I_{RAP} is the mean read current (when MTJ is in AP state), and I_{HL} is the nominal high-to-low switching threshold current (i. e., when FL switches from AP →P direction).
Similarly, when the MTJ is in P state, read margin is defined as

$$RM_P = (I_{LH} - I_{RP}) \tag{9}$$

where I_{RP} is the mean read current (when MTJ is in P state), and I_{LH} is the nominal low-to-high switching threshold current (i. e., when FL switches from P →AP direction). MRAM bitcell to be read-fail-safe, both of its read margins should be negative in sign and as large as possible in magnitude.

When a cell is read which is storing "1", the associated current of MTJ is measured and compared with reference value. If the current is so high that it is larger than the switching threshold current of MTJ, then the cell flips, resulting in read failure. Read failure can be avoided if read margin is higher. However, to increase read margin (for reducing read disturbance failure), read current should be reduced [15].

We simulated our 2-NMOSFETs based bitcell with 35 nm device width @ 0.9 V and @27℃ for estimation of read current and read margin with varying pulse width in P state and AP state (see Figs. 8 and 9). As can be observed, the read current decreases with increase in pulse width. However, read margin increases with increase in pulse width.

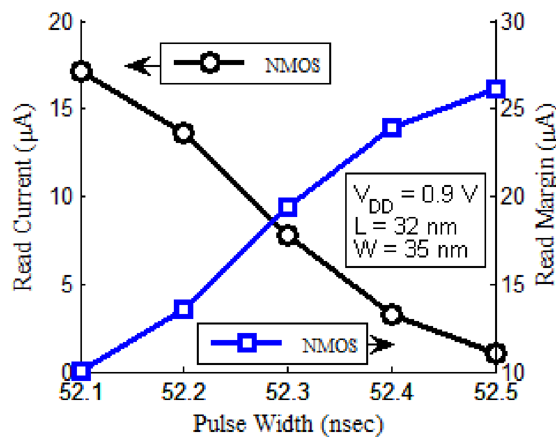

Fig. 8. Read margin and read current analysis of MRAM bitcell at P state.

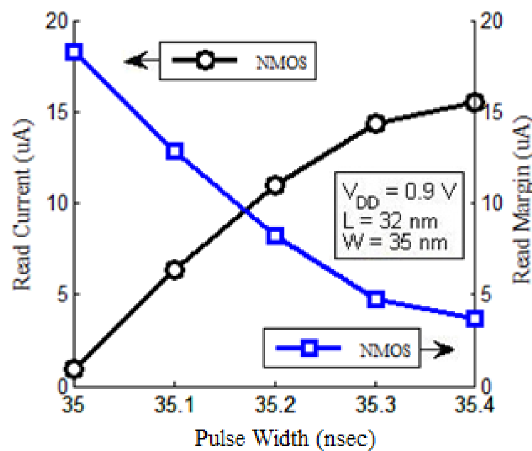

Fig. 9. Read margin and read current analysis of MRAM bitcell at AP state.

3.4. Write Margin (WM) analysis

We can measure write-ability by write margin (WM) which is the difference between the write current and the trip point (switching threshold).

When the MTJ is in P ("0") state and it switches from P to AP state, then the write margin is given by

$$WM_{(P \to AP)} = (I_{W(P \to AP)} - I_{LH}) \tag{10}$$

where $I_{W(P \to AP)}$ is the mean write current (when MTJ switches from P to AP state), and I_{LH} is the nominal low-to-high switching threshold current.

Similarly, when the MTJ is in AP ("1") state and it switches from AP to P state, then the write margin is given by

$$WM_{(AP \to P)} = (I_{W(AP \to P)} - I_{HL}) \tag{11}$$

where $I_{W(AP \to P)}$ is the mean write current when MTJ switches from AP to P state, and I_{HL} is the nominal high-to-low switching threshold current.

Write failure occurs if the write current is less than the nominal switching threshold current. Suppose a bitcell is in '0' state and we want to write '1' to it, then we have to bias the bitcell for parallel to antiparallel switching and the current passing through the bitcell should be higher than the switching threshold current in P to AP direction otherwise the bitcell will remain in the same state. If the write margin is higher, better is the write-ability. There are two methods by which we can improve write margin: firstly, by increasing write current; and secondly, by decreasing nominal write threshold current [15]. We simulated our 2-NMOSFETs based bitcell with 35 nm device width @ 0.9 V and @27 °C for estimation of write current and write margin with varying pulse width in P to AP switching and AP to P switching (see Figs. 10 and 11). As can be observed, write current and write margin increase with increase in pulse width.

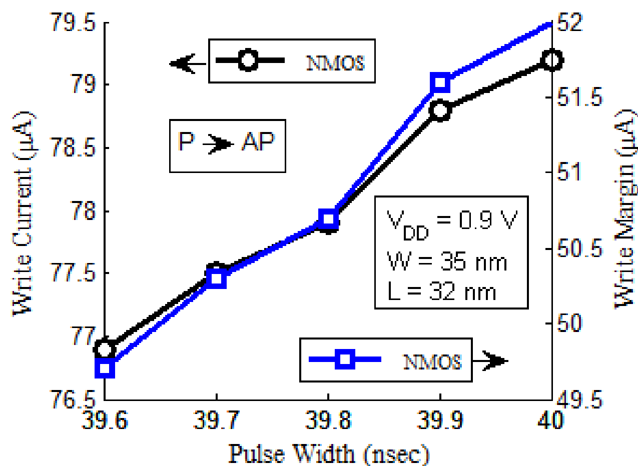

Fig. 10. Write margin and write current analysis of MRAM bitcell at P to AP direction.

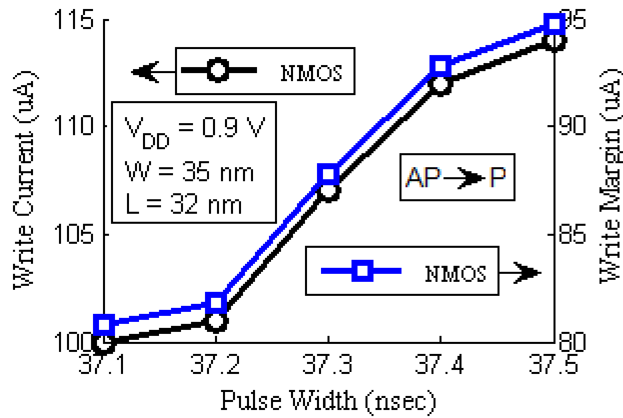

Fig. 11. Write margin and write current analysis of MRAM bitcell at AP to P direction.

3.5. Variability analysis of read current and write current of MRAM bitcell at different supply voltage

Aggressive device dimension scaling has made devices prone to PVT (Process, Supply voltage and Temperature) variations thereby causing variation in device current and circuit performance. PVT variations affect threshold voltage of device thereby varying the drain to source current (I_{ds}).Therefore, it is very important for a bitcell to have less variability in read current and write current to have robust cell performance because read current and write current directly affect design metrics such as read margin, write margin, read failure and write failure. We performed variability analysis of read current and write current of 2-NMOSFET based bitcell (See Figs.12 and 13). As can be observed, the read current variability and write current variability vary less about the nominal supply voltage of V_{DD} = 0.9 V.

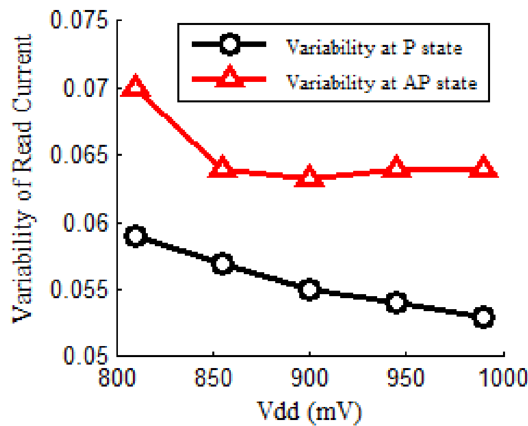

Fig. 12. Variability analysis of read current at P and AP state

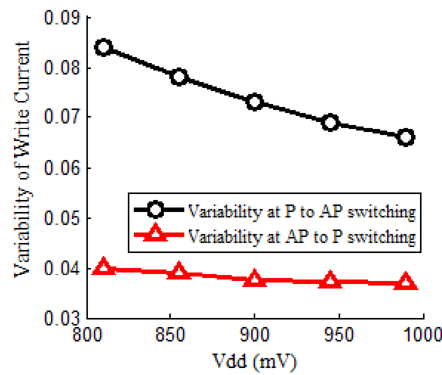

Fig. 13. Variability analysis of write current at P to AP switching and AP to P switching.

4. Comparison of Proposed MTJ Model with Existing Model

MTJ switching threshold current is a critical parameter of MTJ-CMOS hybrid circuit because it affects read margin and write margin which further affect read failure and write failure probability of a bitcell. Very high switching threshold current implies that a very high write current is needed for the cell to flip. This also increase write failure probability. Moreover, higher write current results in higher power dissipation during write operation. Lower critical switching current allows power saving which is beneficial for magnetic memory and logic circuit applications [29]. The proposed MTJ model and the bitcell require lower switching threshold current. The proposed MTJ model is compared with an MTJ model presented in [2] in terms of switching threshold current.

Table 2. Comparison of switching threshold current

Parameter	Proposed MTJ Model	Existing MTJ Model [2]
I_{LH}	*27.2 μA*	*72.22 μA*
I_{HL}	*-19.2 μA*	*-27.88 μA*

5. Conclusions

This paper presents a behavioral model of MTJ which is developed using latest experimental data. Our proposed MTJ model is employed to design MRAM bitcell for validating its versatility. The proposed MTJ model is compatible with CMOS technology for nanoscale MRAM design. We validate our model by simulating hybrid CMOS-MTJ MRAM circuit using our proposed model. Various design metrics of MRAM bitcell like read margin and write margin are estimated to verify suitability of our model in designing MRAM bitcell. Results of our analysis agree with the results reported in the literature.

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