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Q FUNCTION AWARE OPTICAL PACKET SWITCH WITH LOW PACKET LOSS RATE

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Abstract

Optical packet switching (OPS) is a very promising technology for the next generation data transfer due to the very large bandwidth of the optical fiber. The success of the OPS relies heavily on design of the node architecture which supports comparatively larger buffering capacity without detiorating signal quality too much and it should provide very low packet loss probability with reasonably low average delay. In this paper, a design analysis of low complexity OPS node architecture is discussed along-with its advantages. The presented architecture support both fixed and variable length packets. The packets are stored in a single piece of fiber using the WDM technology. Physical layer analysis presented in this paper is to obtain the *Q* function (Bit Error Rate). Finally, the Monte Carlo simulation is done to obtain the packet loss. The average delay performance of the switch and effect of *Q* values on packet loss rates are discussed.

Keywords: FDL, FBGs, WDM, TWC.

1. Introduction

Optical packet switching (OPS) is the next generation data transfer technology, where information is transferred in terms of optical packets. The OPS technology utilizes the bandwidth of the optical fiber efficiently using WDM technique [1]. The high speed OPS technology can be used to cater to the growing internet traffic.

Today's optical packet networks are not entirely optical, i.e., referring to Fig. 1, the data goes electrical to optical *E*/*O* when data enter in optical network (edge

Nomenclatures

$a_{ib}(t)$	Arriving packets
B	Buffer Space
$d_{ib}(t)$	Departing packets
G	Gain of the amplifier, dB
L_{Cir}	Loss of Circulator, dB
L_{Com}	Loss of Combiner, dB
L_{FBG}	Loss of Fiber Bragg Gratings, dB
L_{Spl}	Loss of Splitter, dB
L_{Twc}	Loss of TWC, dB
m	Module
N	Size of switch
p	Probability

Greek Symbols

η	Population inversion factor
π	Steady state probability
ρ	Offered load

Abbreviations

EDFA	Erbium Doped Fiber Amplifier
FDL	Fiber Delay Line
PLR	Packet Loss Rate
TF	Tunable Filter
TWC	Tunable Wavelength Convertor
WDM	Wavelength Division Multiplexing

node A) and again converted back in optical to electrical when data exit (edge node B) the optical network, while within the network data remains in optical domain. In nut-shell, optical signals are converted to electrical form before switching and processing. This clearly indicates that the major advantages of optical packet switching, i.e., speed and efficiency, are lost due to the data conversion delay. The biggest problem associated with all optical switching is un-availability of optical RAM. Additionally, very high switching rates needed in packet networks cause problems [2]. In the near future, development seems to lead to integration of optical and electronic networks and the use of optical packet/burst switching.

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The OPS/OBS networks design is complex problems; as there are countless attribute that need to care of in networks [1]. As in the optical network aggregated data packet will traverse therefore, it is mandatory that the packet loss should be

very minimal and signal quality degradation at each node should be minimal so that packets can traverses a large distances in optical networks.

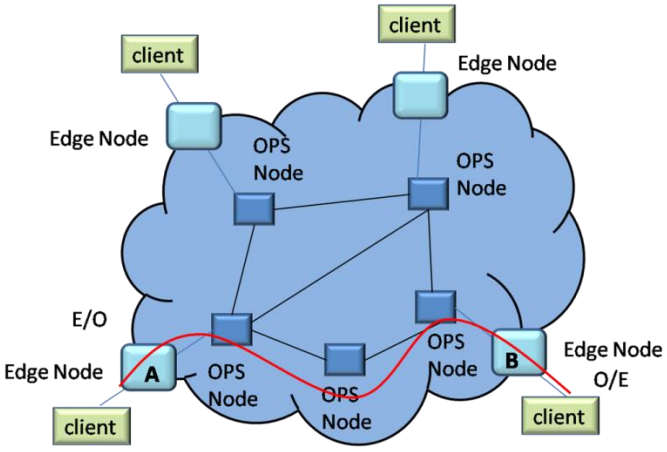

Fig. 1. Generic layout of the optical network.

The basic layout the OPS node is shown in Fig. 2. The OPS node consists of input, output block along-with switching or buffering section. Due to the un-availability of the optical controller the functionality of the switch is controlled by an electronic controller and shown Fig. 2 and thus referred as photonic packet switching [2].

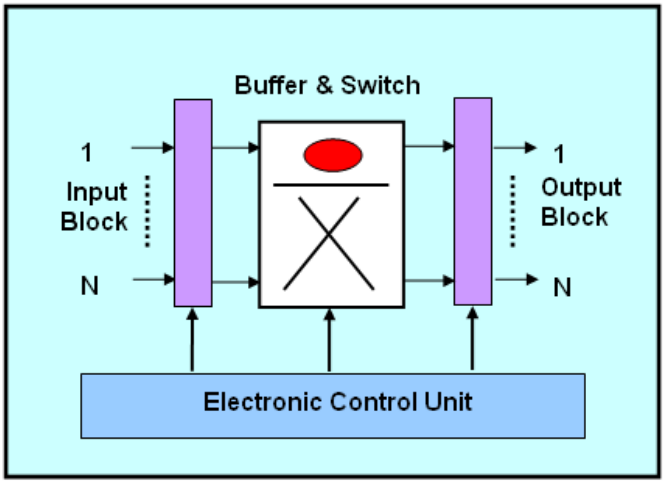

Fig. 2. Generic layout of the optical packet switch.

The important components of photonic packet switching [2] are control, packet routing, packet synchronization, clock recovery, contention resolution, buffering, and packet header replacement. In optical packet switching, buffering will only be required when two or more packets try to occupy the same output

fiber in a single time slot. Then, except one which is directly transmitted towards output, other contending packets are stored within the switch using the fiber delay lines. The use of fiber delay lines is an alternative to the optical RAM. In the considered architecture hybrid scheme which utilizes both Fiber delay line (FDL) and wavelength conversion for contention resolution, is used.

In past many optical packet switch architectures has been proposed and demonstrated. A good review of the photonic packet switching can be found in [2]. The comparative analysis of the optical loop buffer based architecture is presented in [1]. The detailed description of optical packet switches in recent past can be found in [5-10].

The optical switches presented in the past, have their advantages and disadvantages. In the design of the switch architecture the main parameters that are to be considered are low insertion loss, low crosstalk with very less noise components like SOA and EDFA. In many of the architectures presented in past, these parameters are neglected and the performance of the architecture is measured in terms of only network layer parameters like packet loss probability and average delay, however in real scenario these parameters are inter-related.

In this paper, a very simple optical switch design is presented. The architecture presented in this paper has very simplified buffering structure. In the presented switch architecture, once packets are placed in the buffer, they will come out of the buffer after required amount of definite delay, and in the buffering no controlling is required. This architecture can also be easily used in optical burst switching (OBS) where the burst size cannot be known in advance. The description of the OBS and use of this architecture is beyond to the scope of this paper. However, our next paper will discuss the use of this architecture in OBS. Still over here we addressed this to state that the architecture is equally efficient in OPS and OBS.

2. Related Work

In OPS various work is proposed in past, a brief review of the work detailed in this section. He et al. [10] discusses heuristic based offline wavelength assignment mechanism. In this work, QoS is guaranteed by taking care of both BER and latency. He et al. [11] discussed that the quality of an optical signal degrades due to physical layer impairments such as noise crosstalk, etc. as it propagates down the length. As a result, the signal quality at the receiver of may not be within the acceptable limit, leading to increased call blocking.

Josep Sole´-Pareta et al. [12] discussed the accumulation of physical layer impairments on the signal along its optical transparent paths, therefore limiting the system reach and the overall network performance. Mariño et al. [13] discusses the cross-layer planning of optical networks considers physical impairments. Rastegarfar et al. [14] discusses how the Fiber delay lines (FDLs) can be used to realize optical buffer. However, the practical limitation on the number of FDLs in a router requires its ports to be run at low utilization, sacrificing a significant portion of network capacity.

Rest of the paper is organized as follows, in Section 3; description of the architecture is presented and mathematical analysis is done to obtain the loss, power and noise and finally BER. The effect of *Q* function is also discussed, on

switch performance. The queuing analysis of the switch is presented in section 4, simulation results suing the Monte Carlo method is also presented to obtain switch performance in terms of packet loss rate. The major conclusions of the thesis are presented in section 5 of the paper.

3. Architecture Description and Analysis

The switch shown in Fig. 3 is designed for equal length packets and packets arrive synchronously at the input of the switch [15]. This synchronization is necessary for the correct operation of the switch.

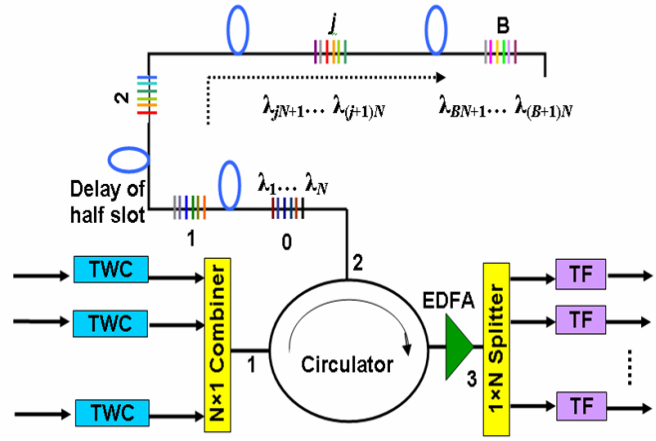

Fig. 3. Layout of the FBG based optical switch.

Considering a $N \times N$, i.e., N inputs and N outputs switch, the FBG marked as '0' reflects wavelength λ_1-λ_N without any delay, and received by output 1 to N respectively. Buffer wavelength ranges from λ_{N+1} - $\lambda_{(B+1)N}$ as shown in Fig. 3. These wavelengths are grouped into the set of N wavelengths. In the buffer, sets of FBGs are placed, and between two consecutive gratings fiber delay line of half of the slot duration is added. These delay lines provide delay of integral multiple of slot duration as each packet pass through each delay line twice, once going in forward direction and once in backward direction after reflection from the grating. The input TWC tunes the wavelengths of the incoming packets as per the desired output and required amount of delay.

Total number of wavelengths used by the switch is $T = (B+1)N$. The number of TWCs at the input is always equal to N, but number of FBGs inside the buffer will depend upon packet loss probability and can be greater or less than N.

In the earlier work, optical buffer is realized using the large number of components as discussed in optic switch based on fiber Bragg gratings [15]. However, in this architecture the buffer is created using Multi-wavelength Fiber Bragg Gratings only. Therefore buffering complexity is reduced significantly. Moreover, in this architecture, fixed as well as variable length packets whose length is integral multiple of smallest size packet can also be stored. This feature makes architecture very unique.

In this architecture for the buffering of '*B*' packets complexity given as Θ(*B*/*N*) where '*N*' are the wavelengths handled by each grating, whereas in earlier architecture [2, 10] it was Θ(*B*). Thus, complexity Θ (*B*/*N*) reduces significantly.

3.1. Power budget analysis

The power budget analysis is necessary to identify the minimum power of the signal which passes through the switch and correctly identified at the switch outputs. In the power budget analysis following steps is as:

1. Calculation of loss when signal passes through the switch,
2. Gain estimation of EDFA,
3. Total signal power received at the output.
4. Noises accumulation within and at the receiver of the switch.
5. Bit Error Rate analysis.
6. At a fix BER of $\leq 10^{-9}$, identification of minimum power levels for different switch and buffer combinations.

3.1.1. Loss analysis

The loss of the input which consists of TWC and combiner is $L_{Com}^{N\times1}L_{TWC}$, the loss of output unit which consists of splitter and TF is $L_{FBG}L_{TF}L_{Cir}L_{TF}^{1\times N}$, and the loss of buffer unit is BL_{FBG}.

Thus the maximum possible loss when a packet passes through the switch is

$$L = L_{TWC}L_{Com}^{N\times1}(B+1)L_{FBG}L_{Cir}L_{Spt}^{1\times N}L_{TF} \quad (1)$$

The loss is compensated by EDFA and *LG*=1, is the condition which maximizes the SNR is assumed. Here, G is the gain of the amplifier.

3.1.2. Power analysis

Again, power entering in buffer module for bit b is

$$P_s = bP_{in}b \in [0,1] \quad (2)$$

The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero. Power at the output of the switch is

$$P_{Out} = P_{in} + P_{sp}$$

$$P_{Out} = bP_{in} + \eta_{sp}(G-1)h\nu B_o L_{Spt}^{1\times N}L_{TF} \quad (3)$$

The term$\eta_{sp}(G-1)h\nu B_o$represents the ASE noise of the EDFA amplifier.

3.1.3 Noise analysis

Due to square law detection by the photo detector in the receiver, various noise components are generated. These noise components are shot noise, ASE-ASE beat noise, sig-ASE beat noise, shot-ASE beat noise and thermal noise variances

are denoted by σ_s^2, σ_{sp-sp}^2 , σ_{sig-sp}^2, σ_{s-sp}^2 and σ_{th}^2 respectively [16]. For the bit b the different noise components in the receiver area

$$\sigma_s^2 = 2qRPB_e$$

$$\sigma_{sp-sp}^2 = 2R^2P_{sp}(2B_o - B_e)\frac{B_e}{B_o^2}$$

$$\sigma_{sig-sp}^2 = 4R^2P\frac{P_{sp}B_e}{B_o} \ , \sigma_{s-sp}^2 = 2qRP_{sp}B_e$$

$$\sigma_{th}^2 = \frac{4K_BTB_e}{R_L} \tag{4}$$

The total noise variance for bit b is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sp}^2 + \ \sigma_{s-sp}^2 \ + \sigma_{th}^2 \tag{5}$$

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right) \tag{6}$$

$$Q(z) = \frac{1}{\sqrt{2\pi}}\int_z^{\infty} e^{-\frac{z^2}{2}}\,dz \tag{7}$$

where $I(1) = RP(1)$ and $I(0) = RP\ (0)$ are photocurrent sampled by receiver during bit 1 and bit 0 respectively, and R is responsivity of the receiver.

3.2. Calculations

Using the above formulation and the values of the parameters as given in Table 1, the results obtained in terms of BER at different power levels for different buffering condition for fixed input switch size is presented in Tables 2-3. For a switch of size 4×4, for the buffering capacity of 8 packets for each output, BER at different power levels is presented in Table 2.

Table 1. List of parameters and their value [10].

Parameters	Value
Size of the switch	4,8
Population inversion factor	1.2
Speed of light	3×10^8m/s
Loss of FBG	1 dB
Responsivity	1.28 A/W
Electronic charge	1.6×10^{-19}C
Optical bandwidth	40GHz
Electrical bandwidth	20GHz
TWC insertion loss	2.0 dB
Loss of AWG (32 channels)	3.0 dB
Loss of the fiber loop	0.2 dB/Km
Loss of Circulator	1.0 dB

It is clear from the table that as the power increases the BER performance of switch improves significantly. For the acceptable BER$\leq10^{-9}$, the minimum power level is nearly 400 nano-watts, which is much lesser in comparison to earlier

switch loop buffer based design where a power level of ~ milli watts is required for same performance. In recent past, AWG based switch is heavily investigated due to lesser power requirements of micro-watts levels. Thus in terms of power required, the presented switch performs better in comparison to recently published switch designs. In recent past, some questions have been raised on the higher power requirements in optical switch in comparison to electrical switches [17], as in electrical chips power requirement is some tens of nano-watts. Thus the presented switch is at par with electrical switch in terms of power requirements.

Table 2. Switch size 4×4, and buffer 8.

Power in nano-watts	BER
100	0.0074
200	4.7370×10^{-5}
300	2.6539×10^{-7}
400	1.3485×10^{-9}
500	6.3780×10^{-12}
600	2.8553×10^{-14}
700	1.2234×10^{-16}
800	5.0568×10^{-19}
900	2.0278×10^{-21}
1000	7.9243×10^{-24}

For a switch of size 4×4, for the buffering capacity of 16 packets for each output the BER at different power levels is presented in Table 3.For such a switch combination the required amount of power for successful operation is higher in comparison to buffering of 8 packets. It is again noticeable from the table that as the power increases the BER performance of switch improves. For the acceptable BER$\leq10^{-9}$, the minimum power level is now nearly 900 nano-watts, thus as the buffer size increases the power requirements also increases.

Table 3. Switch size 4×4, and buffer 16.

Power in nano-watts	BER
100	0.0731
200	0.0062
300	5.6240×10^{-4}
400	5.0682×10^{-5}
500	4.5318×10^{-6}
600	4.0148×10^{-7}
700	3.5247×10^{-8}
800	3.0688×10^{-9}
900	2.6517×10^{-10}
1000	2.2756×10^{-11}

Physical layer impairments can limit the ports and buffering of switch [8, 10]. *Q*-factor a measure of packet signal quality and for optical system the acceptable BER$\leq10^{-9}$the value of *Q* is 6. Thus the *Q* factor has an impact of packet drops can in turn limits the maximum achievable throughput. Thus it becomes important to investigate physical layer parameters effect for optimizing the router performance.

It is expected that in most of the optical application, BER≤10^{-9} will be required; however, in some application BER≤10^{-12} may be desirable. Therefore, in *Q* function analysis both BER descriptions are considered.

In Fig. 4, *Q* function vs. Buffer space is plotted for *N*=4 and *B*=8 at the power level of 500,700 and 900 nano-watts. At the power level of 700 nW, BER≤10^{-12} can be achieved for the buffering capacity of ≤7.Similarly, at the power level of 300 nW, BER≤10^{-9} can be achieved for the buffering capacity of ≤4. However at the power level of 500 nW, full buffer capacity can be utilized for BER≤10^{-9}, but only buffering of 2 packets is permissible for BER≤10^{-12}.

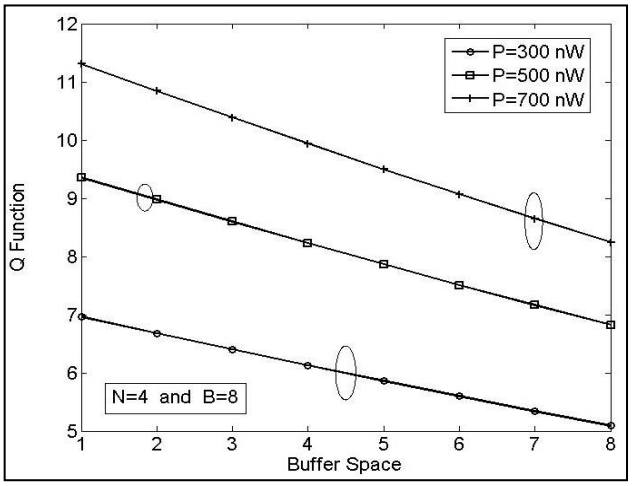

Fig. 4. *Q* function vs. buffer space (*Q*(6)=10^{-9} and Q(9)=10^{-12}).

4. Queuing Analysis of the Switch

The packet arriving at the switch inputs are either directly transmitted to output ports or put in the buffer as a separate queue as shown in Fig. 5, in case of contention. These arriving packets for different output are dropped at the input of the switch, when buffer for individual output port is full, or packet cannot be stored due to the *Q* function reached its allowed minimum threshold value.

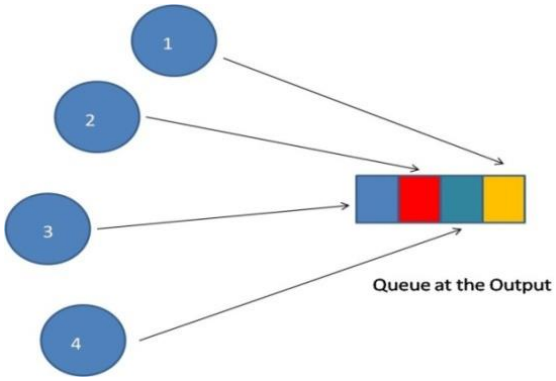

Fig. 5. Queuing structure of the output buffer.

The number of packets $P_i(t)$ stored in the buffer, for a particular output port i, in any time slot t is a random variable and depends on the arriving traffic distribution, and can be expressed as

$$P_i(t) = P_i(t-1) + a_{ib}(t) - d_{ib}(t) \tag{8}$$

In this expression $P_i(t\text{-}1)$ is the number of packets already stored in the loop buffer at the end of time slot (t-1), $a_{ib}(t)$ denotes the number of packets arriving and scheduled for buffering in the (t^{th}) time slot, and similarly $d_{ib}(t)$ are the number of packets that leave the buffer in the (t^{th}) time slot.

The eq. 8 can be simplified by considering the fact that, $d_{ib}(t)$ =1, because for a given output port only one packet will leave the buffer in any time slot.

$$P_i(t) = P_i(t-1) + a_{ib}(t) - 1 \tag{9}$$

The total numbers of packets stored in the buffer, in any time slot t are

$$P(t) = \sum_{i=0}^{N} P_i(t) \tag{10}$$

If in any time slot

$$P(t) > B \tag{11}$$

Then, $\Delta = P(t) - B$ have to be dropped at the input of the switch. Here B is the allowed buffer space.

If in any time slot, due to the Q value constraints only $K<B$ can be stored and if

$$P(t) > K \tag{12}$$

Then again packets have to be dropped at the input of the switch. The number of lost packets $L_i(t)$ for a particular output is

$$L_i(t) = P_i(t-1) + a_{ib}(t) - 1 - K \tag{13}$$

However, using the higher power levels, the 'Q' value constraints can be relaxed and eq. 13 can be modified as

$$L_i(t) = P_i(t-1) + a_{ib}(t) - 1 - B \tag{13}$$

It is customary to note that in the above expression the loss $L_i(t)$ is a random variable and depends on the statistics of arriving packets. We assume identical Bernoulli process for traffic generation. That is, in any time slot, probability of the arrival of packet on a particular input port is 'p' and each packet has equal probability 1/N of being addressed to any one of 'N' outputs.

Defining a random variable 'X' as the number of packet coming for a particular tagged output in a given slot, the probability that exactly 'q' packets will arrive in a slot is

$$P_q = P_r[X = q] = {}^{N}_{q}C \left(\frac{p}{N}\right)^{q} \left(1 - \frac{p}{N}\right)^{N-q} \text{where } 0 \le q \le N \tag{14}$$

The Markov chain model for the loop buffer is shown in Fig. 6, and the state transition probability P_{ij} can be written as

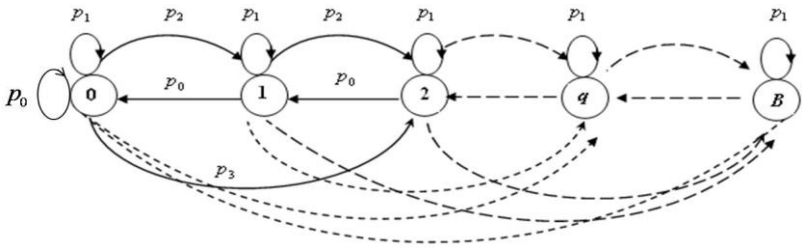

Fig. 6. Description of Markov chain model.

$$P_{ij} = \begin{cases} p_0 + p_1 & i = 0,\ j = 0 \\ p_0 & 1 \le i \le B,\ j = i - 1 \\ p_{j-i+1} & j - N + 1 \le i \le j - 1,\ 1 \le j \le B - 1 \\ \sum_{m=j-i+1}^{N} p_m & j = B,\ 0 \le i \le j \\ 0 & otherwise \end{cases} \quad (15)$$

The steady state distribution of the Markov chain can be obtained as $\pi P_{ij} = \pi$.

where, $\pi = [\pi_0\, \pi_1 \pi_2 \pi_3 - - - - \pi_B]^T$ is the steady state distribution of the different states. The vector π should satisfy the following condition. $\sum_{i=1}^{B} \pi_i = 1$

If we define normalized throughput ρ_0, then

$$\rho_0 = 1 - \pi_0 p_0 \quad (16)$$

The packet success probability can be obtained by dividing ρ_0 by ρ. Here ρ is the offered load. Then packet loss probability can be obtained as

$$P_r[Packet\ Loss] = 1 - \frac{\rho_0}{\rho} \quad (17)$$

To obtain results Monte Carlo simulation were performed for 10^6 time slots in the steady state.

In Fig.7, packet loss probabilty vs. Load is plotted for N=4, with Q function constraints as in Fig. 4. As per Fig. 4, at different BER requrements the allowed buffering space is 2,4,7 and 8. From this figure it is clear that the loss probability heavily dependenton buffer space. At the load of 0.6, for buffering capacity of 2,4,7 and 8, the loss probability is 2×10^{-2}, 1.5×10^{-3}, 3×10^{-5} and 1×10^{-5} respectively. Thus by increasing buffering capacity from 2 to 8, the loss probability improved by a factor of 1000. From Figs. 4 and 7, it can be concluded that to fully utilized buffering capacity higher Q value is needed, thus higher power level can be used. But it must be remembered that power cant be arbitrarily

high as higher power (~mW) non-linear effect of fiber starts to dominate and reduces *Q* value [10]. From the above it can be deduced that, maximum permissible power for any switch is of the order of *mW*.

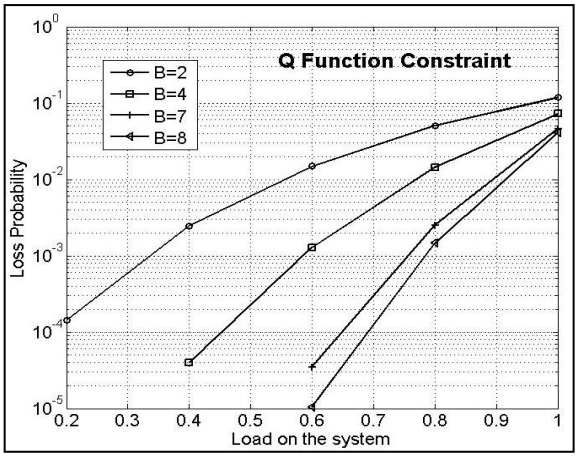

Fig. 7. Loss probbilty vs. load as *Q* function constraint.

In most of the optical communication base system the desired PLR is (Packet Loss Rate) $\leq 10^{-5}$. In Fig. 8, PLR vs. load is plotted for switch of size N=4 for different buffering capacity B=4, 8 and 16. It is clear from figure that, for B=8, the desired *PLR* can be achieved till the load 0.6,which can be further increase to a load of 0.8, for the buffering of 16 packets.

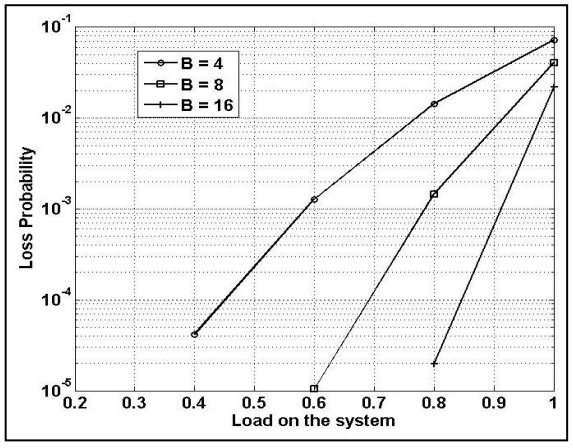

Fig. 8. Loss probbilty vs. load on the system.

In Fig. 9, PLR vs. load is plotted for switch of size N=16 for different buffering capacity B=4, 8 and 16. This graph is produced to compare this architecture with recently published AWG based architecture, where $PLR \leq 10^{-5}$ for N=16 is obtained till a load of 0.6, which is much higher and up to a load of 0.75 in our switch.

Thus, the presented architecture is very efficient in terms of power requirements and packet loss rate.

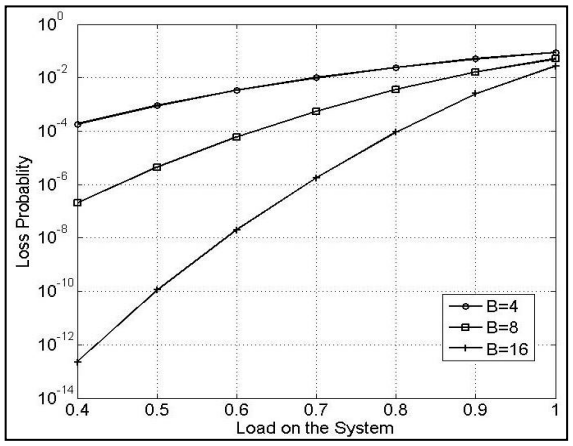

Fig. 9. Loss probability vs. load on the system for *N*=16.

5. Conclusions

In this paper a simple FBG based optical packet switch design is presented and it is shown that FBG can be effectively utilized to create buffer. In this paper Q function aware based optical switch design is presented and analysed. The switch can be efficiently used at some fraction of micro-watts power.

From this work, following conclusions can be made:

- The presented switch can operate in sub-micron power levels.
- *Q* function is heavily depends on the loss and noises of the system.
- In this architecture very low PLR$\leq 10^{-5}$ available till load 0.75.
- Low *Q* value restricts the full usage of the buffer space.

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