NEW ELECTRONICALLY TUNABLE GROUNDED INDUCTOR SIMULATOR EMPLOYING SINGLE VDTA AND ONE GROUNDED CAPACITOR

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Abstract

In this paper a new grounded inductor simulator employing single voltage differencing transconductance amplifier (VDTA) and one grounded capacitor has been proposed. The proposed circuit is electronically controllable and exhibits low parasitic effects. The performance of proposed inductor simulator is demonstrated by SPICE simulations with TSMC CMOS .18 µm process parameters.

Keywords: Grounded inductor simulator, Electronic control, VDTA, Grounded capacitor, Active inductor.

1. Introduction

The Inductor is an integral part of many analog circuits such as filters, oscillators, phase shifters etc. A conventional spiral inductor has several drawbacks such as large size and weight, generates unwanted harmonics of the signals due to saturation of its core, picks as well as radiates electromagnetic waves etc. Its quality factor and liner dimensions are directly proportional to each other. Hence, it is not possible to design a small size inductor with high quality factor. Therefore, in last three decades, attention is extensively focused on active simulation of inductors. Numerous actively simulated grounded inductor configurations employing different active building blocks such as operational amplifiers (Op-amp)[1-4], current conveyors (CC) [5], Op-amps[6], voltage current conveyors(DVCC)[7], CC[8], Op-amp[9], CCs [10-16], Current feedback-
Nomenclatures

\( C_A, C' \)  
Equivalent capacitances, \( \mu \text{F} \)

\( C_{0}, C_{1}, C_{2} \)  
External capacitances, \( \mu \text{F} \)

\( C_P \)  
Parasitics capacitance at “P” port of VDTA, pF

\( C_N \)  
Parasitics capacitance at “N” port of VDTA, pF

\( C_{X+}, C_{X-} \)  
Parasitics capacitance at “X+” “X-” port of VDTA, pF

\( C_Z \)  
Parasitics capacitance at “Z” port of VDTA, pF

\( g_{m1}, g_{m2} \)  
Transconductance gains of VDTA, \( \mu \text{A/V} \)

\( g_m \)  

\( I_{b1}, I_{b2} \)  
Bias currents of VDTA, \( \mu \text{A} \)

\( I_{b1}, I_{b2}, I_{b3} \)  

\( I_{X+}, I_{X-}, I_{Z} \)  
Currents at “X+”, “X-”, “Z” port of VDTA, mA

\( L, L_{eq}, L_{Gh} \)  
Equivalent inductances, \( \mu \text{H} \)

\( R_1, R_{eq} \)  
External resistance, k\( \Omega \)

\( R, R_{eq}, R_P, R_N, R_X \)  
Equivalent resistances, k\( \Omega \)

\( \beta_{x+}, \beta_{x-}, \beta_{z} \)  
Output stage tracking error (at port X+), (at port X-), (at port Z) of VDTA

\( \omega_1, \omega_2 \)  
Pole frequencies, MHz

\( \tau_1, \tau_2 \)  
Time delays, \( \mu \text{s} \)

Abbreviations

CC  
Current conveyors

CDTA  
Current differencing transconductance amplifier

CFOA  
Current feedback operational amplifiers

CMOS  
Complementary metal oxide semiconductor
operational amplifiers (CFOA)[17-19], current differencing trans-conductance amplifiers (CDTA)[20], four terminal floating nullors(FTFN)[21], Current Follower transconductance amplifier (CFTA)[22], Fully Differential Second-Generation Current Convoyor (FDCCII )[23], Voltage differencing differential input buffered amplifiers(VDDIBA)[24]. Dual output Differential Difference current convoyer (DO-DDCC)[25], CFOA[26], Dual-X current convoyer (DX-CCII)[27-28], Operational trans-conductance amplifiers(OTA)[29], Differential difference current convoyer(DDC)[30],operational trans-resistance amplifiers(OTRA)[31], voltage differencing transconductance amplifiers (VDTA)[32], Voltage differencing buffered amplifiers(VDBA )[33] and Voltage differencing current conveyors(VDCC)[34] have been proposed in the literature. Unfortunately, all of the reported circuits suffer from one or more of following drawbacks:

(i) Excessive (more than one) use of the active components [1], [6], [7], [9], [12], [14-16], [18], [20], [22], [24], [31].

(ii) Excessive(more than one) use of the passive components [1-3], [5], [6], [8-11], [13], [15], [17-19], [21-23], [25-31], [33-34].

(iii) Partial utilization of active component(s) [7], [9], [18], [23], [29], [32-34].

(iv) Use of floating passive component(s) [1-11], [13], [15-19], [21], [25-31], [33].

(v) Lack of electronic controllability [1-6], [8-11], [13-19], [21], [23], [25-31].

(vi) Requirement(s) of external passive component matching constraints [1-3], [8], [10-11], [13], [21], [27], [30-31].

(vii) High parasitic effects [24], [32-33].

Therefore, the purpose of this communication is to propose a new grounded inductor simulator circuit composed of minimum active and passive components (single VDTA and one grounded capacitor) with following advantageous features: (i) use of a grounded capacitor, (ii) availability of electronic control, (iii) no requirement of any external passive component matching constraint (iv) full utilization of VDTA and (v) low parasitic effects.

2. Proposed Grounded Inductor Simulator

VDTA [35-36] is a versatile active element finds several applications in analog filter designing [37-39], oscillators [40] and inductor simulators [41]. The schematic symbol of the VDTA and CMOS implementation of VDTA are shown in Fig. 1 and Fig.2 respectively, where P and N are input terminals and Z, X+ and
X- are output terminals. All terminals of VDTA exhibit high input impedance values. The terminal characteristics of VDTA can be described by:

$$\begin{bmatrix}
I_x^- \\
I_x^+ \\
I_x^-
\end{bmatrix} =
\begin{bmatrix}
g_{m_1} & -g_{m_1} & 0 \\
0 & 0 & g_{m_2} \\
0 & 0 & -g_{m_2}
\end{bmatrix}
\begin{bmatrix}
V_{Gp} \\
V_{Gn} \\
V_Z
\end{bmatrix}$$  \hspace{1cm} (1)

![Fig. 1. The schematic symbol of VDTA.](image1)

The proposed grounded inductance circuit is shown in Fig. 3. A routine analysis of this circuit yields the following expression for its input impedance:

$$Z_{in} = \frac{sC_0}{g_m^2}$$  \hspace{1cm} (2)

with \( g_{m_1} = g_{m_2} = g_m \)

Thus the circuit simulates a lossless grounded inductor with inductance value.

$$L_{eq} = \frac{C_0}{g_m^2}$$  \hspace{1cm} (3)

which is electronically tunable by \( g_m \).
The condition $g_m = g_m = g_m$ can be easily achieved in practice by equating the two bias currents of VDTA and does not require any external passive component matching.

![Diagram of grounded inductor simulator configuration](image)

**Fig. 3. Proposed grounded inductance simulator configuration.**

3. **Non-ideal analysis and effects of Parasitics**

In the non-ideal case, the VDTA can be characterized by the following equations

\[ I_x = \beta_x g_m (V_p - V_n) \]  
\[ I_{x+} = \beta_{x+} g_m V_Z \]  
\[ I_{x-} = -\beta_{x-} g_m V_Z \]

where $\beta_x, \beta_{x+}$ and $\beta_{x-}$ are voltage tracking errors.

Under non ideal conditions the input impedance of circuit proposed in figure 3 is given by

\[ Z_{in} = \frac{g_m (\beta_x - \beta_{x+}) + sC_0}{g_m^2 \beta_x \beta_{x+}} \]  

Therefore, the circuit simulates a grounded series $R - L$ circuit rather than a pure grounded inductor at low frequencies.

where

\[ R = \frac{(\beta_x - \beta_{x+})}{g_m^2 \beta_x \beta_{x-}} \]  

and

\[ L = \frac{C_0}{g_m^2 \beta_x \beta_{x-}} \]

To evaluate the high frequency performance, the proposed grounded inductor is investigated under the influence of VDTA. $X+$ port parasitic impedance consisting of a capacitor $C_{xs}$ in parallel with resistance $R_{xs}$. $X-$ port parasitic
impedance consisting of a capacitor $C_x$ in parallel with resistance $R_x$. P port parasitic impedance consisting of a capacitor $C_P$ in parallel with resistance $R_P$. N port parasitic impedance consisting of a capacitor $C_N$ in parallel with resistance $R_N$ and Z port parasitic impedance consisting of a capacitor $C_Z$ in parallel with resistance $R_Z$. The expression of non ideal input impedance of proposed configuration is found to be:

$$Z_{in} = \left( \frac{1}{R_x} + \frac{1}{R_y} + sC_x + sC_Z + sC_N + sC_X \right) \frac{1}{g_m}$$

(10)

where $g_m = g_{m_x} = g_{m_z}$.

The non ideal equivalent circuit of proposed grounded inductor simulator shown in Fig. 3 is given in Fig. 4.

Fig. 4. Non ideal equivalent circuit of proposed grounded inductor simulator.

where

$$R_A = \frac{\left( \frac{1}{R_x} + \frac{1}{R_y} \right) g_m}{g_m}$$

(11)

$$L_A = \frac{(C_0 + C_Z + C_Y)}{g_m}$$

(12)

$$C_A = C_R + C_X$$

(13)

The grounded inductor simulator proposed in [32] as shown in Fig. 5, also employs single VDTA and one grounded capacitor.

Fig. 5. Grounded inductor simulator proposed in [32].
The non non ideal equivalent circuit of grounded inductor simulator proposed in [32] is shown in Fig. 6.

![Fig. 6. Non ideal equivalent circuit of grounded inductor simulator proposed in [32].](image)

where

\[
L_{eq} = \frac{(C + C_{ss}) R_x R_z}{(1 + g_m g_m' R_x R_z)} \quad (14)
\]

\[
R = \frac{(C + C_{ss}) R_x R_z}{R_x (C + C_{ss}) + R_z C_z} \quad (15)
\]

\[
C' = \frac{(C + C_{ss}) R_x + C_z R_z}{R_z} \quad (16)
\]

\[
R' = \frac{R_z}{(1 + g_m g_m' R_x R_z)} \quad (17)
\]

\[
D = (C + C_{ss}) R_x R_z \quad (18)
\]

On comparison of Fig. 4 with Fig. 6, it is clear that the effects of parasitics in the proposed circuit are lower as compared to the circuit given in [32]. Hence, the proposed configuration exhibits reduced parasitic effects.

The proposed inductor can be seen as another version of inductor simulator proposed in [29] from the viewpoint of two OTA realization of VDTA. Grounded inductor simulator proposed in [29] employs two OTAs along with one grounded capacitor. The input negative terminals of first stage OTA is grounded so full utilization of OTA is not achieved as an OTA is intended to produce output current for differential input voltage but here at input side only one voltage input is available. Moreover, in both the OTAs only one input is utilized so this work can be done with single input/single output transconductance elements which need less number of MOS transistors for implementation in comparison to MOS transistors required to implement circuit given in [29]. So, all the resources of [29] are not utilized which shows the wastage of resources. In our circuit both the input terminals of VDTA are utilized.

The transconductance gains of VDTA are frequency dependent parameter, which decide the bandwidth limitation of VDTA. The transconductances \(g_{m1}\) and \(g_{m2}\) of VDTA can be described by single pole model as follows
\[
g_m(s) = \frac{g_{m0}}{1 + s\tau_1}
\]
(19)

\[
g_{m1}(s) = \frac{g_{m20}}{1 + s\tau_2}
\]
(20)

where \(g_{m0}\) and \(g_{m20}\) are the transconductance gains at zero frequency and \(\omega_1 = \frac{1}{\tau_1}\) and \(\omega_2 = \frac{1}{\tau_2}\) are pole frequencies. Here, \(\tau_1\) and \(\tau_2\) are delays corresponding to pole frequencies \(\omega_1\) and \(\omega_2\) respectively.

The bandwidth of VDTA can be improved by inserting a compensation resistor \(R_A\), one voltage buffer and MOS transistor pair \(M_9\) and \(M_{10}\) in VDTA CMOS structure shown in Fig. 2. The modified CMOS structure is shown in Fig. 7. Transconductance gain \(g_{m1}\) for this modified VDTA can be given as

\[
g_{m1} = \frac{g_m}{1 + g_m R_A}
\]
(21)

From Eq. (21) it is clear that \(g_{m1}\) of modified VDTA can be changed by resistance “\(R_A\)”. We know that bandwidth of VDTA depends on \(g_{m1}\). Hence, bandwidth can also be controlled by \(R_A\).

Fig. 7. Modified CMOS structure of VDTA.

4. Application example
To illustrate the application of proposed grounded inductor simulator it has been employed in the realization of a second order band pass filter as shown in Fig. 8.

\[ V_{\text{out}}(s) = \frac{s(\frac{1}{R_1C_2})}{s^2 + s(\frac{1}{R_1C_2}) + \frac{g_m}{C_1C_2}} \]  

(22)

5. Simulation Result

The performance of the proposed structure has been confirmed by SPICE simulations with TSMC CMOS 0.18\(\mu\)m process parameters with ORCAD 16.3 PSPICE Simulator. The shape factors (W/L) of MOS transistors is given in Table 1.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W/L((\mu)m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1</td>
<td>3.6/.36</td>
</tr>
<tr>
<td>M2</td>
<td>3.6/.36</td>
</tr>
<tr>
<td>M3</td>
<td>16.64/.36</td>
</tr>
<tr>
<td>M4</td>
<td>16.64/.36</td>
</tr>
<tr>
<td>M5</td>
<td>3.6/.36</td>
</tr>
<tr>
<td>M6</td>
<td>3.6/.36</td>
</tr>
<tr>
<td>M7</td>
<td>16.64/.36</td>
</tr>
<tr>
<td>M8</td>
<td>16.64/.36</td>
</tr>
</tbody>
</table>

For simulations have been performed using CMOS VDTA [36] with component values: \(C_0 = 0.01\text{nF}, g_{m1}=g_{m2}=g_m = 636.3\ \mu\text{A/V}\) and power supply \(\pm 0.9\text{V} \text{DC}\). The magnitude response and the phase response of the proposed simulated inductor are shown in Fig. 9 and Fig. 10. From Fig. 9 it is clear that the simulated magnitude response of proposed inductor is same as the ideal magnitude response in the
frequency range of 804 kHz to 31.62 MHz. Similarly Figure 10 indicates that the ideal and simulated phase responses are almost identical in frequency range of 5.012 MHz to 31.42 MHz. The deviation of simulated responses from ideal responses at low frequencies can be understood by Eq. (7), which shows that under the effects of non-idealities, the proposed circuit works as a grounded series R-L circuit. The lossy term “R” is responsible for the deviation of simulated responses from ideal responses. At high frequencies the difference between ideal and simulated responses is mainly due to the parasitics of VDTA terminals.

On comparing magnitude and phase response of our circuit and responses of circuit given in [32] with ideal response, it is clear that at low frequencies the responses of circuit given in [32] are a bit better due to non availability of lossy term in non ideal conditions which is because of leaving “P” and “X-” terminal unused in this circuit. The grounded “P” terminal results in wastage of recourses and the parasitics of floating “X-” terminal are not balanced and will consume the power. So, improved low frequency response of circuit proposed in [32] is at the cost of wastage of recourses and power. At high frequencies the magnitude and phase responses of circuit given in [32] is highly deviated from ideal response due to presence of high parasitic effects. Our proposed circuit gives better response at high frequency due to low parasitic effects. So, it is verified that proposed circuit experience less parasitic effects in comparison to the circuit given in [32].

In proposed grounded inductor simulator, the bias currents $I_{b1} = I_{b2} = I_{b3} = I_{b4} = I_b$ for satisfying the condition $g_{m1} = g_{m2}$. The electronic control of proposed configuration is demonstrated by changing $I_b$ from 150 μA to 180 μA. Fig. 11 shows the magnitude responses of input impedance of proposed grounded inductor at different bias currents $I_b = 150 \mu A, 160 \mu A, 170 \mu A$ and 180 μA.

To confirm the workability of bandpass filter, the circuit was simulated using the CMOS VDTA [36] with $R_1 = 1.58k\Omega$, $C_1 = 0.01nF$, $C_2 = 5pF$, $g_{m1} = g_{m2} = g_m = 636.3 \mu A /V$ with power supply ± 0.9V DC. The frequency response of this realized bandpass filter is shown in Fig. 12, where central frequency of simulated filter is found to be 14.1 MHz.
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Fig. 10. Phase response.

Fig. 11. Electronic tunability of magnitude response of proposed grounded inductor simulator.

Fig. 12. Frequency response of second order voltage mode bandpass filter.
6. Conclusion

A new single VDTA based grounded inductor simulator circuit has been proposed which offers electronic controllability and reduced parasitic effects. The proposed configuration requires a realization condition which can be easily met by equating the two bias currents of VDTA. To verify the validity of the proposed grounded inductor, a second order bandpass filter has been realized. The SPICE simulation results confirm the theoretical predictions.

References


