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# IMPROVING BANDWIDTH OF FLIPPED VOLTAGE FOLLOWER USING GATE-BODY DRIVEN TECHNIQUE

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**Abstract**

In this paper, a new approach to enhance the bandwidth of flipped voltage follower is explored. The proposed approach is based on gate-body driven technique. This technique boosts the transconductance in a MOS transistor as both gate and body/bulk terminals are tied together and used as signal input. This novel technique appears as a good solution to merge the advantages of gate-driven and bulk-driven techniques and suppress their disadvantages. The gate-body driven technique utilizes body effect to enable low voltage low power operation and improves the overall performance of flipped voltage follower, providing it with low output impedance, high input impedance and bandwidth extension ratio of 2.614. The most attractive feature is that bandwidth enhancement has been achieved without use of any passive component or extra circuitry. Simulations in PSpice environment for 180 nm CMOS technology verified the predicted theoretical results. The improved flipped voltage follower is particularly interesting for high frequency low noise signal processing applications.

Keywords: Body effect, Gate-body driven MOS transistor, High bandwidth, Flipped voltage follower, Low voltage, Low power.

## 1. Introduction

The need for analog voltage buffer circuits in modern mixed-signal VLSI chips for multimedia, perception, control, instrumentation, medical electronics and telecommunication is very high. One of the most widely used buffer is flipped voltage follower (FVF), introduced by Carvajal et al. [1] for low voltage and low power operation. A FVF has better performance than many conventional voltage buffers in terms of signal swing, gain, impedance etc. The applications of the FVF

and its variations in analog and mixed signal circuit design have increased continuously over the last few years and these structures specially seem to be promising in deep submicron CMOS technology. The shrinking sizes of semiconductor devices in CMOS technology entail the simultaneous reduction of supply voltage and threshold voltage of MOS transistor. Since the threshold voltage of MOS transistor is not reduced at the same rate as the power supply, it becomes increasingly difficult to design analog buffer circuits because of the reduced voltage headroom. At reduced supply voltage, the degradation of the transistor's intrinsic gain and related tradeoff between cutoff frequency and intrinsic gain poses a major challenge in the design of wideband analog circuits using FVF in scaled technologies [2].

Many different techniques have been reported in the literature to meet the specific requirements of FVF for applications such as current sensor, current mirrors, differential pair, OTA, instrumentation amplifier, arithmetic circuits, translinear loops [3-9]. However, many of these reported techniques have become inefficient in a reduced supply voltage environment. This trend has forced FVF to be redesigned using alternative circuit structures, in an attempt to guarantee high performance. This has also diverted the circuit designers to use non-conventional MOS transistor implementation techniques [10] such as bulk-driven, floating gate and quasi-floating gate techniques for designing FVF based circuits where high data rates and large bandwidth are required.

The increasing demand of high speed wireless communication systems has motivated the circuit designers to design FVF with wider bandwidth. Angulo et al. [11] have used quasi-floating gate (QFG) technique to increase the bandwidth of FVF. This technique uses a large resistor in the order of hundreds of hundreds of GΩ to set the quiescent voltage at the gate of MOS transistor. A large increase in bandwidth of FVF was achieved using QFG technique; however, this technique increases circuit complexity, occupies a large chip area and has higher input referred noise. Gupta et al. [12] improved the bandwidth of FVF using an on-chip resistor. The bandwidth of FVF and output impedance depends on the value of resistor. For higher bandwidth and lower output impedance, a large value of resistor is essential. However, peaking in the frequency response increases significantly with increase in resistor value. In addition to this, use of resistor increases the dc power dissipation and overall circuit noise owing to the additional thermal noise. Also, integrated have large tolerance of its absolute values and even with mature process, the integrated resistor can have more than 10% variations. Singh et al. [13] bandwidth of FVF is improved using two methods, first one being an on-chip inductor and second one is on-chip resistor along with inductor in series. Generally, use of inductors is preferred as compared to resistors in high frequency integrated circuits due to lower noise and dc power dissipation. However, inductors occupy large chip area and therefore increases the overall fabrication cost. Inductor also has a strong interaction with the substrate thereby added inductor-substrate capacitance may result in ringing.

In this work, the bandwidth of FVF is improved using gate-body driven technique. This technique improves the bandwidth of FVF without using any passive component and additional circuitry. The most attractive feature of the gate-body driven technique is that it utilizes the body effect in a MOS transistor to lower its threshold voltage electronically, without any technology modification. This technique not only increases the effective transconductance of MOS

transistor but desirable low voltage low power operation is also fulfilled. The remainder of the paper proceeds as follows: In section 2, gate-body driven technique is presented and the small signal model of gate-body driven MOS transistor is proposed. Conventional FVF is given in section 3. In section 4, the analytical formulation of impedance and transfer function of improved FVF is obtained using small signal analysis. Section 5 presents application of the improved FVF in a current mirror. The simulation results are provided in section 6 and concluding remarks are given in section 7.

## 2. Gate-body driven technique

The transition frequency of a MOS transistor is directly proportional to its transconductance whereas the input referred noise power spectral density of a MOS is inversely proportional to its transconductance [14]. Therefore, for design of a low noise wideband circuit, a higher value of MOS transconductance is highly desired. The transconductance of a MOS transistor can be increased by increasing its aspect ratio (W/L) but this technique is not suitable for low voltage applications as it increases the power dissipation. Also, the increased parasitic capacitance limits the input/output swing of circuit. Therefore other techniques must be investigated for increasing the transconductance of MOS transistor.

In a conventional gate-driven technique, the input signal is applied to the gate terminal of MOS transistor, therefore, only gate transconductance ($g_m$) contributes to the conduction current. The threshold voltage of gate-driven MOS transistor is not expected to decrease further than what is available today. One of the possible solutions to overcome this limitation is body/bulk-driven technique. The threshold voltage drop is removed from signal path as input signal is applied at the body terminal of the MOS transistor while a sufficient voltage at the gate terminal, $V_{GS}$ keeps the transistor in the conductance region [10]. As the gate terminal in body-driven MOS transistor is at AC ground therefore, only body transconductance ($g_{mb}$) contributes to conduction current. However, body-driven technique suffer from low transconductance, low transition frequency, higher noise, complex circuit structure and require more chip area. If input signal is applied to the gate as well as body terminal simultaneously then both $g_m$ and $g_{mb}$ can contribute to the conduction current in a MOS transistor. Figure 1 shows such a solution where, both gate and body terminals are tied together and used as signal input. This technique, named as gate-body driven technique and first presented in [15], preserves some of the advantages of gate-driven technique and overcomes some of the limitations of body-driven technique.

In gate-body driven technique, the threshold voltage ($V_T$) of MOS transistor becomes function of input signal due to body effect [16]. With applied input signal at gate terminal, bias voltage at body terminal ($V_{BS}$) changes dynamically as input changes. In a gate-body driven MOS transistor, $V_{GS} = V_{BS}$ is maintained all the time as gate and body terminals are shorted together. Therefore, any variations of the gate potential induce the same variations to the body potential and dynamically changes the threshold voltage due to body effect. The relation between input signal and $V_T$ for gate-body driven MOS transistor is described using the following equation [17].

$$V_T = V_{T0} + \gamma\left(\sqrt{|\psi_s - V_{GS}|} - \sqrt{|\psi_s|}\right) \quad (1)$$

where $V_T$ is threshold voltage due to body effect i.e. potential difference between body and source terminal, $V_{T0}$ is the threshold voltage when body and source terminals are at same potential and mainly depends on the manufacturing process. $\gamma$ is body effect factor and depends on the gate oxide capacitance, silicon permittivity, doping level and other parameters. The body effect factor signifies the effect of changes in $V_{SB}$ on threshold voltage and is given as $\gamma = \sqrt{2q\varepsilon_{si}N_A}/C_{ox}$ and has the dimension of $\sqrt{\text{Volts}}$. q is electronic charge, $\varepsilon_{si}$ is dielectric permittivity of silicon, $N_A$ is doping concentration of the p-type substrate and $C_{ox}$ is oxide capacitance per unit area. The parameter $\gamma$ is typically 0.4 $V^{0.5}$ . $\psi_s$ in Eq. (1) is assumed to be $|\, 2\varphi_F \,|$, where $\varphi_F$ is Fermi potential.

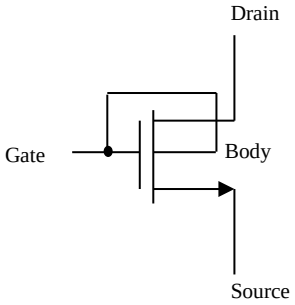


**Fig. 1. Gate-body driven technique.**

A gate-body driven MOS transistor can be been viewed as dual gate transistor due to the applied bias ($V_{BS}$=$V_{GS}$) at body terminal of the transistor. The potential in the channel region of a gate-body driven MOS transistor is strongly controlled by both gate and body terminals, leading to a high transconductance owing to faster current transport. Thus, both gate and body transconductances contribute to the conduction current and effective transconductance of the gate-body driven transistor is ($g_m + g_{mb}$). In gate-body driven MOS transistor, source-body junction gets slightly forward biased when input signal increases. Although source-body junction parasitic diode is slightly forward biased but any substantial conducting pn junction current is absent as $V_T$ decreases due to the body effect.

The small signal equivalent model of gate-body driven MOS transistor proposed in [16] is shown in Fig. 2. It has two transconductances, the gate transconductance ($g_m$) and body transconductance ($g_{mb}$). The relation between both transconductances is

$$\frac{g_{mb}}{g_m} = \frac{C_{BC}}{C_{GC}} = \eta \approx (0.2 - 0.4) \tag{2}$$

where $C_{BC}$, $C_{GC}$, and $\eta$ are the total body-channel capacitance, the total gate channel capacitance and the specific parameter, respectively. The value of the specific parameter $\eta$ depends on bias conditions and on the technology used. The gate-body driven MOS transistor has additional parasitic capacitance and resistance associated with body. The effective input capacitance ($C_{DB}$) and effective input resistance ($R_{DB}$) for a gate-body driven MOS transistor is defined as

$$C_{DB} \approx \left(C_{gs} + C_{body}\right) \tag{3}$$

$$R_{DB} \approx \left(R_{gb} + R_{body}\right) \tag{4}$$

where $C_{body}$ is body-capacitance, $C_{gs}$ is gate-capacitance, $R_{gb}$ is gate-body contact resistance, $R_{body}$ is body resistance of a gate-body driven MOS transistor. Based on the small signal model in Fig. 2, a comparison of gate-body driven MOS transistor with conventional gate-driven and bulk/body-driven MOS transistors has been summarized in Table 1.

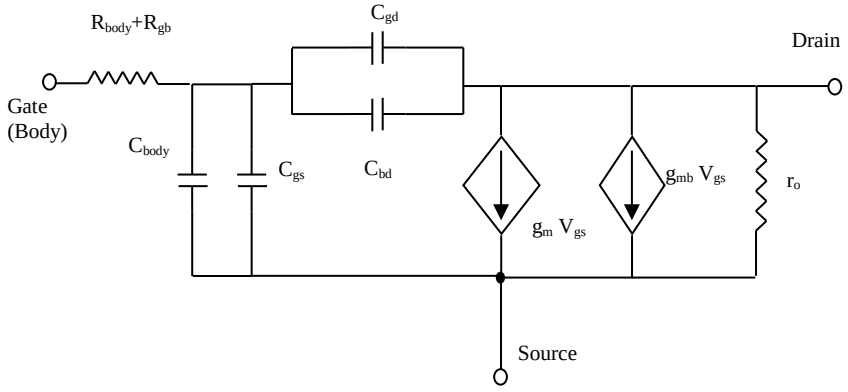


**Fig. 2. Small signal model of gate-body driven MOS transistor.**

**Table 1. Comparison of gate and body driven transistor with gate-driven and bulk-driven transistors.**

| **Type of MOS transistor** | **Gate-driven** | **Bulk/Body-driven** | **Gate -Body driven** |
|---|---|---|---|
| **Threshold Voltage requirement** ($V_T$) | $V_{T0} + \gamma\left(\sqrt{\psi_s + V_{SB}} - \sqrt{\psi_s}\right)$<br>$V_T = V_{T0}$ (as $V_{SB} = 0$ ususally) | Removed from signal path | $V_{T0} + \gamma\left(\sqrt{\psi_s - V_{GS}} - \sqrt{\psi_s}\right)$<br>Reduced when input signal is applied otherwise it's same as gate-driven MOS transistor for no input signal. |
| **Effective Transconductance** | $g_m$ | $g_{mb}$ | $(g_m + g_{mb})$ Increased |
| **Transition frequency (** $f_T$) | $\frac{g_m}{2\pi C_{gs}}$ | $\frac{g_{mb}}{2\pi(C_{bs} + C_{body}}$ | $\frac{g_m + g_{mb}}{2\pi(C_{gs} + C_{body})}$ |
| **Input referred noise** ($v^2_{noise,}(f)$) | $\frac{i_{ni}^2}{g_m^2}$ | $\frac{i_{ni}^2}{g_{mb}^2}$ | $\frac{i_{ni}^2}{(g_m + g_{mb})^2}$ |

From the results shown in Table 1, it is seen that gate-body driven technique utilizes body effect advantageously and offers many advantages such as lower threshold voltage, higher effective transconductance, lower input referred noise and higher transition frequency. This technique is implemented using triple well CMOS technology; hence latch-up is absent [18]. A triple well structure reduces the cross-talk in mixed systems-on-chip designs and is more robust to process and well junction capacitance variations.

## 3. Conventional Flipped Voltage Follower

A FVF is used as voltage buffer given that it is characterized by high input impedance, low output impedance and high bandwidth. A FVF can operate at low voltage and has almost unity gain if short channel effects are negligible The conventional FVF circuit is shown in Fig. 3 [1]. It is essentially a cascode amplifier with negative feedback where the gate terminal of transistor $M_1$ is used as the input node and its source terminal as the output node. The maximum current through $M_1$ is equal to the biasing current source ($I_b$ ) and is constant as the gate terminal of transistor $M_2$ does not take current from $I_b$. Therefore neglecting the body effect, the gate-to-source voltage ($V_{GS1}$) of $M_1$ has to remain constant and thus the variations in the input signal ($V_{in}$) will be reflected in the output signal ($V_{out}$) level, shifted by DC voltage of $V_{GS1}$. The shunt negative feedback between the gate terminal of $M_2$ and the drain terminal of the $M_1$ adjusts the gate-to-source voltage ($V_{GS2}$) of $M_2$ to satisfy the current requirements of the circuit. This gives $M_2$ the property to sink a large current if needed, although the current sourcing capability of the circuit is limited to $I_b$ coming from $M_1$.

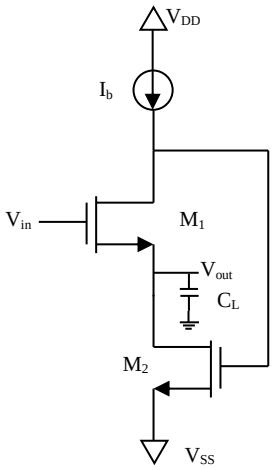


**Fig. 3. Conventional flipped voltage follower.**

The output impedance ($Z_{out}$) of conventional FVF, is given as [8]

$$Z_{out} = \frac{1}{g_{m2}(g_{m1}r_{o1})} \quad (5)$$

Generally the output impedance of CFVF is reduced by using either large bias current or large W/L ratio of MOS transistor but both these techniques increase the quiescent power dissipation. Increasing the size of MOS transistor also increases the silicon area.

The transfer function of conventional FVF is given by following expression [12]

$$A_v(s) = \frac{s^2+a_1 s+a_2}{s^2+a_1 s+(a_2+\Delta a_2)} \tag{6}$$

where $a_1 = \left(\frac{1}{C_{gs2}\, r_{o1}} + \frac{g_{m1}}{C_{gs1}}\right)$, $a_2 = \frac{g_{m1} g_{m2}}{C_{gs1} C_{gs2}}$ and $\Delta a_2 = \frac{g_{m2}}{C_{gs1} C_{gs2}\, r_{o1}}$

From Eq. (6), the zeroes and poles of conventional FVF are obtained as

$$Z_{1,2} = \frac{-a_1}{2}\left[1 \mp \sqrt{1 - 4\left(\frac{a_2}{{a_1}^2}\right)}\right] \tag{7}$$

$$P_{1,2} = \frac{-a_1}{2}\left[1 \mp \sqrt{1 - 4\left(\frac{a_2+\Delta a_2}{{a_1}^2}\right)}\right] \tag{8}$$

and -3 dB frequency of conventional FVF is obtained as

$$\omega_o = \sqrt{\frac{2 g_{m1} g_{m2}}{C_{gs1} C_{gs2}} - \frac{4 g_{m2}}{C_{gs1} C_{gs2}\, r_{o1}} - \frac{1}{\left(C_{gs2}\, r_{o1}\right)^2} - \left(\frac{g_{m1}}{C_{gs1}}\right)^2} \tag{9}$$

It is evident from Fig. 3 that output of FVF, $V_{out}$ is affected by the body effect present in $M_1$. Due to body effect, the ideal square-law behaviour of MOS transistor in saturation region of operation approaches more closely to an ideal linear transfer function. Zhu et al. [19] has shown that due to body effect high-order harmonics are introduced to the drain current expression which results in an error in the transconductance of a MOS transistor. If body effect in $M_1$ is neglected then this error is given by

$$\Delta V_T = (V_T - V_{T0}) = \gamma\left(\sqrt{\psi_s + V_{SB}} - \sqrt{\psi_s}\right) \tag{10}$$

From Eq. (10) it can be seen that if body and source terminals are at different potentials then body effect in MOS transistor causes nonlinear behaviour of transconductance with respect to input signal. As a result, high-order harmonics introduced to the drain current expression. This degrades linearity in FVF and output is not able to follow input signal over a wider range without distortion. In this work, body effect in $M_1$ is utilized using gate-body driven technique, which results in enhanced bandwidth and improved impedance of FVF.

## 4. Improved Flipped Voltage Follower

In most of the reported FVF analysis, body effect has been neglected. For a given fabrication process, the main factors determining the amount of distortion are the quiescent output voltage and the output swing. To a first order, distortions are nearly proportional to the body effect factor $\gamma$ and do not depend on $I_b$ or device geometry of $M_1$ [20]. Body effect plays insignificant role when operated at higher power supply voltage. However, when operating at low voltage, it is desirable to

study its effect on the performance of MOS transistor. In this work, body effect present in a MOS transistor has been effectively utilized by using gate-body driven technique. The circuit implementation of the improved FVF is shown in Fig. 4. Gate-body driven technique is applied to $M_1$ and for $M_2$ body terminal is connected to ground. When input signal is applied to $M_1$, its body-source junction gets forward biased and $V_{BS}$ increases which reduces threshold voltage of $M_1$ as seen from Eq. (1). Reduction in threshold voltage is due to the reduction in body charge which leads to an advantage of lower effective normal field and higher carrier mobility. Higher mobility results in higher on current drive in $M_1$ proportional to increase in gate overdrive voltage ($V_{GS1}$-$V_{T1}$). This higher on current to the output load will reduce the charging time, thereby making FVF to work faster.

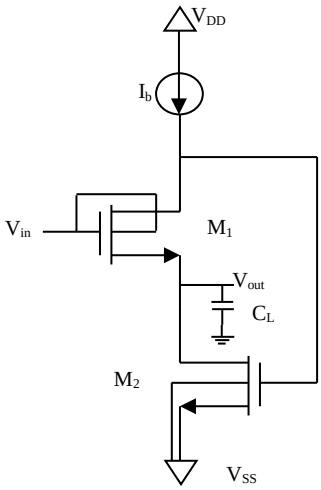


**Fig. 4. Improved flipped voltage follower.**

In this section, the effect of gate-body driven technique on the input and output impedance of the improved FVF has been analysed. Based on the derived analytical equations, it has been found that effective input resistance of $M_1$ is the controlling factor for the input impedance of the improved FVF. The output impedance in improved FVF decreases and transfer function analysis result of the improved FVF predicts a very large improvement in its bandwidth.

## 4.1. Input impedance analysis of improved FVF

The small signal model of improved FVF to obtain input impedance ($Z_{in}$) is shown in Fig. 5. The notations used in the analysis are as follows: $r_{oi}$ is resistance and $g_{oi}$[=$1/r_{oi}$ ]is conductance due to channel length modulation for $M_i$, for i=1,2. $r_b$ is the impedance of $I_b$, $g_{mi}$ is transconductance of $M_i$, $V_{gsi}$ is gate-to-source voltage of Mi, where i= 1,2. $g_{mb1}$ is body transconductance of $M_1$ and $R_{DB}$ is effective input resistance of $M_1$ defined by Eq. (4).

Writing equation for node $S_1$, we get

$$I_{in} + (g_{m1} + g_{mb1})(V_{in} - V_{s1}) + \frac{V_{gs2} - V_{s1}}{r_{o1}} = g_{m2}V_{gs2} + \frac{V_{s1}}{r_{o2}} \quad (11)$$

Assuming $R_{body} \gg R_{gb}$, from(4) we get, $R_{DB} \approx R_{body}$. Also,

$$I_{in} = \frac{V_{in} - V_{s1}}{R_{body}} \tag{12}$$

and combining Eqs. (11) and (12) and simplifying we get,

$$I_{in}\left[1 + (g_{m1} + g_{mb1})R_{body} + \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right)R_{body}\right] - V_{in}\left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right) = V_{gs2}\left(g_{m2} - \frac{1}{r_{o1}}\right) \tag{13}$$

Assuming $(g_{m1} + g_{mb1})R_{body} + \left(\frac{1}{r_{o1}} + \frac{1}{r_{o2}}\right)R_{body} \gg 1$, Eq. (13) is simplified as

$$V_{gs2} = \frac{I_{in}\left[(g_{m1}+g_{mb1})R_{body} + \left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}\right)R_{body}\right] - V_{in}\left(\frac{1}{r_{o1}}+\frac{1}{r_{o2}}\right)}{\left(g_{m2}-\frac{1}{r_{o1}}\right)} \tag{14}$$

Writing equation for node $G_2$, we get

$$\frac{V_{gs2}}{r_b} = \frac{V_{s1} - V_{gs2}}{r_{o1}} - (g_{m1} + g_{mb1})(V_{in} - V_{s1}) \tag{15}$$

and combining Eqs. (12) and (15) and simplifying we get

$$V_{gs2} = \frac{\frac{V_{in}}{r_{o1}} - I_{in}\left[\frac{R_{body}}{r_{o1}} + (g_{m1}+g_{mb1})R_{body}\right]}{\left(\frac{1}{r_b}+\frac{1}{r_{o1}}\right)} \tag{16}$$

From Eqs. (14) and (16), input impedance of improved FVF is obtained as

$$Z_{in} = \frac{V_{in}}{I_{in}} \approx R_{body}\left[\frac{\left(g_{m2}+\frac{1}{r_b}\right)\left(g_{m1}+g_{mb1}+\frac{1}{r_{o1}}\right)+\frac{1}{r_{o2}}\left(\frac{1}{r_{o1}}+\frac{1}{r_b}\right)}{\frac{1}{r_{o1}}\left(g_{m2}+\frac{1}{r_b}\right)+\frac{1}{r_{o2}}\left(\frac{1}{r_{o1}}+\frac{1}{r_b}\right)}\right] \tag{17}$$

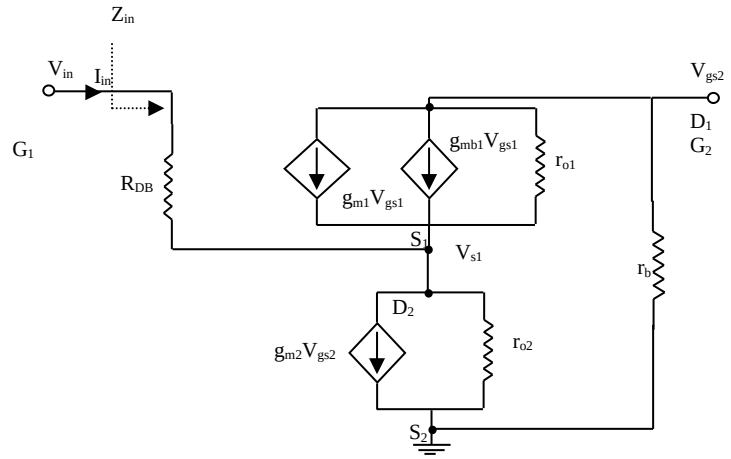


**Fig. 5. Small signal model for calculating input impedance of improved FVF.**

From Eq. (17), it is observed that the input impedance of the improved FVF can be controlled by $R_{body}$. Body resistance plays an important role in both DC & AC performance. For gate-body driven MOS transistor, $R_{body}$ is proportional to number of gate fingers and gate width. Thus the width of transistor needs to be optimized to obtain body resistance values. In FVF high input impedance is desirable. Therefore in improved FVF, $R_{body}$ is an effective knob to control the input impedance requirement in any application. The typical values of the body sheet resistance for gate-body driven MOS transistor are nearly (1-10) KΩ per square.

## 4.2. Output Impedance analysis of improved FVF

The output impedance ($Z_{out}$) is obtained using open loop analysis by connecting a test voltage source at the output and measuring the current flowing into the circuit, while keeping input terminal at ac ground. Figure 6 shows open-loop circuit equivalent to improved FVF. The notations used in the analysis are same as used in section 4.1. Figure 6 shows open-loop circuit equivalent to improved FVF. Due to gate-body driven technique, the total transconductance of $M_1$ is ($g_m$+ $g_{mb}$) . For $M_2$, $V_{SB}$ = 0. We open the feedback loop at node Y and apply a test voltage ($V_t$) at gate terminal of $M_2$.$V_{in}$ is set to zero and returned voltage ($V_r$) is connected at node Y. To ensure that the conditions that existed prior to breaking the loop do not change, we terminate node Y with impedance corresponding to $C_C$ so that impedance at node Y is equal to that seen before the loop was broken. Closed loop resistance at node X( $R_{CLX}$ = $Z_{out}$) is obtained using following relations [14].

$$R_{CLX} = \frac{R_{OLX}}{1+|A_{OL}|} \tag{18}$$

where $R_{OLX}$ is open loop resistance at node X and $A_{OL}$ is open loop gain of improved FVF in Fig. 6

$$A_{OL} = -\frac{V_r}{V_t} = -g_{m2}R_{OLY} \tag{19}$$

where $R_{OLY}$ is open loop resistance of node Y.

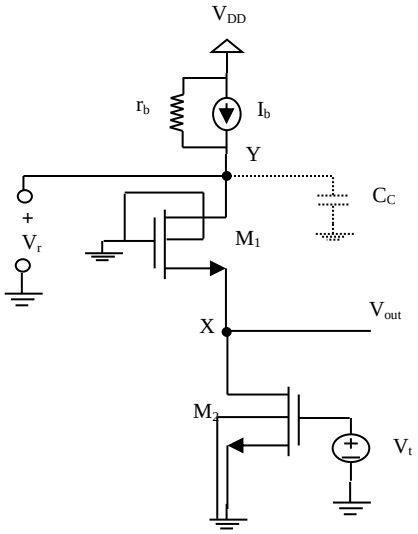


**Fig. 6. Open-loop circuit of improved FVF.**

### 4.2.1. Small signal analysis for $R_{OLY}$

In this section, open loop resistance of node Y is calculated using small signal models in Fig. 7 and Fig. 8 . On applying KCL at node $V_Y$, we get

$$I_Y = \frac{(V_Y - V_{S1})}{r_{o1}} + (g_{m1} + g_{mb1})\, V_{gs1} \tag{20}$$

Simplifying Eq. (20), we get

$$V_{S1} = \frac{g_{o1} V_Y - I_Y}{g_{o1} + (g_{m1} + g_{mb1})} \tag{21}$$

On applying KCL at node $V_{S1}$, we get

$$\frac{(V_Y - V_{S1})}{r_{o1}} + (g_{m1} + g_{mb1})\, V_{gs1} = \frac{V_{S1}}{r_{o2}} + g_{m2} V_{gs2} \tag{22}$$

Simplifying Eq. (22), we get

$$V_{S1} = \frac{V_Y g_{o1}}{g_{o1} + g_{o2} + (g_{m1} + g_{mb1})} \tag{23}$$

Equating Eqs. (21) and (23), $R_Y$ is obtained as

$$R_Y = \frac{V_Y}{I_Y} = r_{o1} + r_{o2} + r_{o1} r_{o2} (g_{m1} + g_{mb1}) \tag{24}$$

Assuming $r_{o1} r_{o2} \gg r_{o1} + r_{o2}$ , Eq. (24) reduces to

$$R_Y \approx r_{o1} r_{o2} (g_{m1} + g_{mb1}) \tag{25}$$

From Fig. 8, $R_{OLY}$ is found to be

$$R_{OLY} \approx r_b || R_Y \approx r_b || [r_{o1} r_{o2} (g_{m1} + g_{mb1})] \tag{26}$$

It is observed from Eq. (26) and Eq. (19) that, gate-body driven technique has increased the open loop gain of FVF. Due to higher open loop gain, the output impedance of improved FVF decreases as evident from Eq. (18).

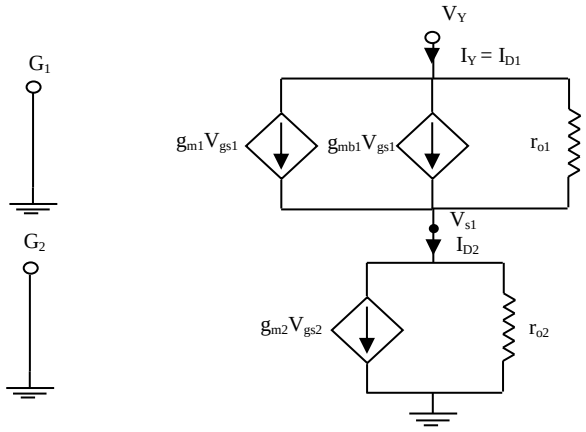


**Fig. 7. Small signal model for calculating $R_Y$ at node Y.**

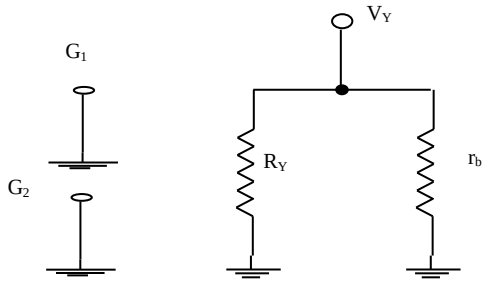


**Fig. 8. Small signal model for calculating $R_{OLY}$ at node Y.**

### 4.2.2. Small signal analysis for $R_{OLX}$

In this section, open loop resistance of node X is calculated using small signal models in Fig. 9 and Fig. 10. On applying KCL at node $V_X$ and $V_{D1}$, we get

$$I_X = (g_{m1} + g_{mb1})V_X + \frac{(V_X - V_{D1})}{r_{o1}} \tag{27}$$

$$I_X = \frac{V_{D1}}{r_b} \tag{28}$$

From Eqs. (27) and (28), $R_X$ is obtained as

$$R_X = \frac{V_X}{I_X} = \frac{r_{o1} + r_b}{1 + (g_{m1} + g_{mb1})r_{o1}} \tag{29}$$

Assuming $g_{m1}r_{o1} \gg 1$ and simplifying, Eq. (29) reduces to

$$R_X \approx \frac{1}{(g_{m1} + g_{mb1})}\left(1 + \frac{r_b}{r_{o1}}\right) \tag{30}$$

From Fig. 10, $R_{OLX}$ is found to be

$$R_{OLX} \approx r_{o2} || R_X \approx r_{o2} || \frac{1}{(g_{m1} + g_{mb1})}\left(1 + \frac{r_b}{r_{o1}}\right) \tag{31}$$

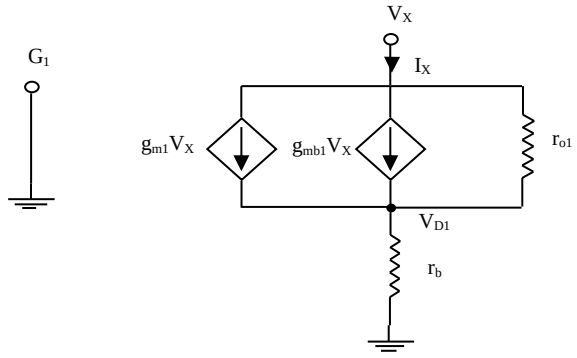


**Fig. 9. Small signal model for calculating $R_X$ at node X.**

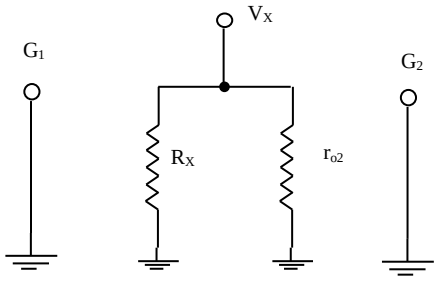


**Fig. 10. Small signal model for calculating $R_{OLX}$ at node X.**

### 4.2.3. Analysis for $R_{CLX}$

In this section, closed loop resistance of node X is calculated using Eq. (18) and Eq. (19). Substituting the value of value of open loop resistance of node Y from Eq. (26) and open loop resistance of node X from Eq. (31), $R_{CLX}$ can be expressed as

$$R_{CLX} = \frac{r_{o2} || \frac{1}{(g_{m1}+g_{mb1})}\left(1+\frac{r_b}{r_{o1}}\right)}{1+g_{m2}[\, r_b || \{r_{o1}\ (g_{m1}+g_{mb1})\ \}]} \tag{32}$$

If $r_b$ is very large then we can assume $r_b \approx r_{o1}r_{o2}(g_{m1}+g_{mb1})$ and $R_{CLX}$ is expressed as

$$R_{CLX} = \frac{r_{o2} || \frac{1}{(g_{m1}+g_{mb1})}\left(1+\frac{r_{o1}\, r_{o2} g_{m1}}{r_{o1}}\right)}{1+g_{m2}[\{r_{o1}r_{o2}(g_{m1}+g_{mb1})\}] || \{r_{o1}r_{o2}\,(g_{m1}+g_{mb1})\}]} \tag{33}$$

Assuming $g_{m2}\frac{[r_{o1}r_{o2}(g_{m1}+g_{mb1})\,]}{2} \gg 1$ and simplifying Eq. (33), the output impedance of proposed FVF is obtained as

$$Z_{out,improved} \approx \frac{1}{(g_{m1}+g_{mb1})g_{m2}r_{o1}} \approx \frac{1}{Z_{out}+g_{mb1}g_{m2}r_{o1}} \tag{34}$$

Comparing Eq. (5) and Eq. (34), it is evident that gate-body driven technique reduces the output impedance of improved FVF.

## 4.3. Bandwidth analysis of improved FVF

The small signal equivalent model for calculating -3 dB frequency of improved FVF is shown in Fig. 11. In the analysis, impedance of current source $I_b$ has been neglected for the sake of simplicity of analytical expressions since the aim is to show that there is bandwidth improvement in improved FVF rather than finding an exact value and rest of the symbols used are same as in section 4.1

Writing KCL at node $S_1$, we get

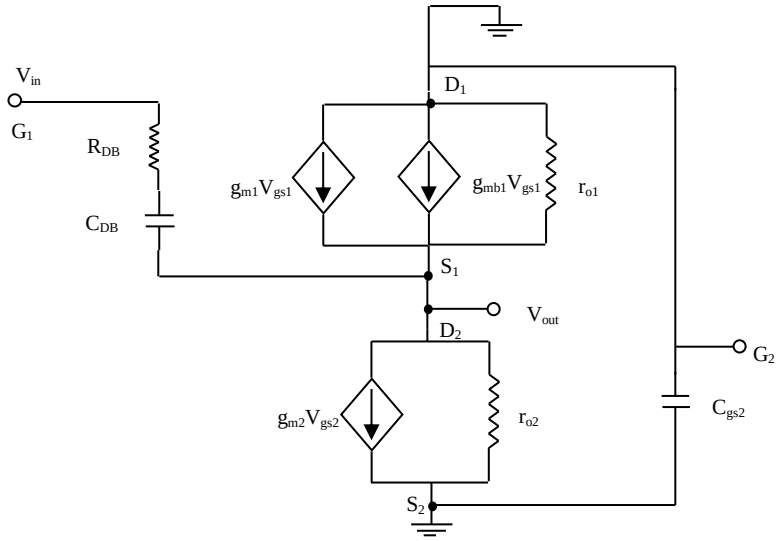


**Fig. 11. Small signal model for calculating -3db bandwidth of improved FVF.**

$$\frac{(V_{out}-V_{in})}{\left(R_{DB}+\frac{1}{sC_{DB}}\right)}-(g_{m1}+g_{mb1})(V_{in}-V_{out})+\frac{V_{out}-V_{gs2}}{r_{o1}}+g_{m2}V_{gs2}+\frac{V_{out}}{r_{o2}}=0 \quad (35)$$

Writing KCL at node $G_2$, we get

$$\frac{V_{gs2}-V_{out}}{r_{o1}}+(g_{m1}+g_{mb1})(V_{in}-V_{out})+sC_{gs2}V_{gs2}=0 \quad (36)$$

Substituting Eqs. (35) in (36) and rearranging, transfer function of improved FVF is obtained as

$$A_v(s)=\frac{V_{out}}{V_{in}}=\frac{\begin{array}{c}s^2[C_{DB}C_{gs2}r_{o1}\,r_{o2}+C_{DB}C_{gs2}r_{o1}\,r_{o2}R_{DB}(g_{m1}+g_{mb1})]+\\ s[C_{DB}\,r_{o2}+C_{gs2}\,r_{o1}\,r_{o2}(g_{m1}+g_{mb1})+R_{DB}C_{DB}\,g_{m2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})]+\,g_{m2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})\end{array}}{\begin{array}{c}s^2[C_{DB}C_{gs2}r_{o1}\,r_{o2}+\,r_{o1}\,r_{o2}R_{DB}C_{DB}C_{gs2}(g_{m1}+g_{mb1})+\,r_{o2}R_{DB}C_{DB}C_{gs2}+\,r_{o1}R_{DB}C_{DB}C_{gs2}]+\\ s[\,r_{o2}C_{DB}+C_{gs2}\,r_{o1}\,r_{o2}(g_{m1}+g_{mb1})+C_{gs2}\,r_{o2}+R_{DB}C_{DB}+C_{gs2}\,r_{o1}+C_{DB}\,g_{m2}\,r_{o2}]+\\ [1+g_{m2}\,r_{o2}+g_{m2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})]\end{array}} \quad (37)$$

Assuming $R_{DB}\gg r_{o2}$ and simplifying Eq. (37) further, we get

$$A_v(s)=\frac{\begin{array}{c}s^2[R_{DB}C_{DB}C_{gs2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})]+\\ s[R_{DB}C_{DB}\,g_{m2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})+C_{gs2}\,r_{o1}\,r_{o2}(g_{m1}+g_{mb1})]+\,g_{m2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})\end{array}}{\begin{array}{c}s^2[R_{DB}C_{DB}C_{gs2}r_{o1}\,r_{o2}(g_{m1}+g_{mb1})]+\\ s[\,r_{o1}\,r_{o2}C_{gs2}(g_{m1}+g_{mb1})+\,r_{o2}R_{DB}C_{DB}g_{m2}]+\,r_{o1}\,r_{o2}g_{m2}(g_{m1}+g_{mb1})\end{array}} \quad (38)$$

Simplifying and rearranging Eq. (38) further, we obtain

$$A_v(s) = \frac{s^2+s\left[\frac{1}{R_{DB}C_{DB}}+\frac{g_{m2}}{C_{gs2}}\right]+\frac{g_{m2}}{C_{gs2}R_{DB}C_{DB}}}{s^2+s\left[\frac{1}{R_{DB}C_{DB}}+\frac{g_{m2}}{r_{o1}(g_{m1}+g_{mb1})C_{gs2}}\right]+\frac{g_{m2}}{C_{gs2}R_{DB}C_{DB}}} \quad (39)$$

As $C_{DB} \gg C_{gs2}$ , Eq. (39) can be expressed as

$$A_v(s) = \frac{s^2+B_1 s+B_2}{s^2+(B_1+\Delta B_1)s+B_2} \quad (40)$$

where $B_1 = \frac{g_{m2}}{C_{gs2}}$, $\Delta B_1 = \frac{g_{m2}}{r_{o1}(g_{m1}+g_{mb1})C_{gs2}} - \frac{g_{m2}}{C_{gs2}}$ and $B_2 = \frac{g_{m2}}{C_{gs2}R_{DB}C_{DB}}$

From Eq. (40), the zeroes and poles of improved FVF are found to be

$$Z_{1,2} = \frac{-B_1}{2}\left[1 \mp \sqrt{1-4\left(\frac{B_2}{{B_1}^2}\right)}\right] \quad (41)$$

$$P_{1,2} = \frac{-(B_1+\Delta B_1)}{2}\left[1 \mp \sqrt{1-4\left(\frac{B_2}{(B_1+\Delta B_1)^2}\right)}\right] \quad (42)$$

By definition [19], at $\omega = \omega_o$

$$|A_v(\omega_o)|^2 = 0.5\,|A_v(0)|^2 \quad (43)$$

where $|A_v(0)|^2 = 1$ of improved FVF

From Eqs. (40) and (43), -3 dB frequency is obtained as

$$\omega_o = \sqrt{\frac{2g_{m2}}{R_{DB}C_{DB}C_{gs2}} + \left(\frac{g_{m2}}{C_{gs2}\,r_{o1}(g_{m1}+g_{mb1})}\right)^2 - 2\left(\frac{g_{m2}}{C_{gs2}}\right)^2} \quad (44)$$

From Eq. (44), it is observed that -3 dB frequency of improved FVF is mainly controlled by the transconductance, effective input resistance and effective input capacitance of gate-body driven MOS transistor $M_1$. On comparing Eq. (42) and Eq. (44) with the results obtained for conventional FVF in Eq. (8) and Eq. (9), it is seen gate-body driven technique has moved the poles of the transfer function apart, resulting a very large improvement in the bandwidth of improved FVF.

## 5. Application of the improved FVF

Modern VLSI systems now operating from single 1.5V supplies or less require high performance current mirrors that can operate at low power supply voltages in applications where high data rates and large bandwidth are required. The increasing demand of low voltage current mirrors in high speed communication systems and wireless equipment have motivated the researchers to explore the techniques for improving the high frequency characteristics. The improved FVF can be used as the input stage of a low voltage current mirror [21]. Figure 12 shows application of improved FVF in a current mirror. Gate-body driven technique enables low voltage and low power operation. The simulation results of all the circuits are discussed in next section.

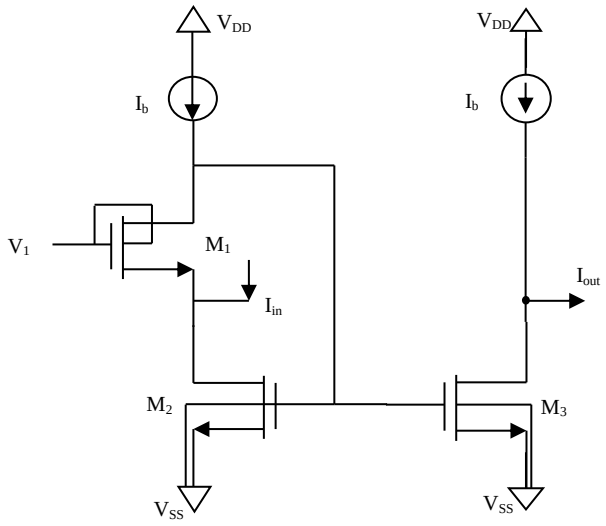


**Fig. 12. Current mirror using improved FVF.**

## 6. Simulations Results

The proposed and conventional circuits are designed in TSMC 180 nm CMOS technology and simulated in PSpice simulator with supply voltage of 1 V and bias current of 0.1 mA. The aspect ratio (W/L) of transistor $M_1$ is selected as 30 and of transistor $M_2$ as 20.

In this work, improvement in the bandwidth of proposed circuits using gate-body driven technique is expressed in terms of the factor bandwidth extension ratio (BWER), obtained using following expression

$$BWER = \frac{Bandwidth\ of\ improved\ circuit}{Bandwidth\ of\ conventional\ circuit} \tag{45}$$

Figure 13 shows the frequency response of conventional and improved FVF. The -3 dB frequency of 914.460 MHz and 2.391 GHz is obtained for the conventional and improved FVF respectively. Thus the BWER of 2.614 is obtained using gate-body driven technique. It is observed from Fig. 13 that, frequency response of improved FVF has sharp tail edge as compared to conventional FVF. This is mainly due to the fact that body effect in transistor $M_1$ has been utilized by connecting body and gate terminals together, resulting in higher transconductance and lower threshold voltage. One important advantage of lower threshold voltage of $M_1$ is increased gate overdrive voltage ($V_{gs}$-$V_T$). For the improved FVF, simulated DC power dissipation is 0.1 mW, input impedance of 868.231 kΩ and output impedance of 138.227 Ω is obtained. Simulated results of improved and conventional FVF are summarized in Table 2. As observed from Table 2, main difference between conventional and improved FVF is higher bandwidth of 2.391 GHz whereas, for same aspect ratio and biasing conditions, bandwidth of conventional FVF is 914.460 MHz. At the same time, gate-body driven technique has achieved this BWER without degrading input and output impedance of FVF. The gate-body driven technique has not increased any appreciable power consumption in the improved FVF.

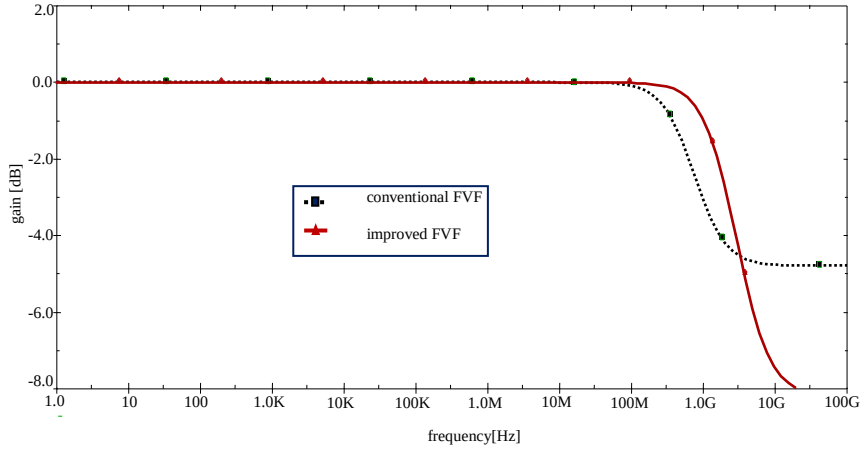


**Fig. 13. Frequency response of conventional and improved FVF.**

Figure 14 shows the frequency response of current mirror using conventional and improved FVF. Aspect ratio of $M_3$ is selected same as $M_2$. For conventional current mirror, -3 dB frequency of 178.720 MHz is obtained. Using improved FVF in the current mirror, -3 dB frequency of 422.753 MHz is achieved with a small amount of peaking. Thus using gate-body driven technique, a BWER of 2.365 is obtained in the current mirror.

**Table 2. Simulated results of the conventional and improved FVF.**

| **Parameter** | **Conventional FVF (Fig.3)** | **Improved FVF (Fig.4)** |
|---|---|---|
| **CMOS Technology** | TSMC 0.18µm | TSMC 0.18µm |
| **Supply voltage** | 1V | 1V |
| **Input impedance** | 852.537 kΩ | 868.231 kΩ |
| **Output impedance** | 157.613 Ω | 138.227 Ω |
| **Bandwidth** | 914.460 MHz | 2.391 GHz |
| **Static power consumption** | 0.08mW | 0.1mW |

The parasitic capacitances in CMOS circuits introduce zeros which results in peaks in the frequency response. It can be observed from Fig. 14 that there is slight peaking in frequency response of proposed current mirror circuit. This may be due to the zero introduced by additional parasitic capacitance in current mirror. Table 3 summarises the BWER in improved FVF and in a current mirror designed using improved FVF. From the results we conclude that gate-body driven technique is very effective for designing low voltage wideband analog integrated circuits.

**Table 3. BWER in conventional and proposed circuits.**

| | **FVF** | **Current Mirror(CM)** |
|---|---|---|
| **-3dB frequency** | Conventional: 914.460 MHz<br>Improved: 2.391GHz | Conventional: 178.720 MHz<br>Improved: 422.753MHz |
| **BWER** | 2.614 | 2.365 |

Table 4 gives a comparison of gate-body driven technique used for enhancing the bandwidth of FVF with other techniques reported in the literature. As seen from this table, the highest BWER is obtained using gate-body driven technique as compared to existing FVF bandwidth enhancement techniques. The main issue with existing FVF bandwidth enhancement techniques is that BWER is dependent on the numerical value of the inductor and/or resistor. For obtaining higher value of BWER, a large value of these passive components is required which not only increases the chip area but also difficult to implement.

**Table 4. Comparison of bandwidth enhancement techniques of FVF.**

| **Parameter** | **[ 12 ]** | **[13 ]** | **[13]** | **This work** |
|---|---|---|---|---|
| **Bandwidth enhancement technique** | Use of on-chip resistor | Use of on-chip inductor | Use of on-chip resistor in series with inductor | Use of gate-body driven technique |
| **Power supply** | 1.5V | 1.5V | 1.5V | 1V |
| **Technology** | 0.18µm CMOS from TSMC | 0.18µm CMOS from TSMC | 0.18µm CMOS from TSMC | 0.18um CMOS from TSMC |
| **DC Power dissipation** | NA | NA | 5.564µW | 0.1mW |
| **Output impedance** | NA | NA | 173.7 Ω | 138.227 Ω |
| **Input Impedance** | NA | NA | NA | 868.231 k Ω |
| **BWER** | 1.4 (for R = 1.8 kΩ) | 1.99 (for L = 5nH) | 2.26 (for L = 5nH and R = 10 kΩ) | 2.614 |

*NA-not available

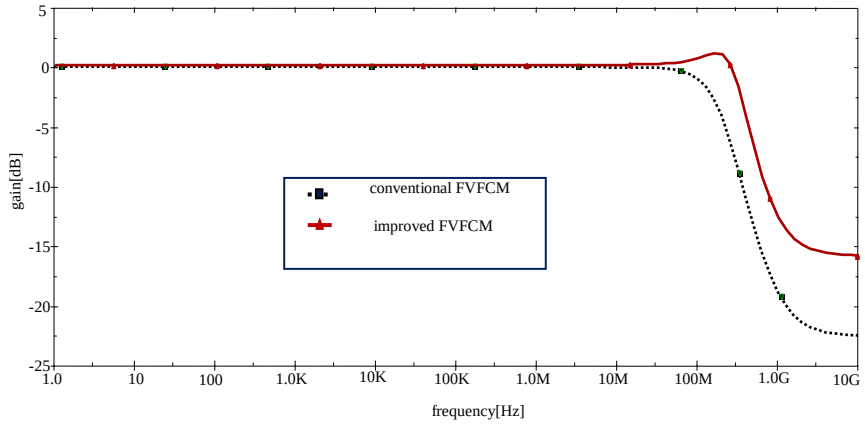


**Fig. 14. Frequency response of conventional and improved FVF based current mirror(CM).**

## 7. Conclusion

A high bandwidth FVF using gate-body driven technique has been proposed in this work. The body effect present in conventional FVF has been utilized using to improve the performance of FVF in terms of bandwidth and impedance. The newly developed FVF accounts for very large bandwidth, high input impedance and low output impedance. This is achieved with the same static power dissipation, very small additional circuit complexity and lower distortion/peaking. Simulation results agree with analytical predictions. It is shown in the work that gate-body driven technique enhances the bandwidth by more than twice in the proposed circuits and thus improved FVF is more suitable for designing wideband low voltage and low power analog integrated circuits.

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