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DESIGN AND ANALYSIS OF STATIC RANDOM ACCESS MEMORY BY SCHMITT TRIGGER TOPOLOGY FOR LOW VOLTAGE APPLICATIONS

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Abstract

Aggressive scaling of transistor dimensions with each technology generation has resulted an increased integration density and improved device performance at the expense of increased leakage current. The Supply voltage scaling is an effective way of reducing dynamic as well as leakage power consumption. However the sensitivity of the circuit parameters increases with reduction of the supply voltage. SRAM bit- cells utilizing minimum sized transistors are susceptible to various random process variations. The Schmitt Trigger based operation gives better read-constancy as well as superior write-ability compared to the standard bitcell configurations. The proposed Schmitt Trigger based bitcells integrate a built-in feedback mechanism make the process with high tolerance. In this paper an obsolete design of a differential sensing Static Random Access Memory (SRAM) bit cells for ultralow-power and ultralow-area Schmitt trigger operation is introduced. The ST bit cells incorporate a built-in feedback mechanism, provided by separate control signal if the feedback is given by the internal nodes, achieving process variation tolerance that must be used for future nano-scaled technology nodes. In this we proposed 32nm technology for designing 10T SRAM cell using Microwind.Total power about 30% is reduced due to 32 nm technology as compared to 65 nm technlology.

Keywords: Low-voltage SRAM, Schmitt-Trigger (ST), Process variation tolerance, Read stability.

1. Introduction

Aggressive scaling of transistor dimensions has resulted in increased integration density and improved performance with each technology generation. This will make a tremendous increase of the active power dissipation. In addition, increased

leakage power forms a significant portion of the total power dissipation with scaling. As a result, total power dissipation has become a crucial design constraint in the present designs. The power consumption requirement in "mobile" devices such as cell-phones and medical devices is even more stringent for extending the battery operating lifetime. Hence the need for ultra-low power designs is ever increasing with scaling of the transistor dimensions. Power reduction methods include: voltage scaling, switching activity reduction architectural techniques of pipelining and parallelism.

Among these methods, power supply reduction has significant effect on power savings. Reducing the supply voltage reduces thermodynamic power quadratically and leakage power linearly to the first order. Hence supply voltage scaling has remained the major focus of low power design. For circuits requiring ultra low power dissipation, researchers have developed circuit techniques to operate circuits in the sub threshold regime. Work on such digital circuit design with supply voltage less than the transistor threshold started back in 1999 [1].

Low power device design is now a vital field of research on account of increase in demand of portable devices. Environmental monitoring or emerging miniaturized energy autonomous systems e.g, for healthcare especially require circuits with extremely tight energy budgets to enable functionality at practical device sizes, motivating further research in this direction [2]. Active power reduction is a critical challenge to translate increasing levels of integration to architectural performance enhancement [3]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly [4]. The supply voltage scaling is the major focus of low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a MOS. Sub-threshold current of a MOSFET device occurs when the gate-to-source voltage of the device is lower than its threshold voltage [5].

The Schmitt Trigger (ST) is a comparator that incorporates positive feedback. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. ST is used to modulate the switching threshold of an inverter depending on the direction of the input transition. The output state depends upon the input level and will change only as the input crosses a predefined circuit threshold. Therefore Schmitt Triggers are bistable networks that are widely used to enhance immunity of circuits to noise and disturbances [6]. The ST circuit has a dc transfer characteristic like an inverter, but with different switching thresholds depending on whether input signal is increasing or decreasing. ST can be used as a CMOS logic inverter. It has a number of applications in sub-threshold SRAM frequency doublers image sensors [7].

2. Static Random Access Memory

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data reminisce, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

Four-transistor SRAM shown in Fig. 1, is quite common in stand-alone SRAM devices (as opposed SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors. A typical SRAM cell is made up of six MOSFETs shown in Fig. 2. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4T, 8T, 10T, or more transistors per bit.

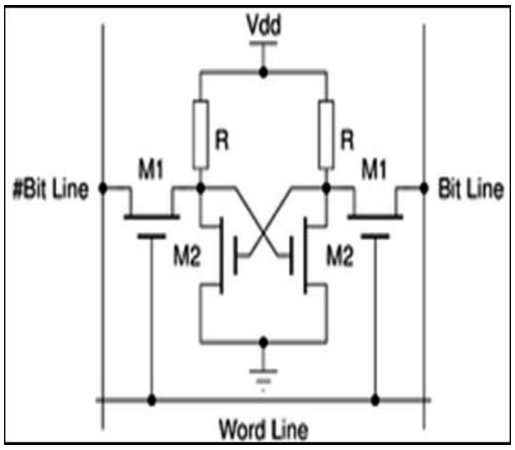

Fig. 1. Four transistor SRAM cell.

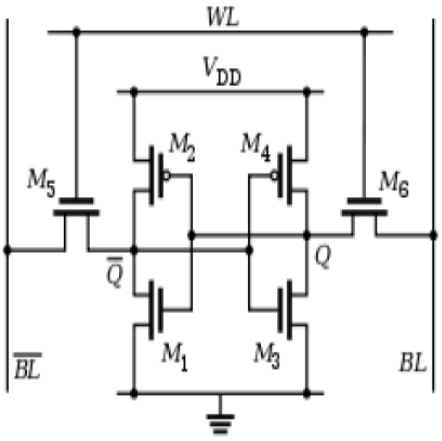

Fig. 2. CMOS six transistor SRAM cell.

An SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows.

2.1. Standby

If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

2.2. Reading

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and Q‘ are transferred to the bit lines by leaving BL at its pre-charged value and discharging BL‘ through M1 and M5 to a logical 0 (i.e. eventually discharging through the transistor M1 as it is turned on because the Q is logically set to 1). On the BL side, the transistors M4 and M6 pull the bit line toward VDD, a logical 1 (i.e. eventually being charged by the transistor M4 as it is turned on because Q is logically set to 0). If the content of the memory was a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then these BL and BL will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier, the faster the speed of read operation is.

2.3. Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

3. 6T SRAM Cell

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 (4T, 8T, 10T SRAM), or more transistors per bit. Conventional 6-Transistor (6T) cell shown in Fig. 3, uses a cross-coupled inverter pair is the de facto memory bitcell used in the current SRAM designs.6T cell mainly utilize differential read operation The memory cell in SRAM consists of two static inverters that feed into each other creating a latch. Access transistor logic is used for controlling the access into the memory cell and the switching for the transistor logic is controlled by word lines. By modulating the virtual-VCC

and virtual-VSS of one of the inverters the write ability will be achieved. In all the existing bit cell configurations the cross-coupled inverter pair plays a vital role. To decouple the read and write operations we need to add the extra transistors. None of the existing bit cells incorporate process variation tolerance for improving the stability of an SRAM bit cell. The stability of the cross-coupled inverter will decides the SRAM operation under PVT variations. However, the bit cell stability can not be affected by the device sizing at very low supply voltage. The design and the cracteristics of 6T SRAM cell are shown in Figs. 4 and 5.

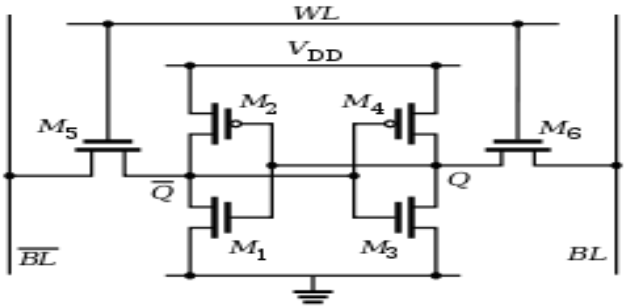

Fig. 3. Conventional 6T SRAM cell.

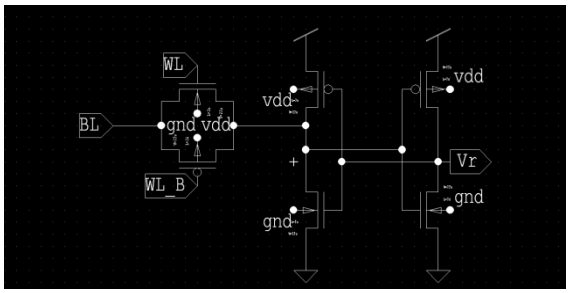

Fig. 4. Design of 6T SRAM cell.

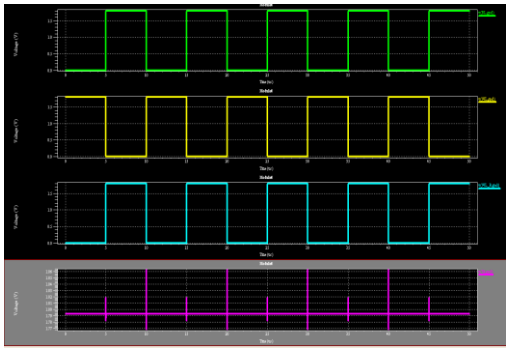

Fig. 5. Characteristics of 6T SRAM cell.

4. Memory Cell Operations

Read Operation: Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is pre-charged to VDD. The read word line RL is then asserted to VDD. The storage node Q' that stores a 1 is statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q' will be 0 and MRA will be in cutoff and the bit line BL would not be able to discharge through MRD to Gnd, and it would read a 1.

Figure 6 shows the 6T SRAM equivalent schematic diagram during read operation. Bit lines are pre charged to supply voltage before read operation. The read operation is initiated by enabling the word-line (WL) and thereby connecting the internal nodes of the SRAM bitcell to bit-lines. The bit line voltage is pulled down by the nMOS transistor at the '0' storage node and the difference between two bit line voltages will be detected by sense amplifier. When the word line(WL) is high, one of the bit line voltages is pulled down through transistors M2 and M6 or M1 and M4. The transistors M2 and M6 forms a voltage divider, because of current flowing through M2, the potential at node QB is no longer at '0'V. Also it should not go beyond switching threshold of inverter (INV1) to avoid destructive read. The rising of potential depends on sizing of access transistor and pull down transistor which is defined as a bitcell ratio.

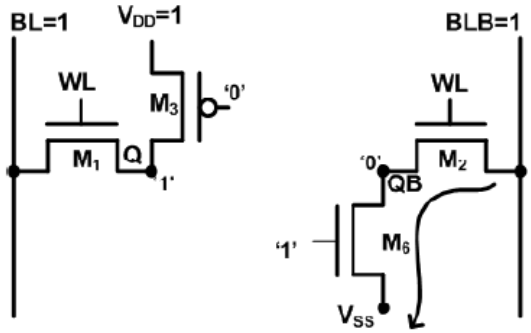

Fig. 6. Memory read and write equivalent circuit.

Write Operation: The word-line WL is charged to VDD as in 6TStandard SRAM. Since NMOS is a stronger driver than PMOS, no problem is incurred while writing a 0 into the cell. The absence of the pull down NMOS for memory node Q allows writing a 1 into the cell easily. Writing a 1 is done by pre-charging bit-line BL to VDD. While writing 0, the bit-line BL is discharged and then word-line WL is charged to VDD as in 6T Standard SRAM. The write operation begins by forcing a differential voltage (V*DD*, and 0) at the bitline pairs (BLB and BL). This differential voltage corresponds to the data to be written at the storage nodes (Q and QB) and it is controlled by the write drivers. The WL is then activated to store the information from the bit-line pairs to corresponding storage nodes. Assume, the nodes Q and QB initially store values '1' and '0' respectively. When the WL is asserted the access transistor (M1) connected to BL (at '0') is turned

on, a current flows from V*DD* to BL through M3 and M1. This current flow lowers the potential at Q. The potential at the node Q has to go below the trip point of the inverter (INV2) for a successful write operation and this depends on the ratio of pull-up transistor (M3) and the access transistor (M1). This ratio is referred to as the pullup- ratio.

Hold Operation: If the cell content is a 1 (Q=VDD, Q'=0), both memory nodes will lock each other at their respective voltages. However, if the cell content is a 0 (Q=0, Q'= VDD), Q is floating. Referring to Fig. 7, the leakage current through M5 must be greater than that of M2 to ensure Q stays at 0. Fortunately, since NMOS (M5) is a stronger current driver than PMOS (M2), this condition is satisfied. When WL goes low , SRAM bitcell is in data retention mode. Two cross coupled inverters hold the data, through bistable action. There is destruction in data stored when V*DD* goes below certain voltage, which is called data retention voltage of SRAM bitcell .A standard 6T SRAM shows poor read stability as technology scale down to nano-regime. To increase the read stability (measured by read SNM) conventional device sizing can be followed by increasing the bitcell ratio. By increasing the bitcell ratio, read SNM and critical charge (node capacitance) will increase which are desirable. However, at the same time power consumption and write time increases which are not desirable features, as they incur loss of power, performance and increase in area overhead. In Table I it is shown that when we are increasing the bitcell ratio there is significant increase in write time, which will affect the performance of SRAM bitcell.

5. 7T SRAM Cell

The Schematic diagram, Simulation, and characteristics of 7T SRAM cell are shown in Figs. 7, 8, and 9 respectively. In the single-ended 7T bitcell consists of single-ended write operation and a separate read port. The single-ended write operation in this 7T bitcell needs either asymmetrical inverter characteristics or differential VSS and VCC bias. The proposed another single-ended 7T bitcell in which an extra transistor is added in the pull-down path of one of the inverters. During this read mode, to isolating the corresponding storage node from VSS when the extra transistor is turned OFF. This gives results in read-disturb-free operation. The feedback between the two inverters is cut off during the write operation in differential 7T bitcell. The successful write operation in an inverter sizing produces asymmetrical noise margins. The extra transistors are added to the conventional 6T bitcell to separate read and write operation, it gives the single-ended 7T bitcell.

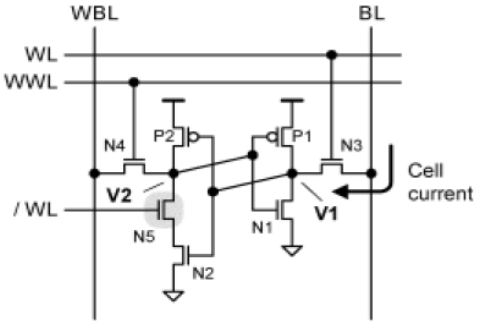

Fig. 7. Schematic diagram of 7T cell design.

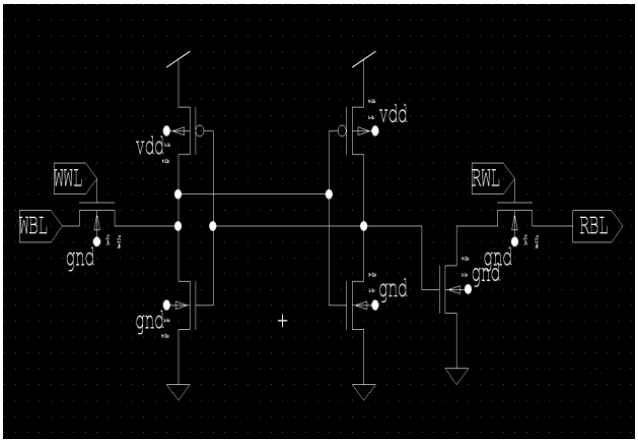

Fig. 8 Simulatio of 7T SRAM cell.

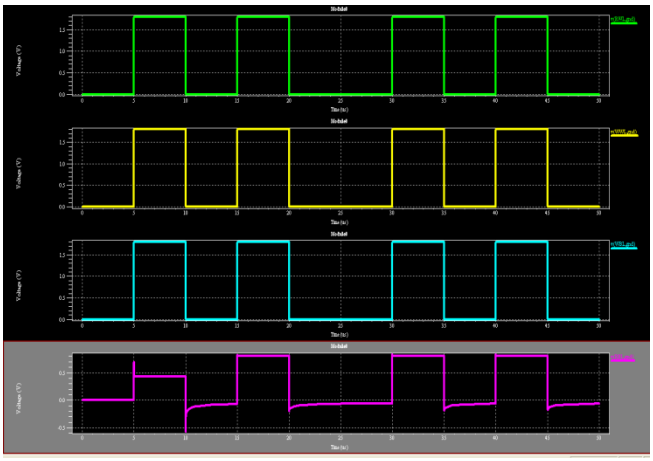

Fig. 9. Characteristics of 7T SRAM cell.

6. 8T SRAM Cell

The Schematic diagram, Simulation, and characteristics of 8T SRAM cell are shown in Figs. 10, 11, and 12 respectively. Figure 10 shows the architecture of new 8T SRAM cell. It consists of two extra transistors MNLL and MNWL as compared to conventional 6T SRAM cell. Transistor MNLL is used to reduce gate leakage while transistor MNWL is used to make cell SNM free in the zero state. Interestingly, transistor MNLL also helps in improving SNM when cell holds logic '1'. The signWLB is the complement of wordline (WL) signal. The timing diagram for signal WL and WLB in read/write cycle and standby mode is shown in Fig. 12. In this work, the basic read/write operations of 8T SRAM cell are preformed using single ended sense amplifier. which are described as follows.

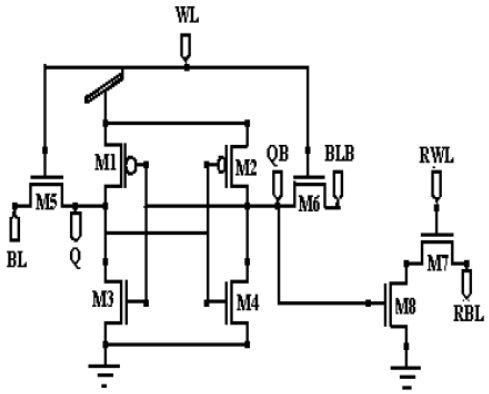

Fig. 10. Schematic of 8T SRAM cell.

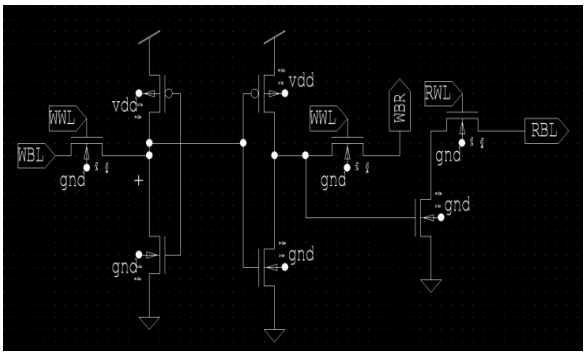

Fig. 11. Simulation of 8T SRAM cell.

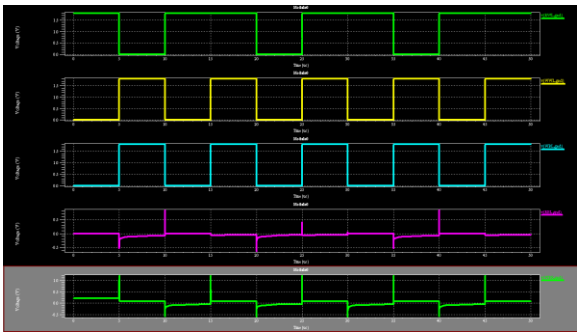

Fig. 12. Characteristics of 8T SRAM cell.

In write '0' operation, the bitline BT is pulled down to logic '0'. As soon as the signal WL rises from logic '0' to logic '1', transistor MNWL is turned off. The node XT starts discharging which turns on transistor MP2 causing cell to flip and logic '0' is written into the cell. In write '1' operation, the bitline BB is pulled down to -VTN, where VTN is the threshold voltage of transistor MN4. The node XB starts discharging which turns on transistor MP1. Once transistor MP1 is turned on, the node XT is at logic '1' and hence logic '1' is written into the cell.

In read operation, the bit lines BT and BB are held at logic '1' by the pre charged circuitry. In read '0' operation, the bit line BT starts discharging through transistors MN3 and MN1.

The single ended 8T SRAM circuitry is being used for making an SRAM memory since the usage of SRAM Cell is in cache memory. For generating a memory, there is a requirement of Address decoder, Data write circuitry and data Read Operation. Since the proposed circuitry do not require pre charge circuit, so there is no elaboration of pre charge circuitry as in 6T SRAM Cell. The memory has been designed for 32 bit storing capacity for read and writes operation. At a time, 8 bits will be activated for read or write purpose. The selection of word line represents the selection of a particular row. The data lines of the cells form the column of the memory matrix. For read operation, the Read Bit line (RBL) is also included to form a separate read column of the memory matrix. The data flow is thus visualized to be vertical for both read and write operations. Once a word line is driven high by the row decoder, every cell in the row is accessible. 8T SRAM cell has the normal 6T SRAM design with a read decoupled path consisting of two NMOS transistors M5 & M6. Read operation of 8T SRAM is initiated by pre-charging the read bit line to full swing voltage. After pre-charging read bit line, RWL is asserted that drives access transistor M5 on. If Q=0 then M6 is on & RBL discharges through transistors M5 & M6 to ground. This decrease in the voltage of RBL is sensed by the sense amplifier. During read „1" operation, when Q="1" M6 remains off so there will be no discharge current flow through the read path. In this situation only a very small amount of leakage current flows which is called bit line leakage. Write operation of 8T cell is similar to 6T cell but the pre-charge circuitry at the bit lines is replaced by write driver.

7. 9T SRAM Cell

The schematic diagram, simulation, and characteristics of 9T SRAM cell are shown in Figs. 13, 14, and 15 respectively. Standard 6T bitcell along with three extra transistors were employed in nine-transistor (9T) SRAM bitcell, to bypass read-current from the data storage nodes, as shown in Fig. 13. This arrangement yields a non-destructive read operation or SNM-free read stability. However, it leads to 38% extra area overhead and a complex layout. Thin cell layout structure does not fit in this design and introduces jogs in the poly.

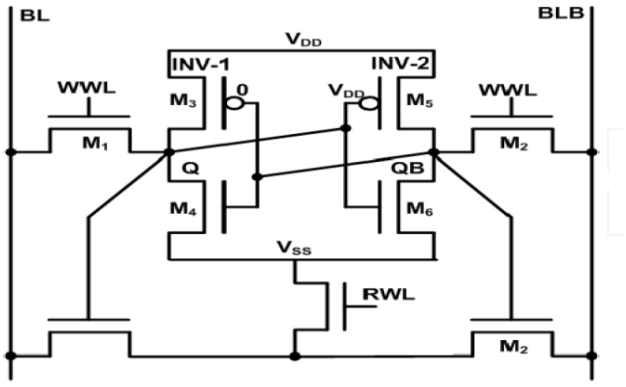

Fig. 13. Schematic diagram of 9T SRAM cell.

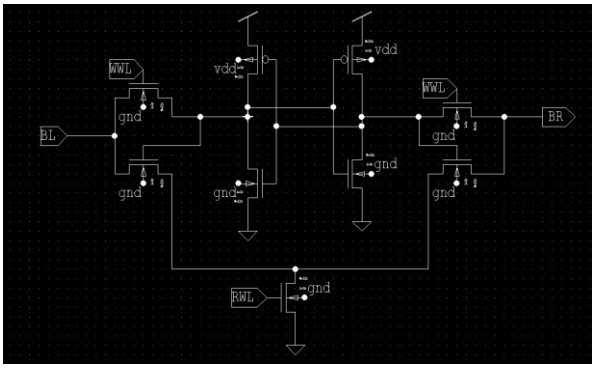

Fig. 14. Simulation of 9T SRAM cell.

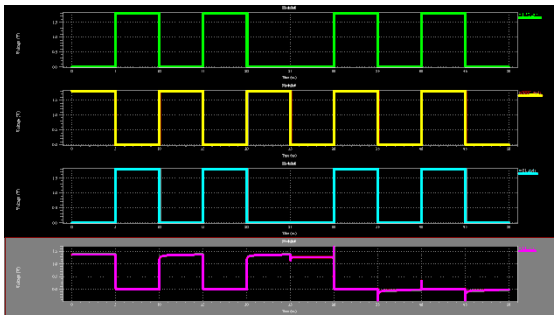

Fig. 15. Characteristics of 9T SRAM cell.

8. 10T SRAM Cell

The schematic diagram, simulation, and characteristics of 10T SRAM cell are shown in Figs. 16, 17, and 18 respectively. In the proposed 10T SRAM bit cell, as shown in Fig. 16, a separate read port comprised of 4-transistors was used, while write access mechanism and basic data storage unit are similar to standard 6T bit cell. This bit cell also offers the same benefits as the 8T bit cell, such as a non-destructive read operation and ability to operate at ultra low voltages. But the 8T bit cell does not address the problem of read bit line leakage current, which degrades the ability to read data correctly. In particularly, the problem with the isolated read-port 8T cell is analogous to that with the standard (non-isolated read-port) 6T bit cell discussed. The only difference here is that the leakage currents from the un-accessed bit cells sharing the same read bit-line, RBL, affect the same node as the read-current from the accessed bit cell. As a result, the aggregated leakage current, which depends on the data stored in all of the un accessed bit cells, can pull-down RBL even if the accessed bit cell based on its stored value should not do so. This problem is referred as an erroneous read. The erroneous read problem caused by the bit line leakage current from the un-accessed bit cells is managed by this 10T bit cell by providing two extra transistors in the read-port. These additional transistors help to cut-off the leakage current path from RBL when RWL is low and makes it independent of the data storage nodes content. Table 1 shows the power at room temperature.

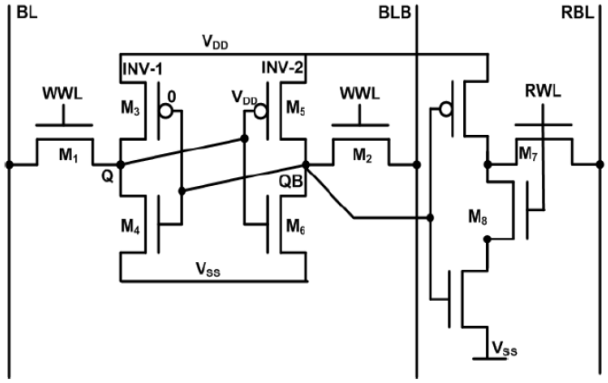

Fig. 16. Schematic diagram of 10T SRAM cell.

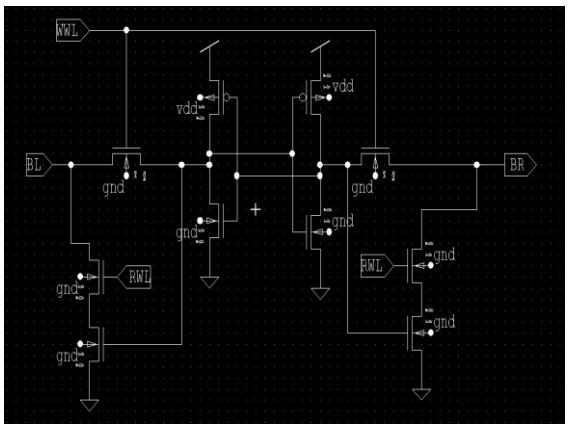

Fig. 17. Simulation of 10T SRAM cell.

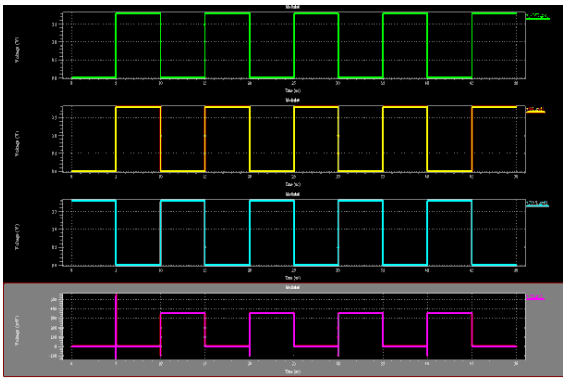

Fig. 18. Characteristics of 10T SRAM cell.

The following table shows the power at room temperature.

Table 1. Analysis of Power Dissipation in Various SRAM Cell Design

No. of transistors	Maximum power (Static power)	Minimum power (Dynamic power)	Average power
4T	0.2470	2.4538×10^{-5}	1.34938
5T	0.0884	7.6206×10^{-5}	0.1419
6T	0.2538	3.8429×10^{-4}	13.766
7T	0.2539	8.7852×10^{-4}	11.654
8T	0.29999	6.1198×10^{-4}	11.377
9T	0.06566	2.8716×10^{-5}	1.1049
10T	0.03518	7.6498×10^{-5}	1.6739

9. Conclusion

Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically. However, as the supply voltage is reduced, the sensitivity of circuit parameters especially temperature to process variations increases. Lowering the supply voltage is an effective way to achieve ultra-low-power operation. In this work, we evaluated different types of ST-based SRAM bit cells suitable for ultra-low voltage applications. In this paper, Simulation results of 4T/5T/6T/8T/9T/10T SRAM bitcell topologies are analyzed for achieving low voltage and low power operation at room temperature.

The simulation waveforms shows that the proposed design of SRAM cell dissipates lesser power at different bitcell design and better stability, than the other existing SRAM cells. Although transistor count and area are increased in comparison to those of other SRAM cells but total low power dissipation, dynamic power, static power and supply voltage variation can easily dominate over this drawback. This proposed 10T SRAM cell can be used to provide low power solution in high speed devices.

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