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DESIGN OF AN ARRAYED WAVEGUIDE GRATINGS BASED OPTICAL PACKET SWITCH

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Abstract

Optical packet switching is considered as the future of data transfer technology in combination with middle-aged electronics. The biggest challenge encountered in optical packet switching is the lack of optical buffers for storing the contending packets. Therefore, for the contention resolution of packets, a temporary storage in terms of fiber delay lines is used. This task is accomplished by an optical packet switch. In this paper, a design modification in the AWGR (Arrayed Waveguide Grating Router) is presented for improving the switch performance. The power budget analysis of the switch is also presented to estimate the sufficient power level of the switch. The obtained results clearly reveal that the architecture presented in this paper can be operated in micro-watts in comparison to the earlier optical switch which operates in milli watts regime. Finally, simulation results are presented to obtain packet loss probability and average delay. Even at the higher load of 0.6, the switch presented in this paper provides a very low loss probability (10^{-6}) and delay remain within 2 slots.

Keywords: Arrayed Waveguide Grating, Optical Packet Switch, BER, TWC, Power budget.

1. Introduction

With the increasing demand of higher bandwidth, the use of optical switching in information transfer seems to be one of the viable solutions. In the current electronic communication environment for data transfer, packet switching is used very efficiently. Thus, one of the simplest and most natural extensions of packet switching over optics is the optical packet switching. Optical packet switching provides a connectionless networking solution, which produces optimum bandwidth utilization using wavelength division multiplexing (WDM) technique [1]. In the op-

Nomenclatures

A_{eff}	Effective area of fiber, m^2
B_e	Electrical bandwidth, GHz
B_o	Optical bandwidth, GHz
c	Speed of light, *m*/*s*
e	Electronic charge, coulomb
G	Gain of the amplifier
h	Plank Constant, Joule-sec
L_{TWC}	TWC insertion loss, dB
$L_{AWG}^{2N\times 2N}$	Loss of Scheduling AWG (32 channels), dB
$L_{AWG}^{N\times N}$	Loss of Switching AWG (32 channels), dB
L_{FDL}	Loss of the fiber loop, dB
L_{SOA}	Loss of SOA, dB
N	Size of the Switch
P_{in}	Input Power, watts
P_{out}	Output Power, watts
P_s	Power entering in to the buffer module, watts
R	Responsivity, Ampere/watts

Greek Symbols

η	Refractive index of fiber
η_{sp}	Population inversion factor
σ_s^2	Shot noise
σ_{th}^2	Thermal noise
σ_{sp-sp}^2	ASE-ASE beat noise
σ_{sig-sp}^2	sig-ASE beat noise
σ_{s-sp}^2	shot-ASE beat noise

Abbreviations

AWG	Arrayed Waveguide Gratings
BER	Bit Error Rate
FDL	Fiber Delay Lines
OPS	Optical Packet Switch
SNR	Signal to Noise Ratio
TWC	Tunable Wavelength Converter

tical packet switching, optical implementations of all the switching functions are not technologically possible and hence due to these technological limitations a hybrid approach is used, where data transfer takes place in optical domain and controlling is done electronically.

In the optical packet switching technology, data is transmitted in the form of optical packets, which contain two distinct parts header and payload. The header contains addressing and control information and the payload stores the actual data. The one of the major issues in the optical packet switching technology is the contention among packets, which arises when different

packets enter the same egress port on the same wavelength and at the same time for a common output port. This can be resolved either by wavelength conversion or by introducing an optical domain (FDL) temporary storage for the contending packets [2].

The performance of an optical packet switch depends on optical loss, noise, crosstalk; etc. These factors degrade the functioning of the switch and thus increase the bit error rate. Hence, it is necessary that switch should have very simple designs with the least number of components so that SNR can be kept as higher as possible. This paper discusses an AWG based optical packet switch, which can be very efficiently used for the buffering of contending packets. The switch is realized by using a very less number of components. In this paper, the switch design modification is detailed and power budget analysis is discussed in the BER analysis of the switch. Finally, simulation results are presented to obtain packet loss probability and average delay performance of the switch.

The main hurdle in the deployment of OPS systems is the unavailability of tunable optical components, especially tunable wavelength convertors. However, in labs these components exist and very soon they will be commercialized. The other components used in the switch are pieces of fiber and AWG. These two components are available in market.

This paper is organized as follows. In section 2, authors discuss the related work. In section 3, architecture modification is detailed. In section 4 loss, power and noise analysis of the switch is presented. In section 5, simulation results in terms of packet loss probability and average delay are presented. In section 6, cross layer optimization is detailed. Finally, in section 7 major conclusions of the paper along with future scope is detailed.

2. Related Works

In the past, numbers of optical packet switch architectures were presented, but it is not possible to cover all of them. In this section, some of the pioneer switch architectures, which are heavily investigated due to their advantages over others, are presented.

Hunter et.al, proposed an AWG based switch. In this switch the Arrayed Waveguide Grating router is used to route the packets, either to the buffer or to the appropriate output directly [3] (Fig.1). The contending packets are placed in the buffer, where they are delayed using the FDL of the length varying of integral multiples of time slot 'T' with a maximum of 'DT' delays. It must be remembered that from each FDL structure only one packet can enter/leave in a single time slot. Packets can also be recirculated in the buffer by tuning the buffer TWCs appropriately. This design assumes the limited tunable range of TWCs, therefore TWCs also considered at the input of switching switch.

Chia et al. [4] and later Rastegarfar et al., [5] design a switch which is AWG based switch and it uses wavelength routing efficiently. The switch uses the static permutation nature of AWG to switch packets from input to output ports [4] (Fig. 2). This architecture is the simplified version of the Hunter architecture. Here, wide range TWCs are considered, therefore, appropriately

tuning of the buffer or inputs TWCs of the scheduling AWG packets can be easily routed to the outputs. In this architecture the priority routing can be implemented in the effective manner. For buffering, switch uses shared feedback delay lines and these lines are used to store the contended packets and also give priority to the packets so that high priority packets allow pre-empting the low priority packets. The number of fiber delay lines, which are necessary for required cell loss probability dependents on the traffic statistics, like Bernoulli, Poisson or Bursty, etc. In both the architecture, considering that 'N' upper ports are used for the buffering of packets, then a total of 'ND' packets can be stored. In recent past, various AWGR based optical packet switch are proposed, with different permutation and combinations of buffer; for detailed about these switches see [5-7].

Author of this paper, R. Srivastava et al. [8], proposed a simplified version of the above mentioned architectures and defined as D1, in Fig. 3.

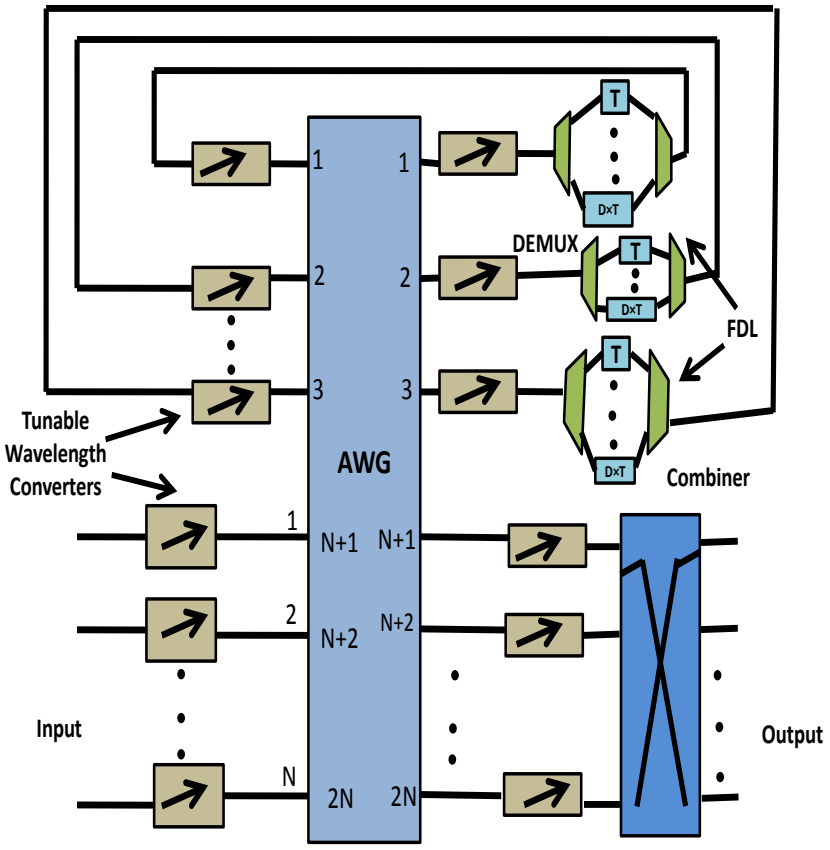

Fig. 1. Optical switch [3].

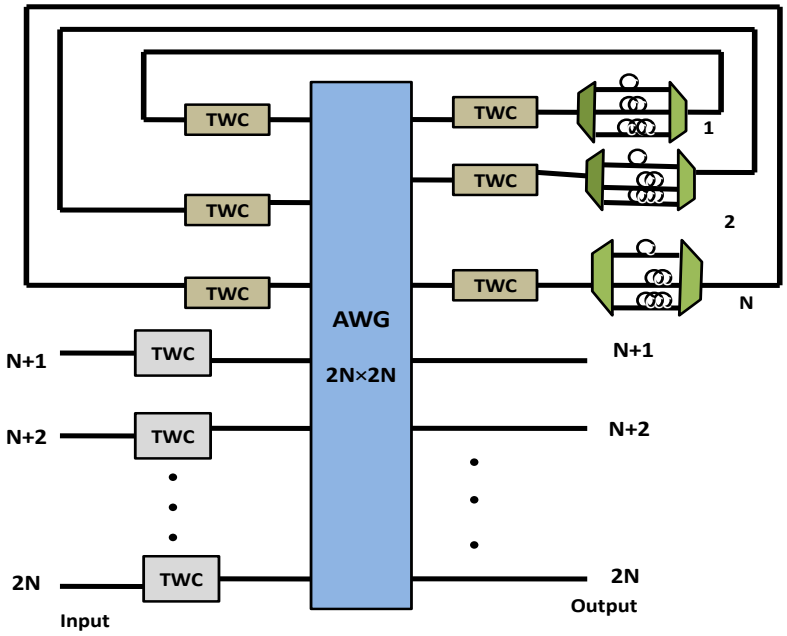

Fig. 2. Optical switch [4].

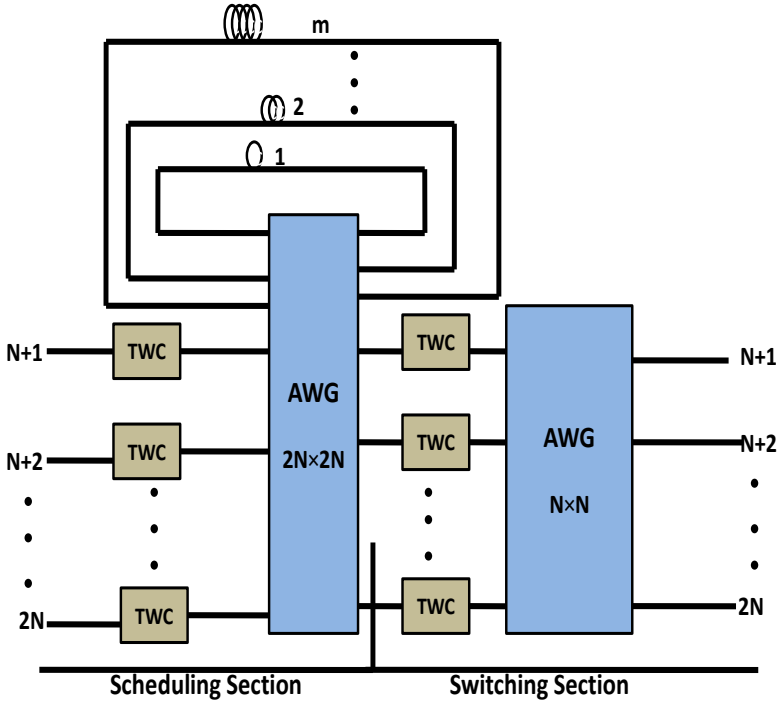

Fig. 3. Optical switch, (D1) [8].

In the architecture D1; the switch is divided in the scheduling and switching section. The scheduling section contains the TWCs, one 2N×2N AWG router, FDL lines for buffering of packets, and the switching section contains TWCs and an N×N AWG router [8]. The upper 'N' ports of scheduling AWG are connected to the 'N' FDL buffer modules. The other ports (N+1 to 2N) are actual input output ports. The input ports are equipped with the tunable wavelength converters (TWCs), and these TWCs are used to tune the wavelength of incoming packets as per the requirement of output packets. Suppose a packet arriving at input '*i*' and destined to the output '*j*' with required amount of delay of '*k*' time slots then the packet is routed to the k^{th} buffer module. To do so, the wavelength of the incoming packet is tuned as per the routing pattern of the cyclic AWG,

$$\lambda(i,k) = \lambda_i$$

$$l = [1 + (i + k - 2) mod\ N]$$

The packet which is deflected through kth buffer module will again re-appear after the delay of 'k' time slots at the input port of scheduling AWG and due to the symmetric nature of scheduling AWG the packet get routed to the output port '*i*' of the scheduling AWG, and finally the packet is forwarded towards the appropriate output '*j*' by tuning wavelength appropriately in the switching section.

3. Architecture Modifications

3.1. Description of architecture D1

In the architecture, *2N×2N*, AWG is considered, with '*N*' input and '*N*' output ports. Thus, maximum '*N*' ports can be used for the buffering of packets. In each buffer module '*N*' packets will be stored one for each output. Thus, in '*N*' modules N^2 packets can be stored.

The main problems with the above architecture D1 are:

a) The packet, which will directly pass through the switch, will suffer lesser loss in comparison to the packets which will first go through the buffer and then to the output. Hence, the direct packet will have better signal quality in comparison to the buffered packets.

b) The buffered packets will also suffer different loss, as the length of each buffer module is different.

c) As different packet will suffer different losses, hence the optimum receiver design is not possible.

3.2. Description of architecture D2

To combat the above stated problems, design modification is possible in the architecture D1. As a modification (Fig. 4, Architecture D2) SOA (Semiconductor Optical Amplifier) can be placed in each branch of the buffer. As SOA's are variable gain optical amplifier (tuning speed ns), the loss of the each buffer module can be fully compensated by the gain of corresponding SOA. This modification will make sure that each received packet has the same optical power when they received at the output of the switch.

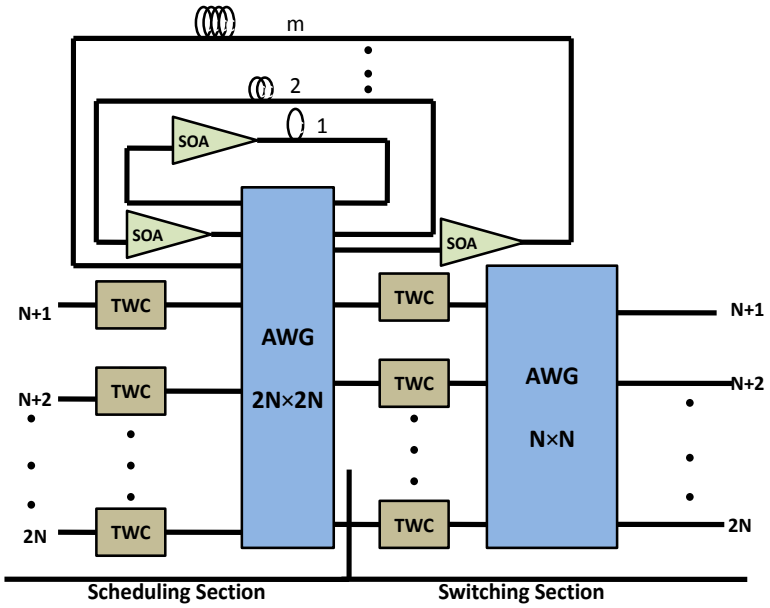

Fig. 4. Design of AWG based switch D2.

4. Analysis of the Switches

4.1. Analysis of switch architecture D1

The Loss Analysis of the architecture (shown in Fig. 3) is presented in this sub-section. The packet, which directly passes through the switch, and the packets, which arrive at the output via buffer, suffers different loss.

Case1: The loss analysis if the packet passes through the buffer

For the mathematical abstraction point of view the switch D1, can be divided into three distinct parts as input unit, buffer unit and output unit.

The loss of the input unit which consist of TWC can be written as

$$A_{in} = L_{Twc} \tag{1}$$

The loss of the buffer can be calculated as

$$A_b = L_{AWG}^{2N\times 2N}\, L_{FDL} \tag{2}$$

Here, $L_{AWG}^{2N\times 2N}$ is loss due to the scheduling AWG L_{FDL} is the loss due to the fiber delay lines.

Similarly, the loss of the output unit which consist of the switching and scheduling AWG and TWC can be obtained as

$$A_{out} = L_{AWG}^{2N\times 2N}\, L_{TWC} L_{AWG}^{N\times N} \tag{3}$$

Combining all the above Eqs. (1), (2) and (3), the total loss of the switch can be written as

$$A_T = A_{in}A_bA_{out} \tag{4}$$

Equation (4) shows the total loss of the switch when packets pass through the buffer unit.

Case2: The loss analysis if the packet directly passes through the output unit

The loss of the input unit which consist of TWC can be written as

$$A_{in} = L_{Twc} \tag{5}$$

Loss due to the scheduling AWG can be written as

$$A_{sch} = L_{AWG}^{2N\times 2N} \tag{6}$$

And the loss of the output unit can be calculated as

$$A_{out} = L_{TWC}L_{AWG}^{N\times N} \tag{7}$$

The total loss of the switch when packets pass directly without entering in the buffer is

$$A_T = A_{in}A_{sch}A_{out} \tag{8}$$

4.1.1. Power analysis

In the sub-section power analysis is presented. Power entering in buffer module for bit 'b' is

$$P_s = bP_{in} \qquad b \in [0,1] \tag{9}$$

The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero. Power at the output of the switch is

$$P_{out}^{D1} = P_{in}A_T \tag{10}$$

4.1.2. Noise analysis

The generated noise components at the receiver are shot noise and thermal noise variances are denoted by σ_s^2 and σ_{th}^2 respectively [9, 10]. For the bit b the different noise components at the receiver are

$$\sigma_s^2 = 2qRPB_e \quad \text{and} \quad \sigma_{th}^2 = \frac{4K_BTB_e}{R_L} \tag{11}$$

The total noise variance for bit b is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{th}^2 \tag{12}$$

$$BER = Q\left(\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right) \tag{13}$$

$$Q(z) = \frac{1}{\sqrt{2\pi}}\int_{z}^{\infty} e^{-\frac{z^2}{2}}\, dz$$

where $I(1)=RP(1)$ and $I(0) =RP(0)$ are photocurrent sampled by the receiver during bit '1' and bit '0' respectively, and R is responsivity of the receiver.

4.2. Analysis of switch architecture D2

Case1: The loss analysis if the packet passes through the buffer

The loss of input, which contains the TWC, can be written as

$$A_{in} = L_{Twc} \tag{14}$$

The loss of the buffer which consist of the loss due to the scheduling AWG, loss due to the fiber delay lines and the insertion loss of SOA

$$A_b = L_{AWG}^{2N\times 2N}\, L_{FDL} L_{SOA} \tag{15}$$

Similarly the loss of the output section is

$$A_{out} = L_{AWG}^{2N\times 2N}\, L_{TWC} L_{AWG}^{N\times N} \tag{16}$$

The total loss of the switch is

$$A_T = A_{in} A_b A_{out} \tag{17}$$

The analysis of case '2' will remain same as in architecture D1.

4.2.1. Power analysis

Again, power entering in buffer module for bit b is

$$P_s = bP_{in} \qquad b \in [0,1] \tag{18}$$

The extinction ratio ($\varepsilon = P_0/P_1$) is assumed to be zero. Power at the output of the switch is

$$P_{out}^{D2} = P_{in} + \eta_{sp}(G-1)h\nu B_o A_{out} \tag{19}$$

The term $\eta_{sp}(G-1)h\nu B_o A_{out}$ represents the ASE noise of the SOA amplifier.

4.2.2. Noise analysis

Due to square law detection by the photo detector in the receiver, various noise components are generated. These noise components are shot noise, ASE-ASE beat noise, sig-ASE beat noise, shot-ASE beat noise and thermal noise variances

are denoted byσ_s^2, σ_{sp-sp}^2, σ_{sig-sp}^2 , σ_{s-sp}^2 and σ_{th}^2 respectively [10]. For the bit 'b' the different noise components at the receiver are

$$\sigma_s^2 = 2qRPB_e,$$

$$\sigma_{sp-sp}^2 = 2R^2P_{sp}(2B_o - B_e)\frac{B_e}{B_o^2}$$

$$\sigma_{sig-sp}^2 = 4R^2P\frac{P_{sp}B_e}{B_o} \quad , \sigma_{s-sp}^2 = 2qRP_{sp}B_e$$

$$\sigma_{th}^2 = \frac{4K_BTB_e}{R_L} \tag{20}$$

The expression for 'P' and 'P_{sp}' will be given by

$$P = bP_{in} \tag{21}$$

$$P_{sp} = P_{in} + \eta_{sp}(G-1)h\nu B_o A_{out} \tag{22}$$

The total noise variance for bit 'b' is

$$\sigma^2(b) = \sigma_s^2 + \sigma_{sp-sp}^2 + \sigma_{sp-sp}^2 + \sigma_{s-sp}^2 + \sigma_{th}^2 \tag{23}$$

The BER can be obtained from Eq. 13.

4.3. Calculation

4.3.1. Fiber loop length

Considering that the packet duration is equal to the slot length. Here the duration of the slot, which is equivalent to the length of fiber, can be calculated as

$$L = \frac{cb}{\eta B_r} \tag{24}$$

Here c =3×10^8 represents the speed of the light, 'b' represents the total number of bits stored in the fiber delay lines, 'η' is the refractive index and '*Br*' is the bit rate. The fiber length '*L*' is for loop '1' and '*2L*' for loop '2' and so on. Thus the maximum length of the fiber is 'mL'.

Now the total length of the fiber in architecture *D*1 and *D*2 is

$$L_T = \frac{m(m+1)}{2}L \tag{25}$$

The typical values of the parameters used in the calculation are shown in Table 1 and 2.The size of the packets is taken to be of 1.646 micro-seconds; the minimum loop length is $1.646\times10^{-6}\times3\times10^8$, i.e., 493.8 m. For a 32×32 input AWG, the maximum possible buffer modules are '16'. Hence, the maximum possible length traversed by the packet would be 493.8 × 16 = 7900 m, approx. 8 km. Therefore, the maximum suffered loss in the buffer would be 8 km × 0.2 dB/km=1.6 dB.

Loss of the architecture D1:

Inserting the values of the various loss parameters we get,

$$A_B^T = A_{in}(dB) + A_b(dB) + A_{out}(dB) = 14.6\ dB$$

$$A_T^S = A_{in}(dB) + A_{sch} + A_{out}(dB) = 10.0\ dB$$

Loss of the architecture D2:

Inserting the values of the various loss parameters we get,

$$A_B^T = A_{in}(dB) + A_b(dB) + A_{out}(dB) = 15.6\ dB$$

$$A_T^S = A_{in}(dB) + A_{sch} + A_{out}(dB) = 10.0\ dB$$

where '*S*' represents straight path loss and '*B*' is the loss through the buffer.

Table 1. AWG specifications.

Specification	Value
Number of Channels	40
Channel Spacing	100 GHz
Operating wavelengths	ITU grid
Insertion loss	3.0 dB
Adjacent channel crosstalk	26 dB

Table 2. List of parameters and their value [6].

Parameters	Value
Size of the switch	4,16
Population inversion factor	1.2
Gain of the amplifier	20dB
Speed of light	$3\times10^8 m/s$
Refractive index of fiber	1.55
Effective area of fiber	$8\times10^{-11} m^2$
Responsivity	1.28 A/W
Electronic charge	$1.6\times10^{-19} C$
Electrical bandwidth	20GHz
Optical bandwidth	40GHz
TWC insertion loss	2.0 dB
Loss of Scheduling and Switching	3.0 dB
AWG (32 channels)	0.2 dB/km
Loss of the fiber loop	1 dB
Loss of SOA	

In Fig. 5, BER analysis of architecture D1 and D2 is presented at various power levels when packets are directed towards the output straight through or via buffer. It is clear from the figure that as the power increases, the BER decreases. The minimum power required for the correct reception (BER < 10^{-9}) of a bit at the output of the switch D1, is 5 micro watts. This is much less in comparison to other optical packet switches where the level power lie in mW orders [9].

In case of direct transfer of the packets towards the output the BER performance is much better and the acceptable BER can be achieved at 2 micro-watts power levels. Moreover the BER at the power level of 5 micro-watts is 3×10^{-22}. Thus the difference in BER for direct transfer and via buffer transfer of packets is huge; therefore in such a case optimal receiver design is not possible. In case of the architecture D2, loss of the switch is compensated with a variable gain

amplifier, such that the power received at the output is equal to the input power. However, the directly transferred packet will follow the same analysis as in the case of architecture D1. It is clear from the figure that the acceptable BER is available at the power level of 2 micro watts with slight difference in the bit error rate, and the obtained BER is well below the acceptable range. In past the concept of slow light buffers was proposed due to the large losses in optical switches [11], moreover, it is also suggested that the power requirement is much higher in optical packet switching and is of the order of mW [9]. In the presented architecture the loss is very less and hence as such no needs for the slow light buffers, and power requirement is very less and in the order of micro-watts as in CMOS circuits [12].

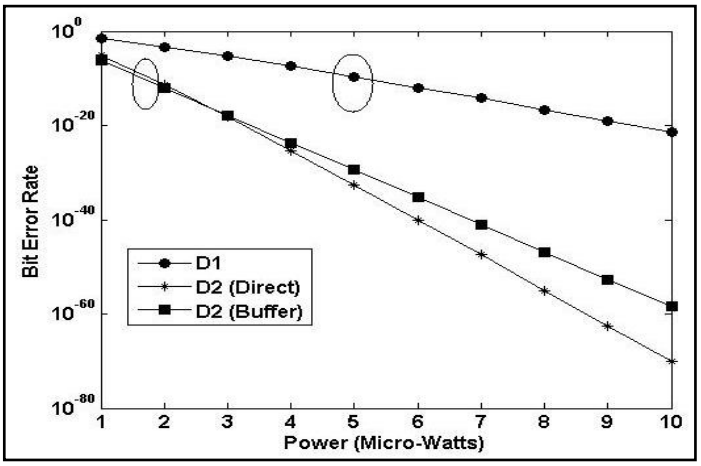

Fig. 5. BER vs. signal power for *N*=16.

5. Queuing Analysis

In the presented architecture, for each output separate queue is formed in wavelength domain. The packet arriving at switch input, create a queue, and packet remains in the queue until they get served (Fig. 6).

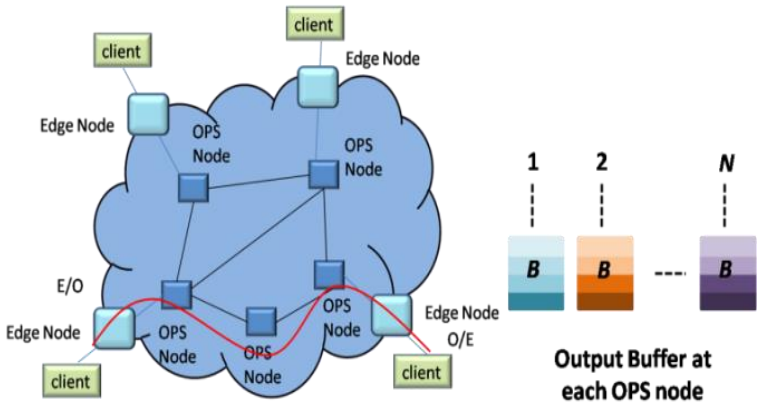

Fig. 6. Schematic of OPS network with output buffer at each node.

In the output queue analysis [8], we concentrate on a specific queue (Fig. 7). The analytical results for this queue will also be valid for all other queues as all of them are equivalent to each other. This model assumes an identical Bernoulli process for traffic generation. That is, in any time slot, the probability of the arrival of the packet on a particular input is 'p' and each packet has equal probability 1/N of being addressed to any one of the outputs.

Defining a random variable X as the number of packets coming for a particular tagged output in a given slot, the probability that exactly 'q' packets will arrive in a slot is

$$P_q = P_r[X = q] = N_{C_q}\left(\frac{p}{N}\right)^q \left(1 - \frac{p}{N}\right)^{N-q} \qquad 0 \le q \le N \tag{26}$$

In queue the minimum number of packets is zero and the maximum numbers of packets are equal to the maximum buffering capacity of the buffer. Assuming the maximum buffering capacity of 'B' packets we have, let if 'Qi' denote the number of packets in the tagged queue at the end of the i^{th} time slot and 'Ai' 'denotes the number of packets arriving in the i^{th} slot, then

$$Q_i = \min\left\{\max\left(0, Q_{i-1} + A_i - 1\right), B\right\} \tag{27}$$

A packet will not be transmitted to the tagged output queue if $Q_{i-1}=0$ and $A_i=0$ in the slot i. If in any time slot $Q_{i-1}+A_{i-1}>B$ then $Q_{i-1}+A_{i-1}-B$, packets will be lost at the input of the switch.

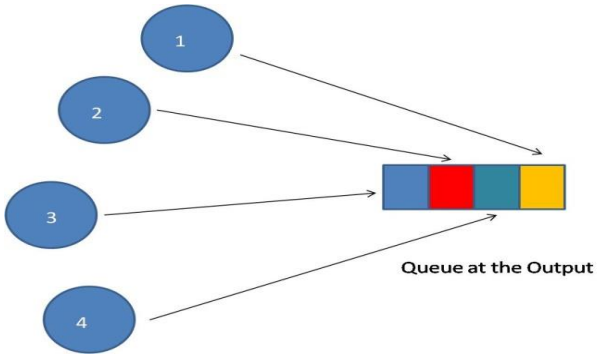

Fig. 7. Queuing structure of the output buffer.

5.1. Without load balancing

In Fig. 8, the packet loss probability vs. load of the system is presented while assuming 4×4 nodes, i.e., '4' inputs/outputs and buffering of '4', '8' and '16' packets. It is clear from the figure that as the load increases the packet loss probability increases. It can also be visualized from the figure that as the buffering capacity increases the packet loss probability decreases. At the load of 0.8, with buffering capacity of '16', '8' and '4' packets, the packet loss probability is 3×10^{-5}, 2×10^{-3}, and 1.5×10^{-2} respectively.

Thus, by increasing the buffer space by four fold, i.e., from '4' to '16', the packet loss probability is improved by a factor of 2000. Therefore, it can be

summarized that the buffering capacity has deep impact on the over-all packet loss probability.

In Fig. 9, average delay vs. load on the system is presented while assuming 4×4 nodes, i.e., '4' inputs/outputs and buffering of '4', '8' and '16' packets. It is clear from the figure that as the load increases the average delay also increases. It can also be visualized from the figure that as the buffering capacity increases the average delay also increases. The average delay remains nearly same till load reaches 0.8 and in fact average delay is independent of buffering capacity. But as we cross 0.8 marks, the average delay shoots up. This is obvious as, at the higher load more number of packets will arrive means more contention, and thus in turn more buffering of packets.

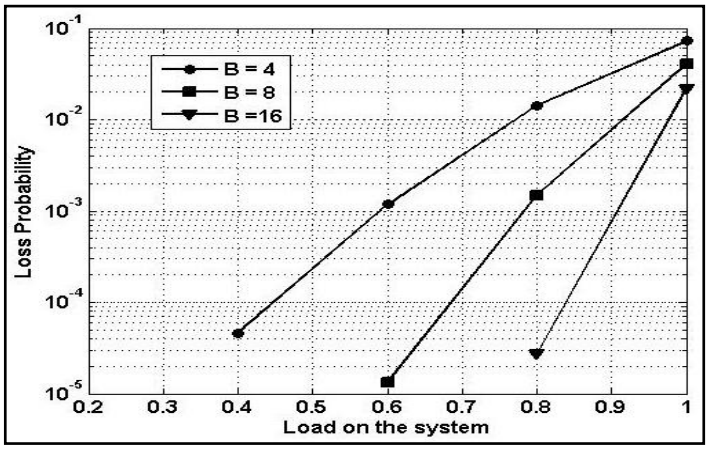

Fig. 8. Packet loss probability vs. load on the system with varying buffering capacity.

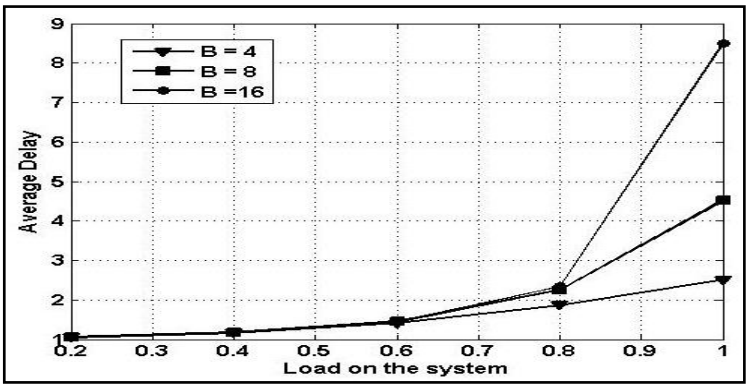

Fig. 9. Average delay vs. load on the system with varying buffering capacity.

5.2. With load balancing

As in past it is suggested that the load balancing scheme improves the packet loss rate [13]. In this scheme we assume that, in case of contention packet may take different routes to reach its destination. Thus the overall load on a particular

switch will be decreased. In Figs. 10 and 11 results under load balancing schemes are presented, while *'g'* denotes the fraction of traffic passes through the switch.

In Fig. 10, the packet loss probability vs. load of the system is presented while assuming 4×4 nodes, i.e., '4' inputs/outputs and buffering of '4' packets. However, the load balancing scheme is applied. In the figure 'g' represents the fraction of traffic routed through some other nodes. For 'g=0.5' the packet loss probability, improves by a factor of 100 in comparison to 'g=0.9'. Similarly, at the load of 0.6, the packet loss improves by 10 when 'g' changes from 0.5 to 0.7 and similarly from 0.7 to 0.9.

In Fig. 11, average delay vs. load on the system is presented while assuming 4×4 nodes, i.e., '4' inputs/outputs and buffering of '4' packets. However, the load balancing scheme is applied. Comparing with Fig. 11, the average delay has reduced considerably and this difference is more prominent at the higher loads. For 'g=0.5' the average delay at the load one is reduced by nearly '7' slots. Similarly for 'g=0. 9', the average delay is required by 6 slots.

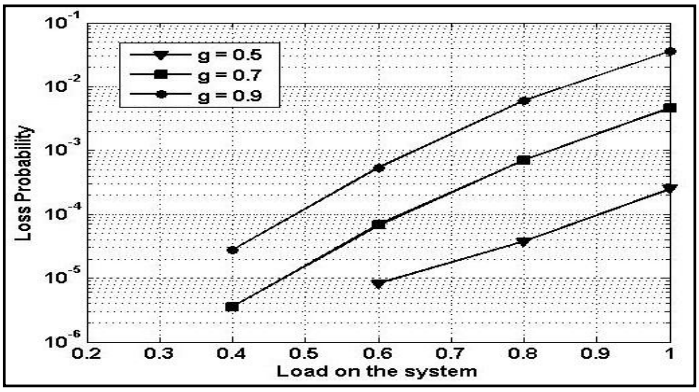

Fig. 10. The packet loss probability vs. load on the system with fix buffering capacity of 4, with load balancing.

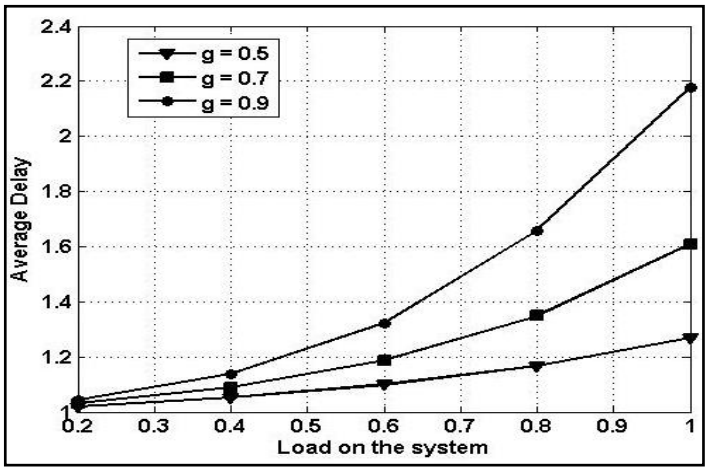

Fig. 11. Average delay vs. load on the system with fix buffering capacity of 4, with load balancing.

5.3. Cross layer optimization

In this section it is shown that how physical and network layers parameters are interrelated. For a particular application, let the desired packet loss be equal to 10^{-4}, at a given load of 0.8 and for a switch size N = 16. First of all consider Fig. 12, where packet loss for N=16 for different buffer space is shown. Thus, as per the requirement, minimum buffer space that needs to be considered is 16. For N=16 and B=16, BER for different power level is shown in Fig. 5. Considering Fig. 5, for acceptable BER<10^{-9} the desired power would be 2μW, with size of packet as 1.646 micro-seconds.

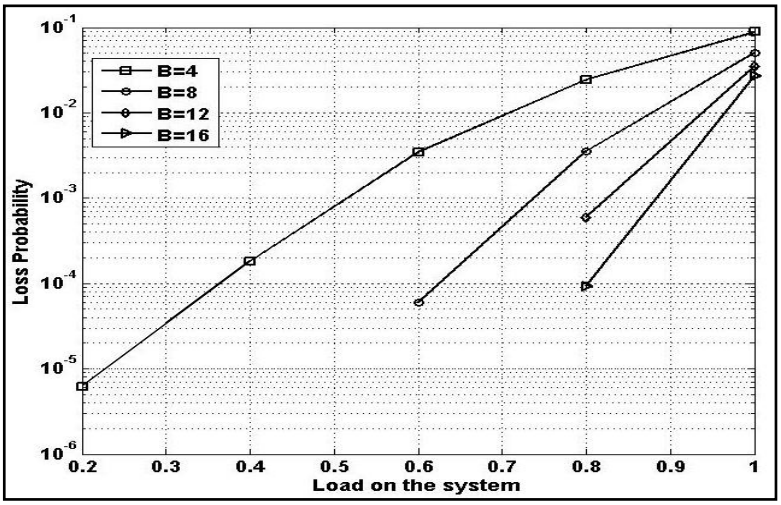

Fig. 12. Packet loss probability vs. load for *N*=16 and buffer varying from 4 to 16.

6. Conclusions

Optical packet switching has shown promises for the next generation data transfer technology due to its advantages like very high speed, low noise perturbation and infinite bandwidth of the optical fiber etc. The main problem of contention is resolved using temporary buffering of the packets at the intermediate nodes. In the past, much research has been done, on the design of optical node, and most of the architectures are very complex. In this paper an AWG based optical packet switch is discussed, the major findings of the research are:

- In this switch the power requirement for the correct operation of the switch is much below than the earlier architectures.
- The simulation analysis also shows that the switch architecture can provide very low packet loss probability with reasonably low delays.
- The load balancing schemes further improves the results in terms of packet loss probability.

In the future work, a detailed analysis of the switch will be done by considering the effect of crosstalk and fiber non-linearity on the optical switch. Further study will also be carried out when such switches are placed in the

network. As the required power is of the order of micro-watts, therefore fiber non-linearity will not affect the performance of a single switch, however, when such switches are placed in the network, this analysis is very important for the cascadability of the switches.

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