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CONTROL TECHNIQUES FOR VARIOUS BIPOLAR PWM STRATEGIES OF THREE PHASE FIVE LEVEL CASCADED INVERTER

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Abstract

This paper presents different types of bipolar Pulse Width Modulation (PWM) strategies for the chosen Cascaded MultiLevel Inverter (CMLI). The main purpose of MLI is to use power semiconductor devices of lower voltage ratings to realize high voltage levels at inverter output. Due to their ability to obtain refined output voltage waveforms, reduced Total Harmonic Distortion (THD) and reduced EMI problems by reducing the switching *dv/dt*. In this paper, a three phase CMLI is controlled with Sinusoidal PWM strategy with Phase Disposition PWM (PDPWM), Phase Opposition and Disposition PWM (PODPWM), Alternative Phase Opposition and Disposition PWM (APODPWM), Phase Shift PWM (PSPWM) and hybrid modulation strategy and the variation of THD in their outputs are observed by varying the modulation index. Simulations are performed using MATLAB-SIMULINK. It is observed that APODPWM and PSPWM provide output with relatively low distortion. It is also seen that PS, APOD and hybrid PWM are found to perform better since they provide relatively higher fundamental RMS output voltage. From hardware results it is seen that POD PWM provides output with relatively low distortion. It is also observed that PSPWM is found to perform better since it provide relatively higher fundamental RMS output voltage.

Keywords: Total Harmonic Distortion, Cascaded multi level inverter, Phase disposition, Phase opposition and disposition, Alternative phase opposition and disposition, Field Programmable Gate Array.

1. Introduction

Power conditioning systems are often designed to supply an AC load from DC source. An inverter should provide constant and ripple free AC voltage to ensure

Nomenclatures

A_c	Carrier amplitude, volts
A_m	Reference amplitude, volts
B	Output voltage terminal
E_1& E_2	Voltage Sources, volts
f_c	Carrier frequency, Hz
f_m	Modulating (or)Reference frequency, Hz
f_s	Switching Frequency, Hz
HF_n	n^{th} harmonic factor
I_s	RMS value of input current, amps
$I_s(peak)$	Peak input current, amps
L	Inductor, Hendry
m	Number of levels
m_a	Amplitude Modulation index
m_f	Frequency Modulation index
n	Number of output phase voltage levels
N	Neutral
R	Output voltage terminal
R_L	Load Resistor, ohms
S	Number of DC Sources
$S_1 - S_4$	Switches
V_{avg}	Average voltage, volts
V_{dc}	Input Voltage, volts
V_{DC}	DC voltage, volts
V_{rms}	RMS voltage, volts
V_{RMS}	RMS voltage, volts
V_{on}	n^{th} harmonic voltage, volts
V_{o1}	Fundamental voltage, volts
Y	Output Voltage terminal

Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
APOD	Alternate Phase Opposition and Disposition
CF	Crest Factor, %
CMLI	Cascaded Multi Level Inverter
dSPACE	Digital Signal Processing and Control Engineering
DAC	Digital to Analog converter
DC	Direct Current
DCMs	Digital Clock Manager
DF	Distortion Factor, %
DTC	Direct Torque Control
EMI	Electro Magnetic Interference
FF	Form Factor, %
FFT	Fast Fourier Transform

Abbreviation

FPGA	Field Programmable Gate Array
HF	Harmonic Factor, %
IC	Integrated Circuit
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LOH	Lower Order Harmonics, %
MATLAB	Matrix Laboratory
MLI	Multi Level Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PD	Phase Disposition
POD	Phase Opposition and Disposition
PROM	Programmable Read Only Memory
PS	Phase Shift
PWM	Pulse Width Modulation
RAM	Random Access Memory
RMS	Root Mean Square
SPWM	Sinusoidal Pulse Width Modulation
STATCOM	Static Synchronous Series Compensator
THD	Total Harmonic Distortion, %
UART	Universal Asynchronous receiver/transmitter
VAR	Volt Ampere Reactance
VF	Variable Frequency
VHDL	Hardware Descriptive Language
VLSI	Very Large Scale Integration

the safety of the equipments .The design of such systems must achieve an output voltage behavior as close as possible to the ideal AC voltage in the sense of fast transient response to load variation and low THD. With the expansion of power electronics towards the medium voltage and high power applications in the past fewyears, multilevel power conversion is an emerging area.

A cascade multilevel inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years. This paper focuses on multicarrier based sinusoidal PWM strategies which have been used in chosen three phase cascaded MLI. A pulse width modulation (PWM) scheme that used sinusoidal modulating signals with a multiple triangular carrier is discussed. The PWM strategies chosen are PDPWM, PODPWM, APODPWM, PSPWM and PD+PSPWM.

The chosen PWM strategies are simulated and implement through FPGA hardware. The new strategies chosen are PD+PSPWM (hybrid) strategy. Donald Grahame Holmes and McGrath [1] proposed opportunities for harmonic cancellation with carrier-based PWM for two level and multilevel cascaded inverters. Jose et al. [2] carried out survey on topologies, controls and applications. Loh et al. introduced in [3] synchronization of distributed PWM cascaded multilevel inverter with minimal harmonic distortion and common mode voltage. Mariethoz and Rufer [4] analysed resolution and efficiency improvements for three phase cascaded multilevel inverters. Xianglian et al. [5]

proposed phase shift SPWM technique for cascaded multilevel inverter. Azli et al. [6] analysed the performance of a three phase cascaded H-bridge multilevel inverter. Roozbeh Naderi and Rahmati [7] proposed phase shifted carrier PWM technique for general cascaded inverters. Gierri Waltrich and Ivo Barbi [8] introduced three phase cascaded multilevel inverter using power cells. Malinowski et al. [9] presented a survey on cascaded multilevel inverter. Tengfei Wang and Zhu [10] analysed and compared various multicarrier PWM schemes applied in H-bridge cascaded MLI. Georgious et al. [11] proposed harmonic elimination control of a five level DC-AC cascaded H-bridge hybrid inverter. Farid Khoucha et al. [12] proposed comparison of symmetrical and asymmetrical three phase H-bridge multilevel inverter for direct torque control induction motor drives. Cougo et al. [13] developed PD modulation scheme for three-phase parallel multilevel inverters.This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI employing SPWM switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonic analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

2. Multi Level Inverter

The CMLI is simply a number of conventional two-level bridges whose AC terminals are simply connected in series to synthesize the output waveforms. Figure 1 shows the power circuit for a three phase five-level inverter with six cascaded cells. The CMLI needs several independent DC sources which may be obtained from batteries, fuel cells or solar cells. Through different combinations of the four switches of each cell, each converter can generate three different voltage outputs, $+Vdc$, 0,$-Vdc$. The AC output is the sum of the individual converter outputs. The number of output phase voltage levels is defined by $n = 2S+1$, where S is the number of DC sources. For instance the output range swings from $-2V_{dc}$ to $+2V_{dc}$ with five levels.

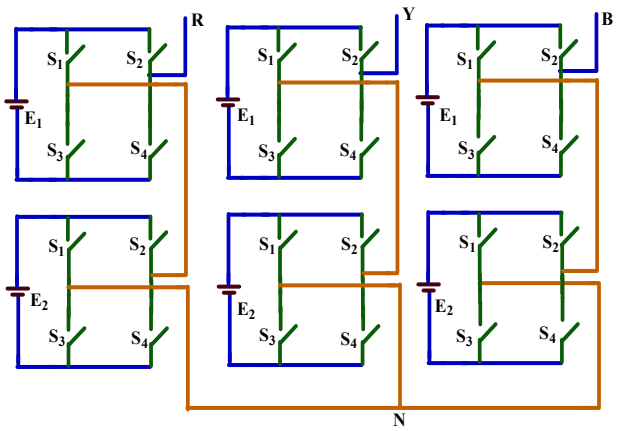

Fig. 1. SIMULINK Model for Three Phase Five Level Cascaded Multilevel Inverter.

The use of CMLI offers several advantages over more traditional inverters including better output waveforms lower THD, lower switching frequency, increased efficiency and reliability.

The gate signals for chosen five level cascaded inverter are simulated using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index m_a and for various PWM strategies. Figure 2 shows a sample SIMULINK model developed for PDPWM method. The simulation and hardware results presented in this work in the form of the outputs of the chosen multilevel inverter are compared and evaluated.

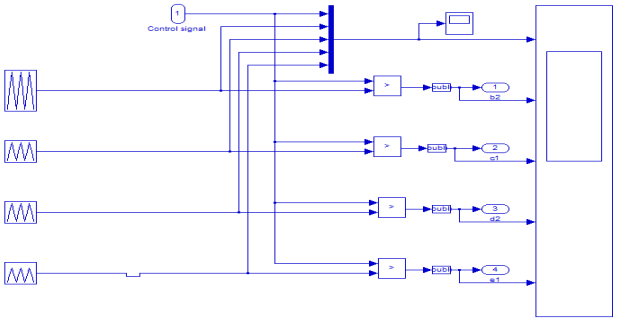

Fig. 2. Sample PWM Generation Logic Model Developed using SIMULINK for PDPWM Technique.

3. Modulation Strategies

Multicarrier PWM techniques entail the natural sampling of a single modulating or reference waveform typically being sinusoidal, through several carrier signals typically being triangular waveforms. This paper focuses on multicarrier based sinusoidal PWM strategies which have been used in chosen three phase cascaded MLI. The following strategies are employed in this study.

The following formula is applicable to PD, POD, APOD and VF. The frequency modulation index

$$m_f = \frac{f_c}{f_m} \tag{1}$$

The Amplitude modulation index

$$m_a = \frac{2A_m}{(m\text{-}1)A_c} \tag{2}$$

where

f_c – Frequency of the carrier signal
f_m – Frequency of the reference signal
A_m –Amplitude of the reference signal
A_c – Amplitude of the carrier signal
m – Number of levels.

3.1. Phase disposition PWM strategy

The principle of the PDPWM strategy is to use several triangular carriers with only one modulation wave. For an *m* level inverter, *m-1* carriers of same frequency f_c and same peak-to-peak amplitude A_c are disposed so that the bands they occupy are contiguous as shown in Fig.3. The reference or modulation wave has amplitude A_m and frequency f_m and it is centered in the middle of the carrier set. If the reference is greater than a carrier signal, then the active devices corresponding to that carrier are switched on; otherwise the devices switch off.

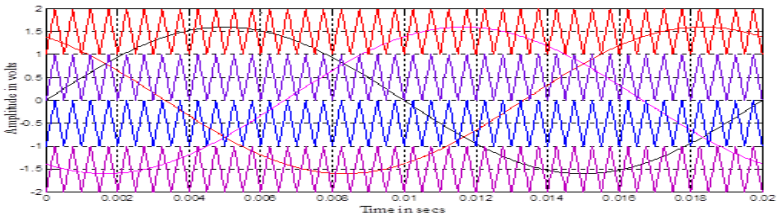

Fig. 3. Multicarrier Arrangement for PDPWM Technique.

3.2. Phase opposition disposition PWM strategy

This method is having the carriers above the zero line of reference voltage out of phase with those of below this line by 180 degrees as shown in Fig. 4.

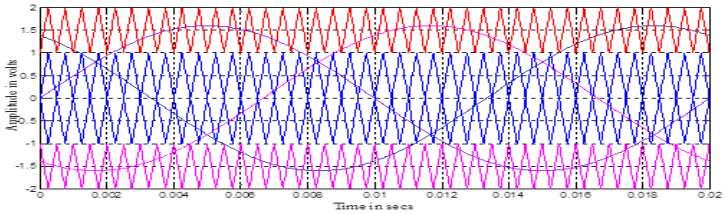

Fig. 4. Multicarrier Arrangement for PODPWM Technique.

3.3. Alternative phase opposition and disposition PWM strategy

Each carrier of this method is phase shifted by 180 degrees from its adjacent one as shown in Fig. 5. It should be noted that POD and APOD methods are exactly the same for a 3-level inverter. This method gives almost the same result as the POD method. The major difference is the larger amount of third order harmonics which is not important because of their cancellation in line voltages when comparing to the POD method.

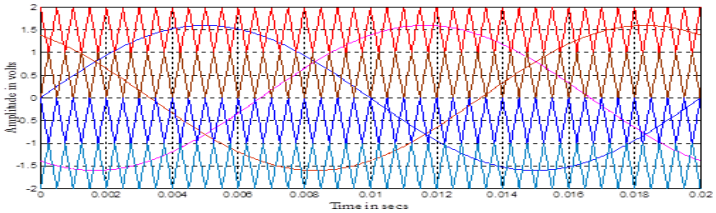

Fig. 5. Multicarrier Arrangement for APODPWM Technique.

3.4. Phase shift PWM strategy

To generate a output phase voltage with m levels, this strategy uses (*m–1*) carriers with the same amplitude but with 360/(*m–1*) degrees phase-shift among themselves. For a *m*-level converter, the most significant harmonics will be located in lateral bands around $(m-1)f_c$ where f_c is the carrier frequency. For even values of the modulation frequency index (m_f), the waveforms synthesized present quarter wave symmetry resulting only even harmonics. Therefore, for a five-level inverter, this strategy uses four carriers with 90º phase-shift among themselves, as can be seen in Fig. 6.

$$m_a = \frac{A_m}{(A_c / 2)} \tag{3}$$

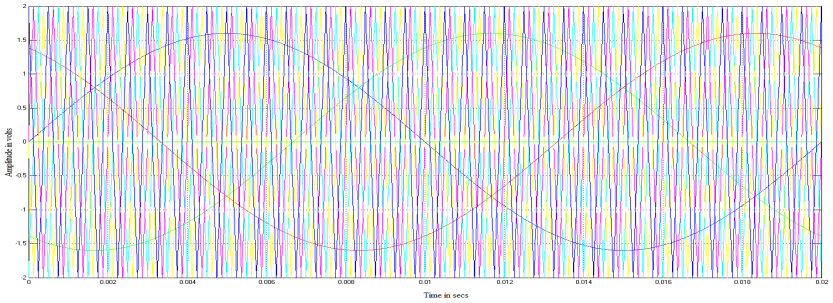

Fig. 6. Multicarrier Arrangement for PSPWM Technique.

3.5. Hybrid PWM strategy

The different modulation strategies have different characters and are applicable to different multilevel topologies. One of the most important methods to optimize control of the inverter is to select and design suitable PWM modulation strategies according to the characters of the multilevel topologies.

Based on the above analysis, the general idea of modulation strategies based on multi-carrier SPWM can be drawn for hybrid topologies. Firstly, the modulation strategies based on the vertical distribution of carriers do not increase the equivalent carrier frequency, while the modulation strategy based on horizontal phase-shifted carrier can effectively increase the equivalent carrier frequency and decrease harmonic content of output voltage; secondly, the cascaded topologies have modular extendibility and high output voltage characteristics. So, for research on hybrid topologies, the overall structure shall be cascaded, the modulation strategy based on horizontal phase-shifted carriers shall be adopted for the overall modulation, and the suitable modulation strategy shall be adopted for specified topology to be used for different modules. For lower module, fundamental wave frequency modulation shall be adopted to reduce the switching loss. For upper module, multi-carrier modulation shall be adopted to improve the frequency spectrum performance of output waveform. The PD and PS techniques can be adopted for the two basic modules. Meanwhile, the PS technique can be adopted to increase the equivalent carrier frequency between

modules. In this way, for the topology given Fig. 1, the PD+PS modulation strategy is adopted, as shown in Fig. 7.

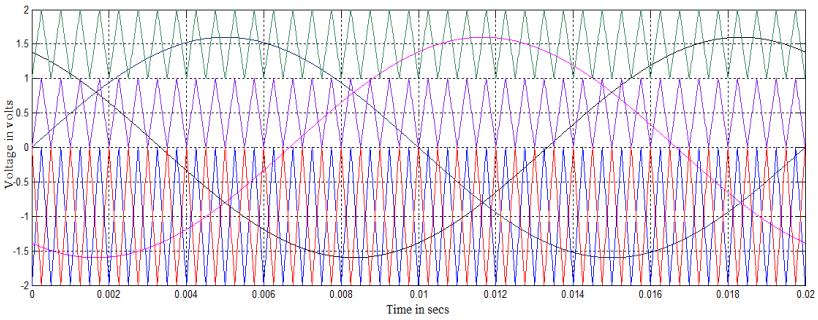

Fig. 7. Multicarrier Arrangement for Hybrid PWM Technique.

In this paper, m_f = 40 and m_a is varied from 0.6 to 1. m_f is chosen as 40 as a trade off in view of the following reasons:

- to reduce switching losses (which may be high at large m_f)
- to reduce the size of the filter needed for the closed loop control, the filter size being moderate at moderate frequencies
- to effectively utilise the available dSPACE system for hardware implementation.

4. Simulation Results

The cascaded five level inverter is modelled in SIMULINK using power system block set. Switching signals for CMLI are developed using bipolar PWM techniques discussed previously. Simulation is performed for different values of m_a ranging from 0.6 – 1. The corresponding %THD values are measured using FFT block and they are shown in Table 1. Table 2 displays the V_{rms} of fundamental of inverter output for same modulation indices. Table 3 shows crest factor, Table 4 provides form factor and Table 5 displays distortion factor for various values of modulation indices. Figures 8-17 show the simulated output voltage of CMLI and corresponding FFT plots with above strategies but for only one sample value of m_a = 0.8. Figure 8 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig. 9. From Fig. 9 it is observed that the PDPWM strategy produces significant 30^{th}, 32^{nd}, 36^{th} and 38^{th}harmonic energy. Figure 10 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig. 11. From Fig. 11 PODPWM strategy produces significant 33^{rd}, 35^{th} and 39^{th} harmonic energy. Figure 12 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig. 13. From Fig. 13 it is seen that the APODPWM strategy produces significant 35^{th} and 37^{th} harmonic energy. Figure 14 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig. 15. From Fig. 15 it is noticed that the PSPWM strategy produces no significant harmonic energy. Figure 16 shows the five level output voltage generated by hybrid strategy and its FFT plot is

shown in Fig. 17. From Fig. 17 it is noticed that the hybrid strategy produces significant 34^{th},39^{th} and 40^{th} harmonic energy.

The following parameter values are used for simulation: V_{DC} =220V, R_L= 100 ohms, L= 0.5 mH and f_s = 2 kHz.

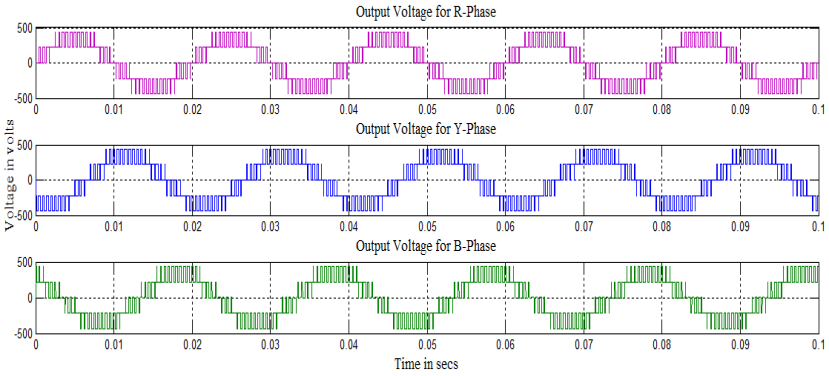

Fig. 8. Output Voltage Generated by PDPWM Technique.

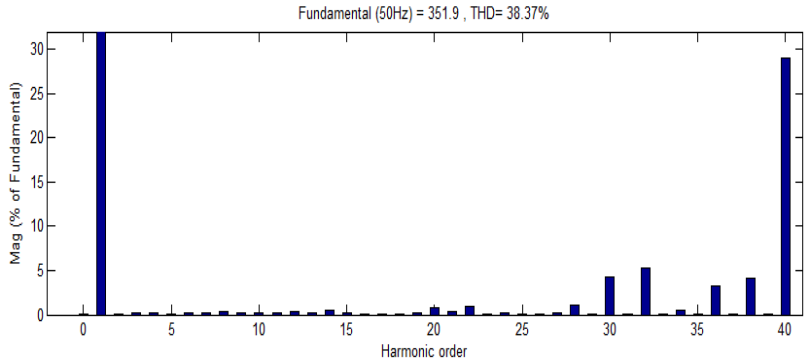

Fig. 9. FFT Plot for Output Voltage of PDPWM Technique.

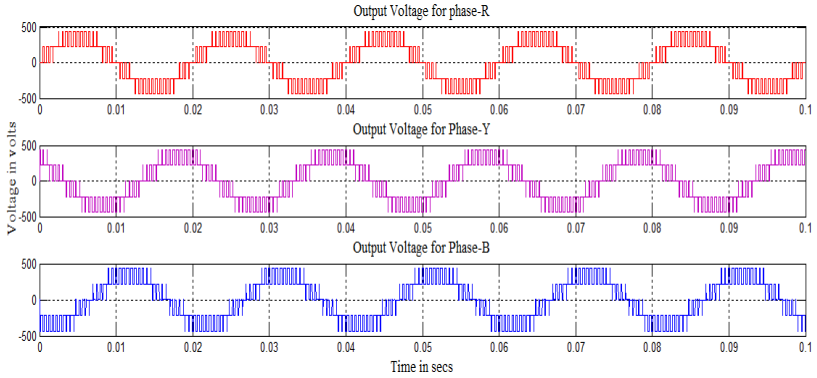

Fig. 10. Output Voltage Generated by PODPWM Technique.

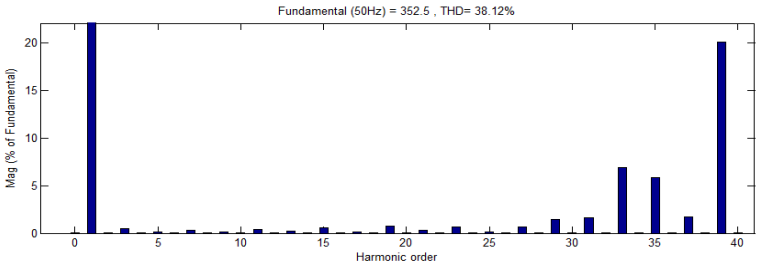

Fig. 11. FFT Plot for Output Voltage of PODPWM Technique.

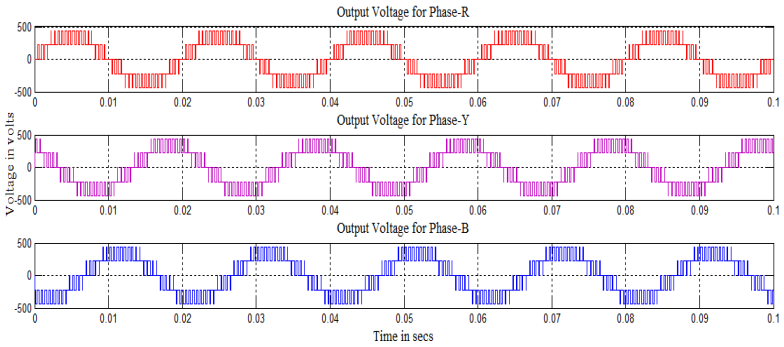

Fig. 12. Output Voltage Generated by APODPWM Technique.

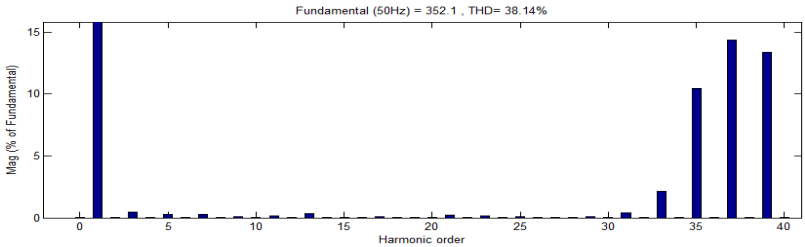

Fig. 13. FFT Plot for Output Voltage of APODPWM Technique.

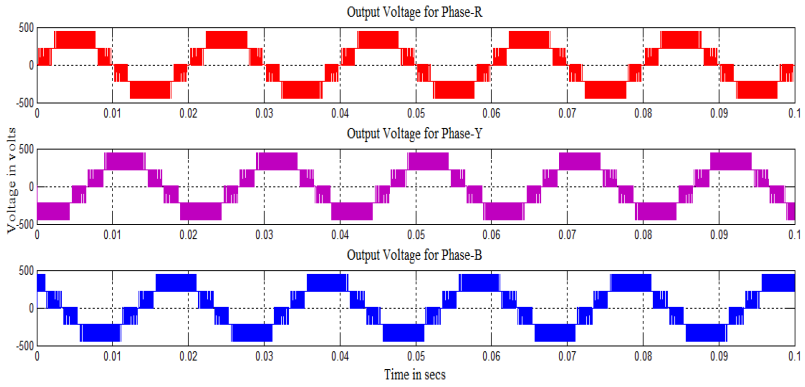

Fig. 14. Output Voltage Generated by PSPWM Technique.

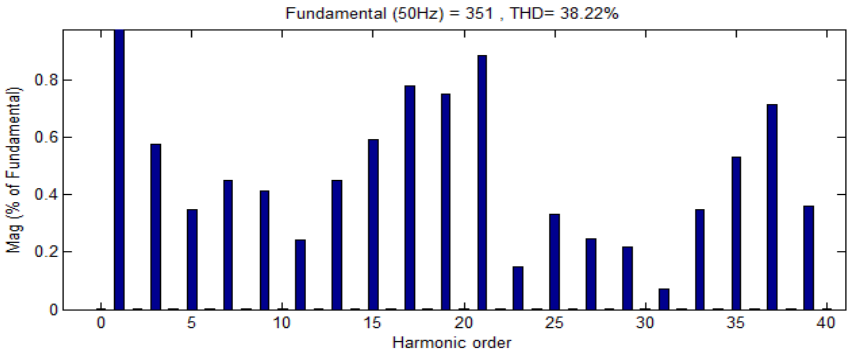

Fig. 15. FFT Plot for Output Voltage of PSPWM Technique.

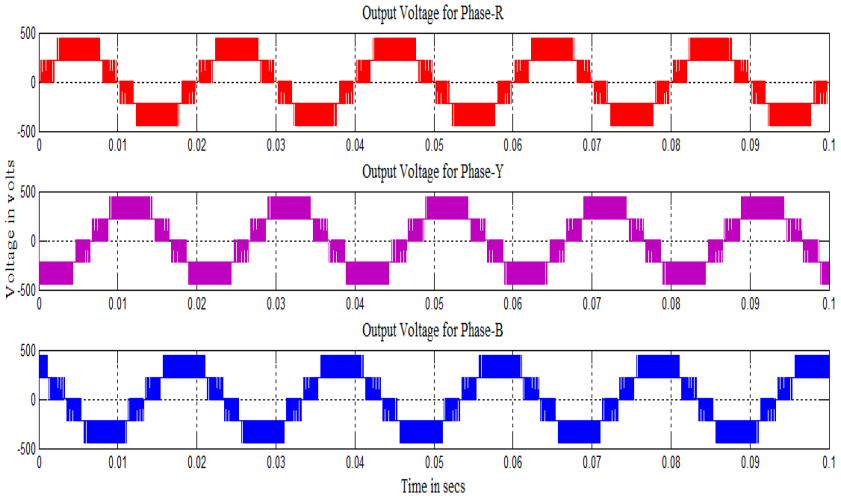

Fig. 16. Output Voltage Generated by Hybrid (PS+PD)PWM Technique.

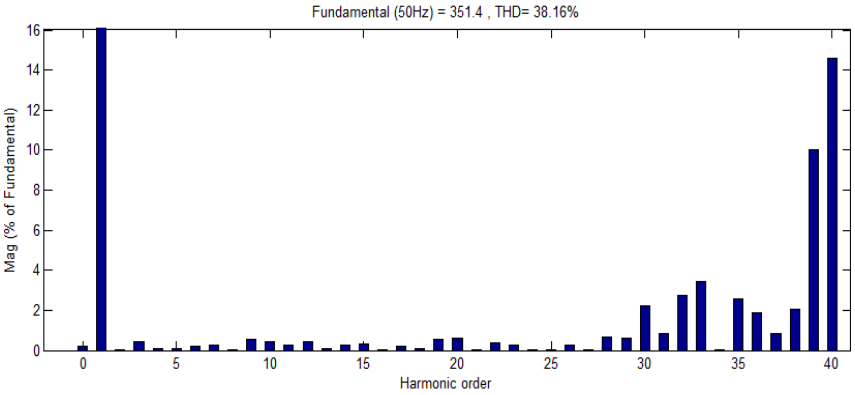

Fig. 17. FFT Plot for Output Voltage of Hybrid (PS+PD)PWM Technique.

Table 1. %THD for Different Modulation Indices (by Simulation).

m_a	PD	POD	APOD	PS	PD+PS
1	27.04	26.94	26.52	27.18	26.84
0.9	33.62	33.50	33.21	32.76	33.40
0.8	38.37	38.12	38.14	38.22	38.16
0.7	42.07	41.88	41.97	41.37	42
0.6	44.47	44.52	44.56	44.35	44.51

Table 2. V_{RMS} (Fundamental) for Different Modulation Indices (by Simulation).

m_a	PD	POD	APOD	PS	PD+PS
1	310.7	310.7	311.1	311	311
0.9	280	279.9	280.3	280.2	279.8
0.8	248.8	249.2	249	248.2	248.5
0.7	217.3	217	217.2	218.1	216.8
0.6	186.1	185.7	186	184.6	186.2

Table 3. %Crest Factor for Different Modulation Indices (by Simulation).

m_a	PD	POD	APOD	PS	PD+PS
1	1.414	1.4139	1.4144	1.4141	1.4141
0.9	1.4143	1.4141	1.4141	1.4141	1.4141
0.8	1.4143	1.4142	1.4142	1.4141	1.4141
0.7	1.4141	1.4139	1.4139	1.4145	1.4139
0.6	1.4137	1.4147	1.4141	1.4136	1.4138

Table 4. %Form Factor for Different Modulation Indices (by Simulation).

m_a	PD	POD	APOD	PS	PD+PS
1	INF	INF	INF	INF	INF
0.9	INF	INF	INF	INF	INF
0.8	INF	INF	INF	INF	INF
0.7	INF	INF	INF	INF	INF
0.6	INF	INF	INF	INF	INF

Table 5. Distortion Factor for Different Modulation Indices (by Simulation).

m_a	PD	POD	APOD	PS	PD+PS
1	0.035	0.043	0.020	0.020	0.041
0.9	0.048	0.069	0.034	0.043	0.063
0.8	0.038	0.057	0.057	0.066	0.028
0.7	0.094	0.028	0.022	0.021	0.058
0.6	0.043	0.085	0.085	0.049	0.107

5. Hardware Results

This section presents the results of experimental work carried out on chosen CMLI using a FPGA-3E board which is based on the VPTB-05. Real time implementation of these strategies using VHDL coding requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/SIMULINK. Spartan-3E Low Cost board which includes the

following components and features 100,000-gate Xilinx Spartan-3E, XC3S100 E FPGA in a 144-Thin Quad Flat Pack package (XC3S100E- Q144), 2160 logic cell equivalents, Four 18K-bit block RAMs (72K bits), Four 18x18 pipelined hardware multipliers, Two Digital Clock Managers (DCMs), 32 Mbit Intel Strata Flash, 3 numbers of 20 pin header to interface VLSI based experiment modules, 8 input Dip Switches, 8 output Light Emitting Diodes(LEDs), On Board programmable oscillator (3 to 200 MHz), 16x2 Alphanumeric LCD, RS232 UART, 4 Channel 8 Bit I2C based ADC & single Channel DAC, PS/2 Keyboard/Mouse, Prototyping area for user applications and on Board configuration Flash PROM XCF01S.The gate signal generation blocks using different PWM strategies listed above are designed and developed using VHDL coding and downloaded to FPGA. The results of the experimental study are shown in the form of the PWM outputs of chosen CMLI

Optocoupler circuit provides isolation between the control circuit and the powerconverter circuit. The optocoupler used is 6N137, which is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is in version of the applied input. The PWM signals from the FPGA are not capable of driving the MOSFETs. In order to strengthen the pulses a driver circuit is provided.

Figure 18 shows the entire hardware setup. After suitably scaling down the simulation values, in view of laboratory constraints, the peak-to-peak output voltage obtained experimentally is 40 V.

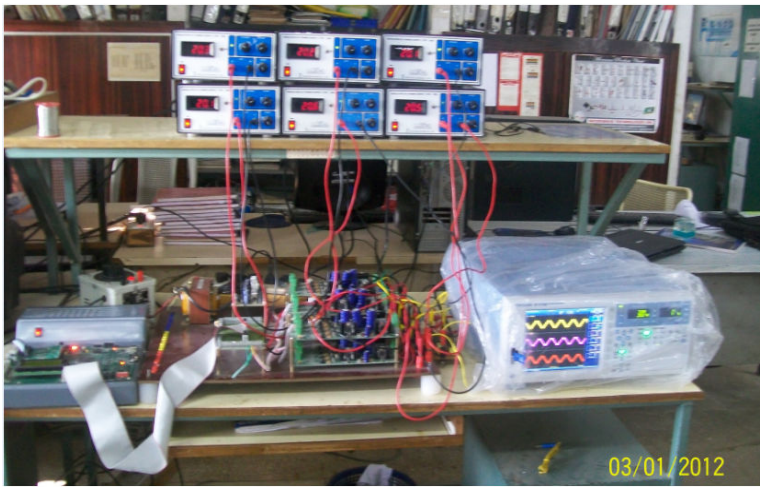

Fig. 18. The Entire Hardware Setup.

Switching signals for CMLI are developed using FPGA processer as shown in Fig. 18. Hardware results are obtained for different values of m_a ranging from 0.6 – 1. The corresponding %THD values are measured using FFT block and they are shown in Table 6. Table 7 displays the V_{rms} of fundamental of inverter output voltage. Tables 8 and 9 provide form factor and distortion factor for

same modulation indices. Figures 19-28 show the hardware output voltage of CMLI and corresponding FFT plots with above strategies but for only one sample value of m_a = 0.8. Figure 19 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig. 20. From Fig. 20 it is observed that the PDPWM strategy produces significant 112th and 120th harmonic energy. Figure 21 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig. 22. From Figure 22 PODPWM strategy produces significant 113rd, 115th and 119th harmonic energy. Figure 23 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig. 24. From Fig. 24 it is seen that the APODPWM strategy produces significant 115th and 117th harmonic energy. Figure 25 shows the five level output voltage generated by PSPWM strategy and its FFT plot is shown in Fig. 26. From Fig. 26, it is noticed that the PSPWM strategy produces significant 119thharmonic energy. Figure 27 shows the five level output voltage generated by hybrid strategy and its FFT plot is shown in Fig. 28. From Fig. 28 it is noticed that the (PS+PD) strategy produces significant 2nd, 3rd, 4th, 112th, 116th, 118th, 119th and 120th harmonic energy.

The following parameter values are used for hardware setup: V_{DC} =20V, R_L= 100 ohms, L=50 mH, and f_s = 6 kHz

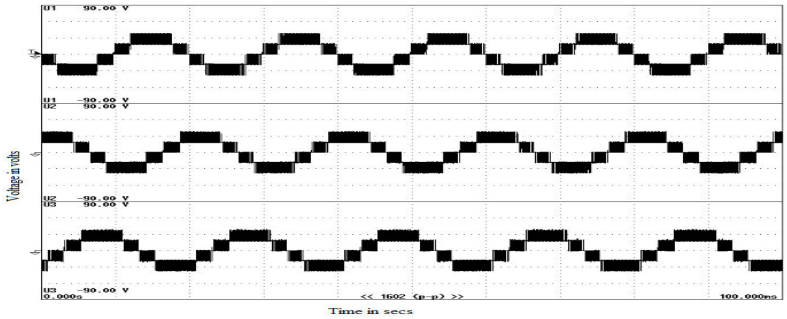

Fig. 19. Output Voltage Generated by PDPWM Technique.

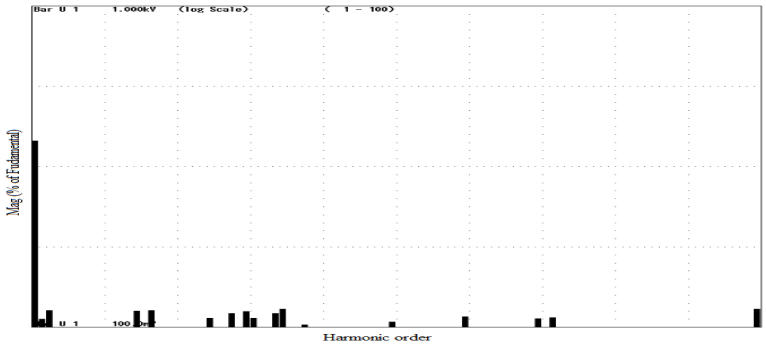

Fig. 20. FFT Plot for Output Voltage of PDPWM Technique.

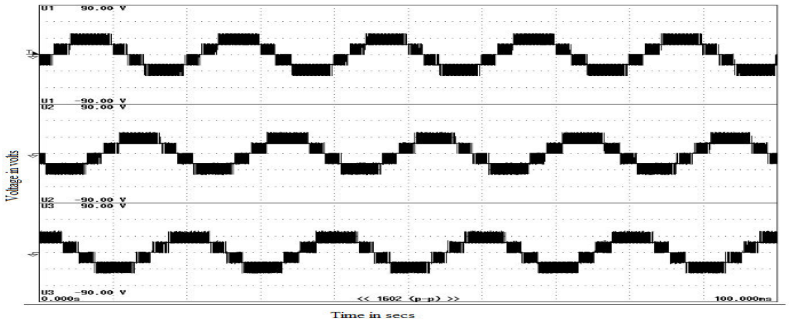

Fig. 21. Output Voltage Generated by PODPWM Technique.

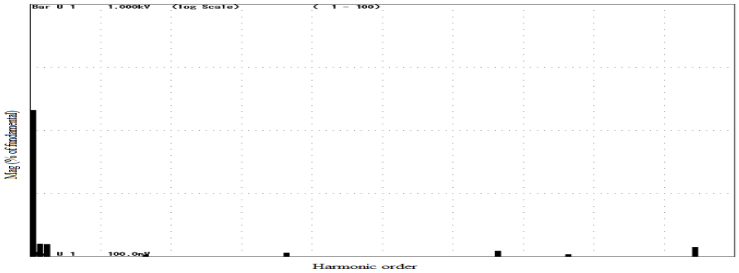

Fig. 22. FFT Plot for Output Voltage of PODPWM Technique.

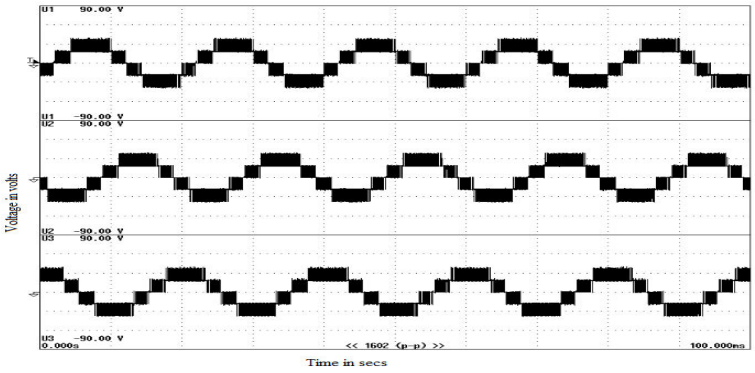

Fig. 23. Output Voltage Generated by APODPWM Technique.

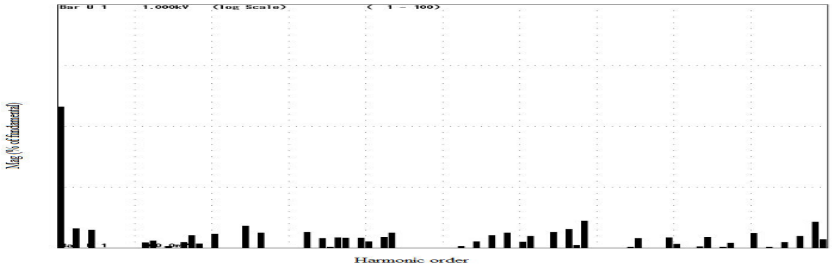

Fig. 24. FFT Plot for Output Voltage of APODPWM Technique.

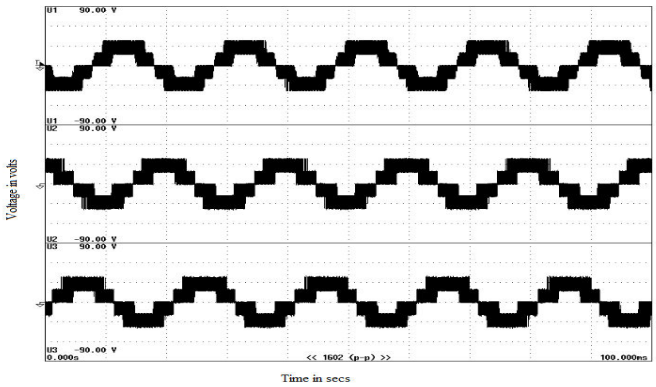

Fig. 25. Output Voltage Generated by PSPWM Technique.

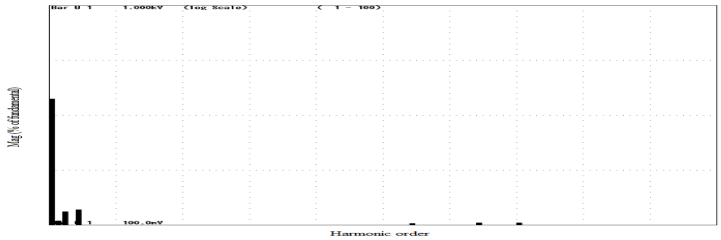

Fig. 26. FFT Plot for Output Voltage of PSPWM Technique.

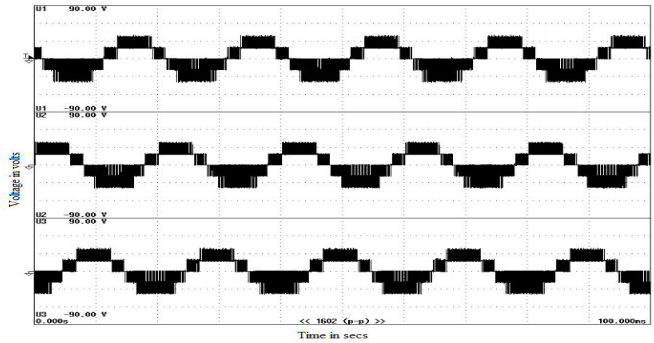

Fig. 27. Output Voltage Generated by (PD + PS) PWM Technique.

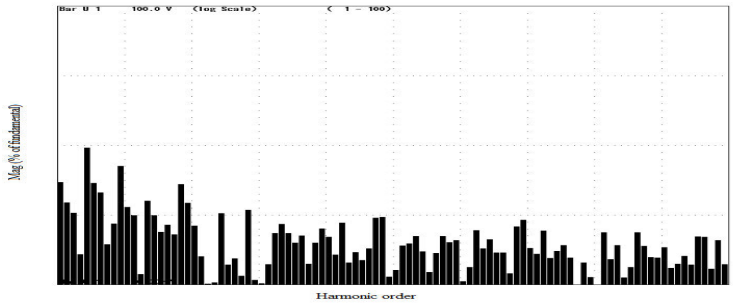

Fig. 28. FFT Plot for Output Voltage of (PD+PS) PWM Technique.

Table 6. % THD for Different Modulation Indices(by Experiment).

m_a	PD	POD	APOD	PS	PD+PS
1	18.22	10.28	17.59	12.87	18.47
0.9	19.23	12.74	19.59	14.27	20.40
0.8	20.76	15.68	21.47	17.18	20.29
0.7	20.50	15.48	21.75	18.99	23.74
0.6	19.91	15.98	24.15	20.70	29.56

Table 7. V_{RMS} (fundamental) for Different Modulation Indices (by Experiment).

m_a	PD	POD	APOD	PS	PD+PS
1	18.24	18.59	18.47	18.94	18.74
0.9	20.99	20.90	20.88	19.94	19.19
0.8	22.62	22.51	22.47	22.06	20.99
0.7	19.95	20.03	19.90	20.13	18.65
0.6	17.28	17.37	17.25	18.08	16.17

Table 8. Form Factor for Different Modulation Indices (by Experiment).

m_a	PD	POD	APOD	PS	PD+PS
1	INF	INF	INF	INF	INF
0.9	INF	INF	INF	INF	INF
0.8	INF	INF	INF	INF	INF
0.7	INF	INF	INF	INF	INF
0.6	INF	INF	INF	INF	INF

Table 9. Distortion Factor for Different Modulation Indices (by Experiment).

m_a	PD	POD	APOD	PS	PD+PS
1	0.165	0.204	0.154	0.261	0.871
0.9	0.174	0.201	0.161	0.251	0.912
0.8	0.181	0.206	0.185	0.193	1.901
0.7	0.206	0.177	0.163	0.149	1.170
0.6	0.229	0.203	0.256	0.138	1.410

6. Conclusions

Various bipolar PWM strategies with triangular carriers have been developed using MATLAB-SIMULINK and tested for different modulation indices ranging from 0.6-1 for the chosen three phase cascaded multilevel inverter are and then implemented in real time using FPGA. The results are satisfactory.

- It is observed from simulation results that (Table 1) APODPWM and PSPWM strategies provide output with relative low distortion.
- PS, APOD and hybrid PWM are found to perform better since they provide relatively higher fundamental RMS output voltage (Table 2) and Table 3 provides crest factor, Table 4 shows form factor and Table 5 provides distortion factor for all modulating indices.
- Various performance factors like (i) THD and harmonic spectra indicating purity of the output voltage, (ii) V_{RMS} indicating the amount of DC bus utilization, (iii) CF specify the peak current ratings of devices and components, (iv) FF measure the shape of the output voltage and (v) DF indicates the amount of harmonics that remains in the output voltage after it

has been subjected to second order attenuation related to power quality issues have been evaluated, presented and analysed.

- It is seen from hardware results (Table 6) that PODPWM strategy provides output with relative low distortion. PSPWM is found to perform better since it provides relatively higher fundamental RMS output voltage (Table 7) for all modulation indices. Table 8 provides form factor and Table 9 shows distortion factor for all modulating indices.
- The result analyses indicate that appropriate PWM strategies have to be employed depending on the performance measure required in a particular application of MLI based on the criteria of output voltage quality (Peak value of the fundamental, THD and dominant harmonic components).
- The proposed PWM methods with less THD and higher RMS voltage can be implemented in industrial applications such as AC Power conditioners, static VAR compensators, drive systems, etc., and in power generation industries.

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Appendix A

Performance Parameters

In the present work a number of factors are used for the prediction of the harmonics

Harmonic factor of n^{th} harmonic (HFn)

The harmonic factor (of the n^{th} harmonic), which measure of individual harmonic contribution, is defined as

$$HFn = V_{om} / V_{o1} \text{ for } n > 1$$

where V_{o1} is the RMS value of the fundamental component and V_{on} is the RMS value of the n_{th} harmonic component.

Total Harmonic Distortion (THD)

The total harmonic distortion, which is a measure of closeness in shape between a waveform and its fundamental component, is defined as

$$\text{THD} = 1/V_{o1}\left\{\sqrt{\sum_{n=2,3}^{\infty}\left(V_{on}\right)^2}\right\}$$

Distortion factor (DF)

THD gives the total harmonic content but it does not indicate the level of each harmonic component. If a filter is used at the output of inverters, the higher order harmonics would be attenuated more effectively. Therefore, knowledge of both the frequency and magnitude of each harmonic is important. The DF indicates the amount of HD that remains in a particular waveform after the harmonics of that waveform have been subjected to a second-order attenuation (i.e., divided by n^2). Thus, DF is a measure of effectiveness in reducing unwanted harmonics without having to specify the values of a second-order load filter and is defined as

$$DF = 1/V_{o1}\left\{\sqrt{\sum_{n=2,3}^{\infty}\left(V_{on}/n^2\right)^2}\right\}$$

The DF of an individual (or n^{th}) harmonic component is defined as

$DF_n = V_{pn} / V_{o1n^2}$ for $n > 1$

Lowest Order Harmonic (LOH)

The LOH is that harmonic component whose frequency is closest to the fundamental one and its amplitude is greater than or equal to 3% of the fundamental component.

Crest Factor (CF)

CF is a measure of peak input current I_s *(peak)* as compared with its RMS value I_s. CF is often of interest to specify the peak current ratings of devices and components. The CF of the input current is defined by

$$\mathrm{CF} = I_s(peak) / I_s$$

Form Factor (FF)

FF is a measure of the shape of the output voltage.

$$\mathrm{FF} = V_{RMS} / V_{avg} + C_{D_b}$$

where V_{RMS} is the RMS value of output voltage and V_{avg} is the DC content in the output voltage.