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DESIGN OF A 16-BIT ADDER FOR DECODER APPLICATION CIRCUIT

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Abstract

The aim of this paper is the design of an adder which relates to error checking and updating circuits required for the analysis of decoder circuits. The parameters such as Delay, Power dissipation, and PDP are usually considered in the design process. The proposed adder circuit uses dynamic logic technique and designed with pass transistor logic TTL configuration. The reduction of components is achieved as two transistors for every logic cell using the dynamic logic design. The proposed adder is implemented in 16 bit by cascading the adder circuit using the carry select adder technique and considering the parameters of delay, power dissipation, and throughput. The generated layout was simulated using VLSI CAD tools for 70 nm and 180 nm feature sizes. The proposed circuit results reflected the intention of having a lower power dissipation of 7.5 nW, reduced delay of 0.127 ns and a throughput of 3.69×10^{9} Gbps. This study emphasised that the proposed design resulted in a better output.

Keywords: Decoder, Delay, Dynamic logic, LDPC, Power dissipation, Throughput.

1. Introduction

An extensive range of adder architectures is used for different requirements such as low power consumption, better speed, and smaller area. Adders such ripple carry adders (RCA), Carry Look Ahead Adder (CLA), Carry Skip Adders (CSA) have been designed with improvement in some of the parameters for the required application circuit. When two logic bits along with a carry bit are added the full adders produces a Sum and Carry output. One of the ways to implement this function will be to use the transmission gate logic which uses the XOR function.

The proposed adder described in this paper is designed using dynamic logic. Dynamic logic depends on the temporary storage of charges (a voltage level). This concept allows us to implement simple circuits with memory functions such as full adders. Complex functions implemented with dynamic logic requires a smaller silicon area since it uses a reduced number of transistors and this helps in the lower consumption of power. This capability of the dynamic logic is used in the design of the proposed full adder. The adder design focuses on obtaining improved parameters of power dissipation, delay, and throughput which would be necessary for the implementation of the LDPC codes. The full adder has been designed using CAD tools for logic design and simulation tools for the layout design and timing simulation. The circuit is simulated, and results show substantially lower power dissipation, smaller delay, and improved throughput.

The proposed adder circuit designed by dynamic logic reduces the steps in design as well as the number of transistors used. The proposed adder is expected to produce power reduction in nanowatts and delay in nanoseconds due to its proper arrangement of transistor cell and it also eliminates power guard problems. This proposed adder is implemented into n bit CSA adder circuits which gives better results than other existing circuits. The adder circuits are imposed in VLSI CAD tool for evaluation and its layouts are generated by VLSI CAD tool.

In this paper Section 2 includes a review of current work in the area of design of adders, Section 3 describes the design of the proposed adder and simulation results have been tabulated and shown in Section 4. Finally, conclusions have been drawn in Section 5.

2. Base line Investigation

Adders have been designed for various applications and specific parameters were improved. These adders' circuits have been designed for 8 bit, 16-bit applications and have been proved to enhance the working capabilities of the circuit. A study of various full adders designed has revealed the enormity of uses of these circuits. was Vasant et al. [1] proposed a dual threshold HSCD domino adder structure using the dual HSCD technique for the Carry Look Adder (CLA) and the Carry-Skip Adder (CSK), which offered reduced delay values of 98.4 ps and 110.4 ps respectively. The use of the dual V_{TH} design helped reduce the power consumption by 18 % compared to other adder circuits. There was also a considerable reduction in leakage power under Clock High Input Low condition. Hiremath [2] presented a high speed 8 - bit carry select adder, which was implemented using 190 nm CMOS process technology. The proposed design by Hiremath [2] decreased the computational time and increased speed.

The propagation delay and power consumption obtained was 340ps and 13.77 µW. Nehru et al. [3] proposed a 64-bit low power parallel prefix adder using four different types of prefix cell operators. This design offered robust adder solutions used for low power and high-performance application needs. The design was suited for the arithmetic logic unit (ALU) and multiplier units for complex ranges of input data computation. Deepa and Kumar [4] reported that the energy efficient PTL based full adders were analysed using different nanometer technologies. 2-bit, 4-bit and 8-bit ripple carry adders were designed at 180 nm and were analysed for their performance in real time applications. Their study revealed that 8T and 13T ripple carry adders had the best delay and energy consumption values. In many of these designs, low power was the crucial parameter considered. Shirakol et al. [5] used a carry skip adder, which was designed to reduced the time required to propagate the carry by skipping over groups of consecutive adder stages. It was seen that carry-skip adders consumed more power, area and had less delay as compared to the ripple carry adders.

To overcome the problem of power and area, efficient full adders were used in the carry-skip adder design. Also,carry-skip adders were found to be faster than ripple carry adders due to its inherent property. Mehrabani and Eshghi [6] proposed the five full adders having driving power and one without driving in their paper, which focussed on high speed and low energy full adders which were noise and process variation tolerant. Simulations confirmed that the proposed circuits were superior in terms of power, delay, power delay product (PDP). Their design had the XOR/XNOR circuit using a combination of PTL and TGL for the novel two-input basic cell of the adder. Results obtained by the author show the design were robust. Chawla et al. [7] proposed an architecture using a combination of the multiplexing ability of the carry select adder and the ability to generate carry bits before the calculation of the sum of the carry look ahead adder to obtain an optimized power consumption and computation time. The 8-bit circuit proved to give a better timing performance and an increase in the number of bits showed better power consumption. Input test patterns play a dominant characteristic in the analysis of a circuit.

An improved test pattern having a primary and supporting set is designed such that any full adder design within the n-bit ripple carry adder can be forced to many possible input transitions. Mewada and Zaveri [8] proposed this circuit design, which can be used for measurement of maximum propagation delay and estimation of power dissipation. Each design of adders with a logic style has its own set of advantages and weaknesses. The adder designs discussed above met certain aspects such as power reduction and reduced delay however the design did not have minimization of the number of transistors used along with the reduction of power dissipation and increase in throughput. According to above mentioned investigation, our proposed adder trades off all drawbacks of existing methods. It gives better performance in terms of the arrangement of logical cells, reduced the power dissipation, area and increases the throughput

3. Design Method

The crux of design technology is to reduce the number of components used because; a large number of components would lead to more power dissipation, higher area requirements which inherently lead to propagation delays. The proposed adder circuit uses the dynamic logic to limit the number of CMOS

transistors. The operation of all dynamic logic gates depends on transient storage of charge in parasitic node capacitor instead of depending on constant state circuit behavior. A dynamic logic circuit gives a result at the output that is valid for only a short period of time. The capability of storing a state temporarily at a capacitive node allows implementing very simple sequential circuits with memory functions such as adders. The use of a common clock throughout the system enables to synchronize the operation of various circuit blocks.

The full adder designed in the proposed circuit exploits the properties of both NMOS and PMOS circuits. From design principle, it is seen that NMOS circuits are preferred as they are faster and occupy less space. But PMOS circuits cannot be totally avoided as they are useful in passing power supply voltage V_{DD} to the inner nodes. In the proposed circuit both NMOS and PMOS transistors have been used incorporating the dynamic logic principle and pass transistor logic.

Figure 1 shows the full adder circuit proposed in this study. It is the building block for the larger circuit. The full adder is given two inputs A and B and the third C_{in} as the carry input of the first stage. The Carry for the first stage is given as in equation 1. The full adder performs 2-bit addition and produces a corresponding sum bit and carry out a bit. The standard output of the full adder is characterized by two equations one for the Sum and another for the Carry. The Sum is given by $S = A \oplus B \oplus C_{in}$ and output Carry given by $C_{out} = AB + BC_{in} + AC_{in}$. Using the concept of Multiplexing Control Input technique (MCIT) where one of the inputs is the control input, the standard Boolean expression for Sum and Carry of the full adder are derived using the Karnaugh map.

The sum circuit is designed based on PMOS transistor which gives current carried by holes from source to the drain. So the output voltage will not leak into the drain terminal, and hence gives a better output voltage through an induced p-type channel. The inputs C_{in} forms the control input. The value of C_{in}, whether it is 1 or 0, decides the output of Sum(S) and Carry (C_{out}) of the adder. The Sum which requires the XOR of A, B and C_{in} is obtained from a combination of PMOS transistors and the inverters. The XOR with the series NMOS transistors is used to obtain the expression for Carry (C_{out}). When input voltage is applied to the gate the hole current in the body (p-type substrate) are driven away from the gate. This allows forming an n-type channel between the source and the drain and a current is carried by electrons from source to the drain terminal through an induced n-type channel.

The design for the Sum and Carry outputs of the proposed adder is developed based on the following equations

$$S = \overline{\left(\overline{AB + \bar{A}\bar{B}}\right)C_{in}} + (AB + \bar{A}\bar{B})C_{in} \quad (1)$$

$$C_{out} = AB + \left(AB + \overline{A}\overline{B}\right)C_{in} \quad (2)$$

It has been seen that the full adder circuit proposed gives a better performance in terms of power dissipation delay and latency as shown by the simulation results. Figure 2 shows the conceptual circuit diagram of the full adder

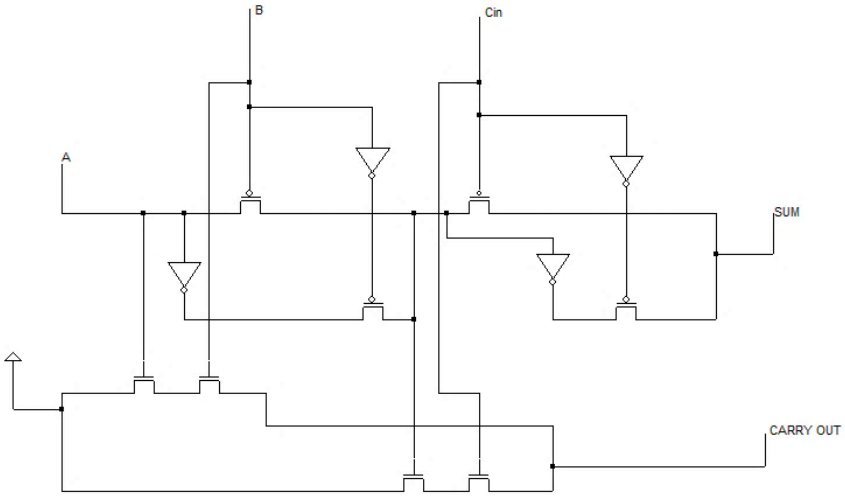

Fig. 1. Proposed full adder circuit.

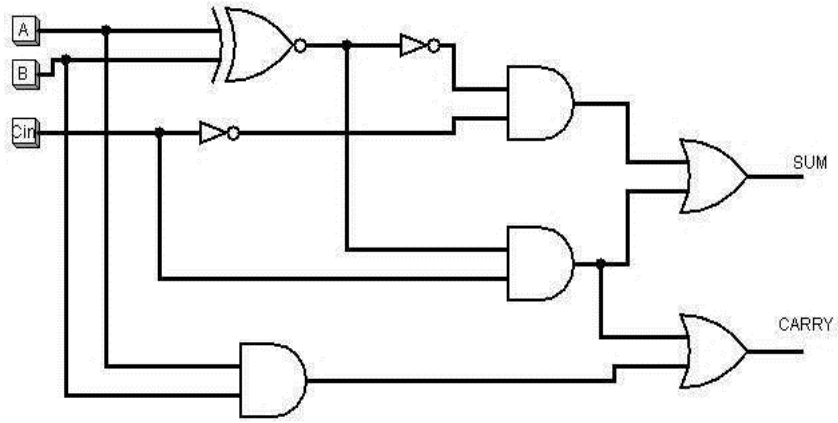

Fig. 2. Conceptual circuit diagram of proposed adder.

The full adder circuit that is proposed when used in an application needs to be cascaded to allow for the addition of a larger number of bits. The adder circuit is then cascaded into a number of stages. In our simulation, a 16-bit full adder using the concept of carrying select adder has been designed. The C_{in} input controls the transfer of the 'carry bit' from one adder to the other. Using a multiplexer, the output values of Co are determined for both when C_{in} = 0 and C_{in}=1. The result for the next stage is determined by making a minimum delay in the circuit. If there are 'n' numbers of stages, the value of 'Sum' and 'Carry' functions can be determined using the following equations. Say for the i^{th} stage, the formula is given by,

$$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i \quad (3)$$

$$S_i = A_i \oplus B_i \oplus C_i \quad (4)$$

The proposed full adder circuit is the cascaded for 16 input bits as shown in Fig. 3:

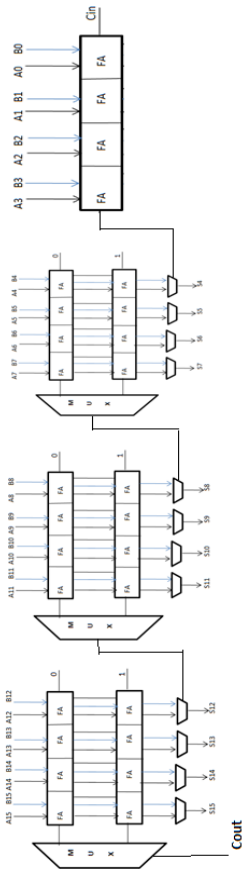

Fig. 3. 16-bit full adder circuit.

The CSA full adder circuit in Fig. 3 shows the inputs of A0 to A15 and B0 to B15 being cascaded to form the 16-bit full adder. The first set of adders with inputs A0 to A3 and B0 to B3 are fed to the full adder circuit along with the C_{in}. Addition of these inputs results in the sum and carry out for this stage. In the consequent stage, it can be seen the carry output is sent to the next stage where values if carry=1 and carry=0 have been calculated prior to receive the carry out from the first stage. This reduces the delay to calculate the output of the carry input to the next stage. Depending on the value of carrying out from the first stage, the multiplexer selects the appropriate carry in and the addition of inputs (A4 to A7 and B4 to B7) of next stage is completed. This process follows for all stages

4. Results

The CSA full adder circuit in Fig. 3 shows the inputs of A0 to A15 and B0 to B15 being cascaded to form the 16-bit full adder. The first set of adders with inputs A0 to A3 and B0 to B3 are fed to the full adder circuit along with the C_{in}. Addition of these inputs results in the sum and carry out for this stage. In the consequent stage, it can be seen the carry output is sent to the next stage where values if carry=1 and carry=0 have been calculated prior to receive the carry out from the first stage. This

reduces the delay to calculate the output of the carry input to the next stage. Depending on the value of carrying out from the first stage, the multiplexer selects the appropriate carry in and the addition of inputs (A4 to A7 and B4 to B7) of next stage is completed. This process follows for all stages

The results shown in Table 1 for the proposed full adder reflects the improvements in parameters. The dynamic logic used in the design helped reduce redundancy of components and made the design more compact. The input to the proposed full adder circuit could use values from 0000 to 1111 for the inputs A, B, and C_{in}. If the input to the circuit is, say, A = 0, B = 1 and C_{in} = 1, then it will be seen that the addition of these bits will have a sum of Sum = 0 and it will generate a carry of Carry out = 1 according to principles of Boolean algebra. The design has complementary pairs of NMOS and PMOS transistors which contribute to low power consumption because any of the transistor in the pair is off and power is drawn only during switching. The dynamic power, caused by power rushing from V_{DD} to Ground when both pull up and pull down networks are partially On while a transistor switches, is reduced. The proposed adder gives low power dissipation of 9.1 µW which is 74.66% less as compared to existing circuits at 70 nm feature size due to the reduced number of transistors used and the layout of the transistor cells which reduces the switching between level 1 to 0 which is one of the sources of power dissipation [9].

Table 1. Proposed full adder results.

Characteristic	Value	Value
Feature Size	70 nm	180 nm
Vo	0.7 V	2 V
$I_{D\,(av)}$	0.013×10^{-3}A	0.058×10^{-3}A
t	4.205×10^{-9} s	4.037×10^{-9} s
Delay (τ)	0.127×10^{-9} s	0.169×10^{-9} s
Throughput	230.95 Mbps	237.75 Mbps
$P_d = V_o\, I_{D(av)}$	9.1×10^{-6} W	0.0116×10^{-3}W
Power Dissipation	0.075×10^{-6} W	0.156×10^{-3}W
Latency (*T*)	4.330×10^{-9} s	4.206×10^{-9} s

From Table 1, it can be seen that the reduced delay of 0.127ns and 0.169 ns obtained for both 70nm and 180nm respectively, contributes to the latency having values of 4.33 ns and 4.206 ns respectively because of the increased utilization of silicon area and reduced interconnection parasitic within the cell due to the arrangement of transistor cells. The proposed 1-bit full adder circuit shows a throughput of 230.95 Mbps and 237.75 Mbps for 70nm and 180nm feature sizes respectively. The reduced power and the minimized delay contribute effectively to a high throughput in the circuit.

The performance of the proposed 1-bit full adder circuit is compared with other existing full adder circuits in the feature sizes of 70 nm and 180 nm. A comparison of the results is tabulated in Table 2.

The proposed full adder circuit performance is compared with other referenced circuits in terms of Power dissipation, Delay, and Throughput parameters. The power dissipation for the proposed full adder circuit with a feature size of 70 nm, has a lower power dissipation as compared to Ref 9 and Ref 6 with an improvement

of 99.8% and 47.91% respectively and an improvement of 96.6 % with Ref 2 having a feature size of 180 nm. The better performance of the proposed circuit in terms of power dissipation is due to the regular arrangement of transistor cells. When transistor cells form a regular pattern of NMOS and PMOS transistors, the current flow from the source to drain is smooth. Referring to the circuit in Fig. 1, NMOS transistors are used in series to obtain the Carry Out for the proposed full adder and a combination of PMOS transistors are used to obtain the Sum of the full adder. It is seen that the power guard problem is eliminated due to this arrangement. The propagation delay is due to the rise (from logic 0 to logic 1) and fall (from logic 1 to logic 0) of voltage during switching.

Table 2. Comparison of proposed full adder circuit with references.

Circuit	Technology (nm)	Power Dissipation P_D (µW)	% of improvement	Delay τ (ns)	% of improvement	PDP (J)
Proposed circuit	70	0.075	-	0.127	-	9.525×10^{-18}
	180	0.156	-	0.169	-	0.0264×10^{-12}
Patel et al. [10]	70	56	99.8	0.396	67.92	0.022×10^{-12}
Hiremath [2]	180	4.7	96.6	0.0987	-71.2	0.463×10^{-15}
Deepa and Kumar [4]	180	-	-	0.244	30.73	-
Mehrabani and Eshghi [6]	70	0.144	47.91	0.0282	-	-

From Table 2 above, the delay in the proposed full adder circuit shows smaller delay as compared to Ref 4 with 44% improvement because of the cascading of PMOS and NMOS transistors in a compact arrangement in the proposed circuit. The current transition in the node is regular due to the circuit arrangement similar to the CMOS structure. The throughput of a circuit is dependent on the delay of the circuit. In Table 2, the proposed circuit shows that the power is reduced and the delay is minimized due to circuit design. Hence the throughput for the proposed full adder is increased due to reduced delay and gives 230.35 Mbps for 70 nm and 237.75 Mbps for 180 nm feature size. Therefore, it can be derived that the proposed circuit has achieved a substantial improvement in the design of a full adder.

For further analysis, the designed full adder was analysed using the CAD tool for parametric analysis. The variation of voltage with power and voltage with final voltage for 70 nm and input voltage vs power and maximum current for 180 nm obtained is shown in the graphs below in Figs. 4 (a) to (d). For the 70 nm feature size, the power analysis showed an exponential increase as the voltage V_{DD} increases in Fig. 4(a). A sudden sharp increase was seen after 0.5V when the power consumed was 0.063 mWatts. The sudden increase is due to the fact that at 0.5V the transistor gate overcomes the resistance of the layer and allows the flow of carriers and is seen to reach a value of 0.375 mW at 0.7V. The variation of input voltage with power for 180 nm in Fig. 4(b) shows an exponential increase as the voltage increases from 0.4V and reaches a maximum of 0.586mW at 2V. The power dissipated is small due to the arrangement of transistor cells and optimized Area of 864 µm^2. For 70 nm and 180 nm feature sizes, the input voltage versus power is shown below in Figs. 4(a) and (b).

For 70 nm feature size, the input voltage versus final voltage and for 180 nm feature size, the input voltage versus maximum current is shown below in Figs. 4(c) and (d).

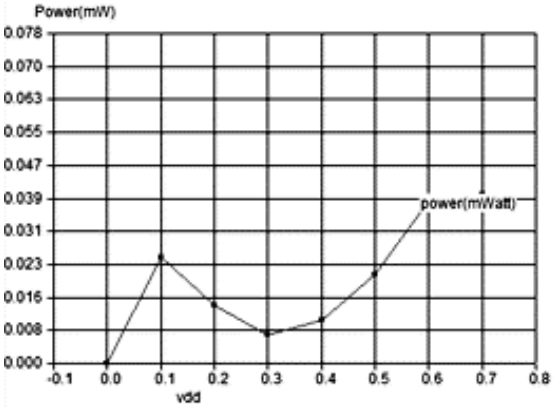

Fig. 4(a). Voltage (V_{DD}) vs. power (P) for 70 nm.

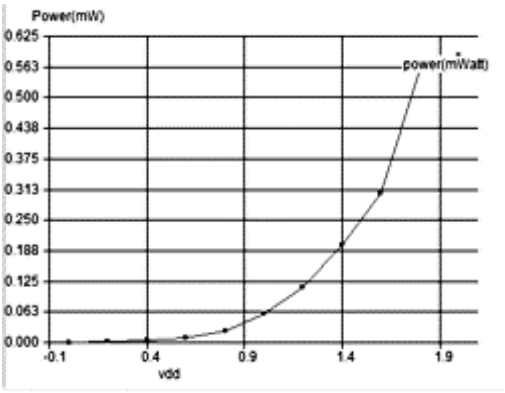

Fig. 4(b). Voltage (V_{DD}) vs. power (P) for 180 nm.

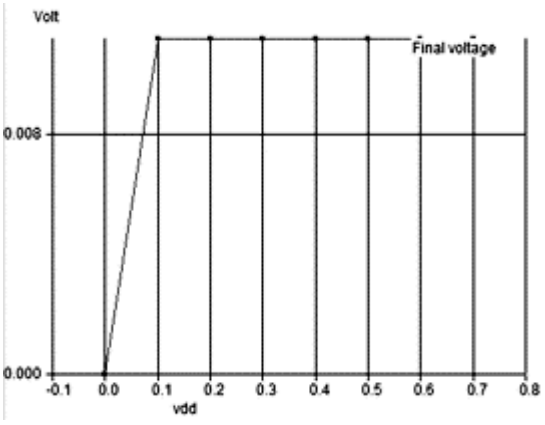

Fig. 4(c). Input voltage vs. final voltage for 70 nm.

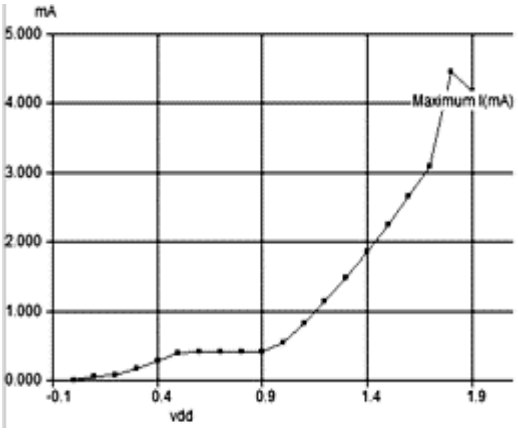

Fig. 4(d). Input voltage vs. maximum current 180 nm.

The variation of V_{DD} with the final voltage is shown in Fig. 4(c). The graph shows that between 0 to 0.1V there is a slow increase in final voltage due to the time required for the change in voltage levels between logic 0 and logic 1. At 0.1V, for any further increase in input voltage the final voltage maintains a maximum approximate steady value which is very small and leads to less power dissipation. This is due to the circuit using dynamic logic characteristics.

The change in current I_{Dmax} with the input voltage V_{DD} for 180 nm in Fig. 4(d) is also a slow exponential increase from 0.1V to a maximum of 4.168 mA at 2V of the input voltage. Even though no steady-state current flows, the transistors in ON condition or logic 1 supplies current to an output load if the voltage changes from 0V or V_{DD}. The parametric analysis confirms that the proposed circuit performs according to expected results

5. Conclusions

The proposed full adder uses the dynamic logic technique and the pass transistor logic in the design and the results show that the model satisfies the intended outcome. The circuits are simulated using CAD tools and results obtained show improvement. The proposed 1-bit full adder is cascaded to form a 16-bit carry select adder and the average power consumption was found to be 9.1 µwatts by a combination of NMOS and PMOS transistors. Overall in terms of performance, the proposed circuit has an improved power dissipation of 0.075 µwatts. It also reduced the delay by 0.127 ns which is due to the transistor cell arrangement in the design. The area for the layout is considered small (3.36 mm^2). The throughput is high because of the optimal utilization of silicon area which reduces the delay and the reduced power dissipation, which makes this circuit suitable for communication applications. The characteristics of lower power dissipation and better throughput give the opportunity to use the proposed full adder circuit in a decoder. The decoder architecture of a communication network requires a cascaded full adder. The cascaded full adder performs the comparison and approximations of the data stored in the memory of the decoder with the bits received from the router of the decoder. This circuit can be used to develop a decoder for communication application as in Low-Density Parity Check (LDPC) codes

Nomenclatures

C_{in}	Carry in
C_{out}	Carry out
$I_{D(av)}$	Average current, mA
P_D	Power dissipation, W
P_d	Power output, W
t	Time, s
V_{DD}	Supply voltage, V
V_O	Output voltage, V
V_{TH}	Threshold voltage, V

Greek Symbols

τ	Delay, s

Abbreviations

ALU	Arithmetic logic unit
CAD	Computer aided design
CLA	Carry look ahead adder
CMOS	Complementary metal oxide semiconductor
CSA	Carry select adder
CSK	Carry skip adder
HSCD	High speed clock delayed
LDPC	Low density parity check code
MCIT	Multiplexing control input technique
NMOS	n-type metal oxide semiconductor
PDP	Power delay product
PMOS	p-type metal oxide semiconductor
PTL	Pass transistor logic
TGL	Transistor gate logic

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